Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7612D PROGRAMMABLE DIGITIZER

For Qualified Service Personnel Only

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-2387-00
Product Group 45

Serial Number _____

First Printing DEC 1982
Revised JUN 1983

INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont)

LIST OF ILLUSTRATIONS (cont)

LIST OF TABLES

SAFETY SUMMARY

The general safety information contained in this summary is for servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL


Static-Sensitive Devices


This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT


DANGER—High voltage.


Protective ground (earth) terminal.


ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition.

For detailed information on power cords, see Figure 4-3, in Section 4, Installation and Maintenance.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making connections to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

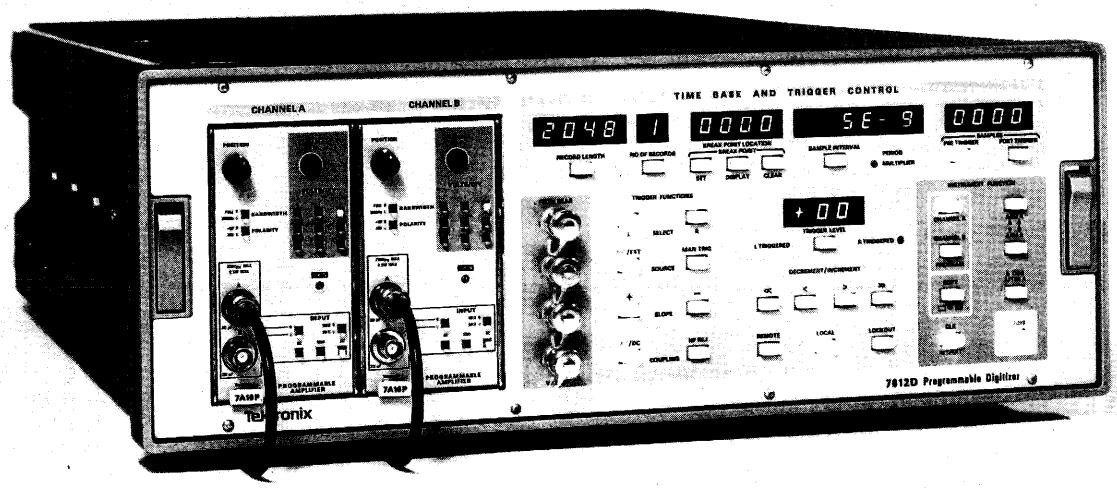
Disconnect power before removing protective panels, soldering, or replacing components.

HANDLING ELECTRON-BIASED SEMICONDUCTOR (EBS) TUBES

Use care when handling an EBS tube. Breakage of the EBS tube causes a high-velocity scattering of glass fragments (implosion). Protecive clothing and safety glasses should be worn. Avoid striking the EBS tube on any object which might cause it to crack or implode. When storing an EBS tube, place it in a protective carton or set it in a protected location on a smooth surface on a soft mat.

SILICONE GREASE HANDLING

Handle silicone grease with care. Avoid getting the silicone grease in your eyes. Wash hands thoroughly after using silicone grease.



2387-999

7612D FEATURES

The TEKTRONIX 7612D Programmable Digitizer is a dual-channel digitizing instrument with a sample rate of 1 Hz to 200 MHz. Digital data representing the input signal is stored in 4,096 eight-bit words (2,048 per channel) of local high-speed semiconductor memory. This data can be displayed on an XYZ monitor or transferred via GPIB (IEEE Standard 488-1978) to peripheral equipment.

The 7612D is fully programmable via the GPIB. Table 2-3, in Section 2, lists the IEEE 488-1978 interface functions implemented in the 7612D.

The 7612D will accept any 7000-series plug-in amplifier. Table 1-3, in Section 1, shows how bandwidth, sensitivity, and other features vary with different plug-in amplifiers.

GENERAL INFORMATION

This section contains a basic content description of both the Operators and Service Manuals, information on instrument installation, packaging for shipment, and specifications. The Specification portion consists of three tables; Electrical, Environmental, and Physical Characteristics.

This section also contains a Standard Accessories list and a full-page instrument dimensional drawing.

The 7612D Programmable Digitizer can sample at rates up to 200 MHz, digitize, and store data about two waveforms. The digitized data can be displayed on an XYZ monitor or transferred to a peripheral device via the IEEE 488 bus.

OPERATORS MANUAL

Section 1—INTRODUCTION contains a brief description of the 7612D and its distinctive features, and lists standard accessories.

Section 2—FRONT-PANEL OPERATION contains a description of the controls, indicators and connectors, and tells how to operate the 7612D.

Section 3—PROGRAMMING contains an introduction to the IEEE 488 bus, a discussion of the IEEE 488 interface functions implemented in the 7612D, and a description of the 7612D command set.

Section 4—INSTALLATION tells how to install the 7612D in a rack and how to connect it to other equipment.

Section 5—SPECIFICATIONS contains definitions of characteristics unique to digitizing instruments, and electrical system, environmental, and physical characteristics of the 7612D.

Section 6—BLOCK DIAGRAM consists solely of the 7612D block diagram.

SERVICE MANUAL

WARNING

THE SERVICE MANUAL CONTAINS INSTRUCTIONS FOR USE BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID PERSONAL INJURY. DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

Section 1—GENERAL INFORMATION contains instrument description, electrical specifications, environmental characteristics, standard accessories, and packaging for shipment instructions.

Section 2—OPERATING AND PROGRAMMING contains information about front- and rear-panel controls, connectors and indicators, and other information relative to operating the 7612D. The Programming part contains an introduction to the IEEE 488 bus, a discussion of the IEEE 488 functions implemented in the 7612D, and a description of the 7612D command set.

Section 3—THEORY OF OPERATION contains general and specific circuit analysis for use when servicing or operating the instrument.

Section 4—INSTALLATION AND MAINTENANCE contains information about installing the 7612D in a rack, connecting signals and power, configuring an IEEE 488 system, selecting internal jumpers, preventive maintenance, troubleshooting, and corrective maintenance.

Section 5—CALIBRATION contains procedures to check the performance and electrical characteristics of the 7612D, and methods to adjust it to meet specifications.

Section 6—INSTRUMENT OPTIONS contains a description of available options and locations of incorporated information about those options.

Section 7—REPLACEABLE ELECTRICAL PARTS contains lists of replaceable parts and assemblies.

Section 8—DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS includes detailed circuit schematics, locations of assembled boards within the instrument, circuit board component locators, and locations of adjustments to aid in performing the Adjustment and Performance Check part of the Calibration procedure.

Section 9—REPLACEABLE MECHANICAL PARTS includes lists of replaceable mechanical parts and shows exploded views which identify assemblies.

DESCRIPTION

The TEKTRONIX 7612D Programmable Digitizer is a microprocessor-based dual-channel waveform digitizing instrument with a maximum sample rate of 200 megahertz. Up to 4,096 eight-bit words (2,048 per channel) can be stored in a local high-speed semiconductor memory for subsequent display on an XYZ monitor or transfer over the bus specified in IEEE Standard 488-1975 (commonly referred to as GPIB—General Purpose Interface Bus). The 7612D is fully programmable over the IEEE 488 bus. Table 2-3 in Section 2 summarizes the IEEE 488 interface functions implemented in the 7612D.

Local data memory can be partitioned into one to eight records of equal length. These records can be further divided into one to fourteen segments, each with a programmable sampling interval. The sampling interval is selectable from five nanoseconds to one second using the internal crystal-controlled clock. When an external clock signal is used, the period of the applied signal can be multiplied by a selectable multiplier from one to 200×10^6.

The sample interval switching is coherent for all intervals greater than five nanoseconds. That is, the last sample of a segment is the time-origin of the following segment.

Two independent digital time bases can be individually programmed for memory partitioning, sampling interval, and triggering functions. Because the channels are independent, digitized data can be read from one channel while the other channel is acquiring data.

The 7612D front panel allows complete local control of the instrument with a simple, logical panel layout. Operating parameters are set by pressing the appropriate function key and decrementing or incrementing the parameter with the DECREMENT/INCREMENT keys. The parameter cycles through only those values which are valid for the current state of the instrument, minimizing the possibility for error. The instrument checks the setting each time the ARM button is pressed in local state or the ARM command is received in remote state. Errors are reported on the front panel and over the IEEE 488 bus.

Remote control, front-panel operation, and data output via the IEEE 488 bus are simplified by the microprocessor system in the 7612D. The firmware operating system makes the front panel "friendly" and allows the programmer to use simple high-level mnemonics to communicate with the instrument over the bus.

Extended IEEE 488 addresses are used so that the 7612D can act as an interface for programmable plug-ins such as the 7A16P Programmable Amplifier. A variety of 7000-series plug-ins are available to tailor the 7612D for bandwidth, input impedance, differential or single-ended input and input voltage.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped for long distances by commercial transportation, we recommend that the instrument be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

Also, if this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

If the original packaging is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton with a 375-pound test strength and having inside dimensions at least six inches greater than the instrument dimensions to allow for cushioning.

2. Enclose the instrument with polyethylene sheeting or equivalent to protect the finish.

3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on each side.

4. Seal the carton with shipping tape or with an industrial stapler.

5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

SPECIFICATIONS

DEFINITION OF CHARACTERISTICS

This discussion defines the terms and provides background for the techniques used to specify the performance of the 7612D.

ACCURACY

Many of the parameters used to specify low-frequency A/D converters are difficult to measure accurately at frequencies above 10 megahertz. In order to accurately specify the performance of the 7612D for higher frequencies, a signal-to-noise ratio is used. This parameter accumulates all of the errors in the A/D converter, excluding any gain and offset errors in the amplifier. Differences between the analog input signal and the digitized output data can be thought of as noise, so the ratio of signal to noise represents the accuracy of the converter.

An ideal A/D converter has some error because there are a finite number of levels available to define the analog input. This error is called quantizing error. Figure 1-1 shows the output and quantizing error for an ideal A/D converter.

In practice, other errors (e.g. nonlinearity) add to the noise signal. As a result, the noise signal represents the accumulated errors in the converter and the signal-to-noise ratio precisely represents the accuracy of the converter.

The signal-to-noise ratio for an ideal converter of N-bits resolution with a full-scale sine-wave input is:

$$S/N = 6N + 1.8dB$$

Where N = the converter's resolution in number of bits

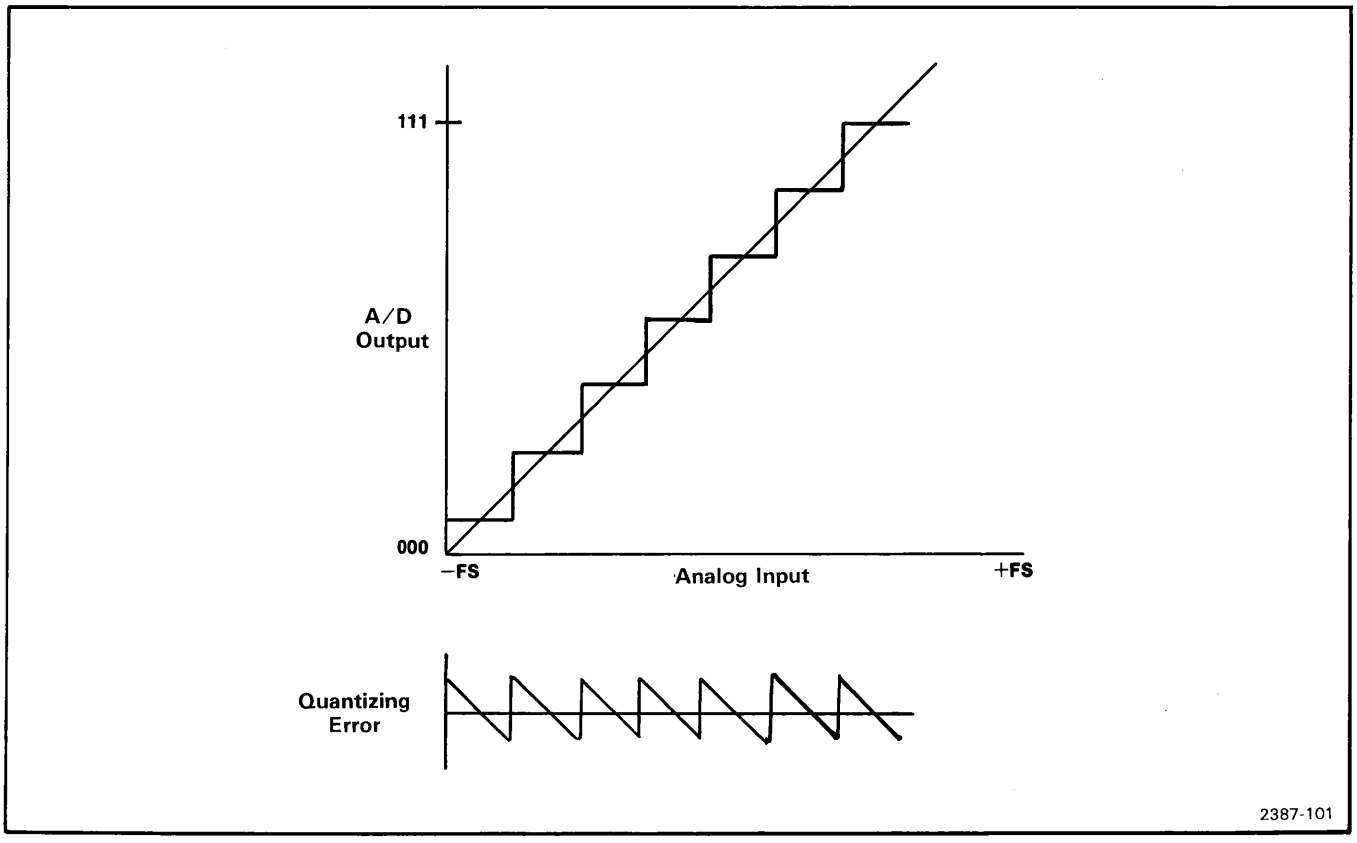


Figure 1-1. The output of an ideal A/D converter showing the quantizing error.

Table 1-1 shows the signal-to-noise ratio calculated for ideal A/D converters of five through eight bits resolution. On this basis, an actual converter's accuracy can be specified in terms of the performance of an ideal converter. For example, if an eight-bit converter has a signal-to-noise ratio of 43.8 dB at 10 megahertz, it is performing to the level of an ideal seven-bit converter. The converter, therefore, has seven effective bits. The effective number of bits for any A/D converter can be calculated from the signal-to-noise ratio by interpolating between the values shown in Table 1-1.

TABLE 1-1
Signal-To-Noise Ratios For Ideal A/D Converters with Full-Scale Sine-Wave Input

No. of Bits	S/N Ratio
8	49.8 dB
7	43.8 dB
6	37.8 dB
5	31.8 dB

MONOTONICITY

If the actual value of the A/D converter's least significant bit (LSB) deviates from the average LSB value by more than one LSB, there will be missing output codes and the codes may decrease at some point with an increasing analog input. When the output code decreases with an increasing analog input, the converter is said to be nonmonotonic. Figure 1-2 shows an example of a nonmonotonic output. The 7612D is checked for monotonicity as part of the performance check procedure given in section 5.

COHERENT SAMPLE INTERVAL SWITCHING

The 7612D sample interval switching is coherent for all sampling intervals greater than 5 nanoseconds. That is, the last sample of a segment is the time-origin of the following segment. Figure 1-3 shows an example of coherent sample-interval switching.

All 7612D sample intervals are integer multiples of the basic clock interval (five nanoseconds when the interval clock is selected, or the period of the external clock signal when external clock is selected). The selected sampling interval is generated by dividing the clock signal by an integer value. Sample-interval switching is implemented by changing this division ratio. For example, assume that the sampling interval for the first segment of a record is set to 10 nanoseconds. A breakpoint at location 128 changes the interval to 20 nanoseconds. Figure 1-4 shows a simplified timing diagram of the sample interval switching.

When the last sample of the first segment is stored, the internal dividers re-configure to change the clock division ratio from two (10 nanoseconds) to four (20 nanoseconds). For sampling intervals greater than five nanoseconds, the time required for the dividers to re-configure for a new sampling interval is less than the sampling clock period. As a result, the first sample of the second segment is taken exactly (within the clock accuracy) 20 nanoseconds after the last sample of the first segment, as shown in Figure 1-4. Thus, the sample

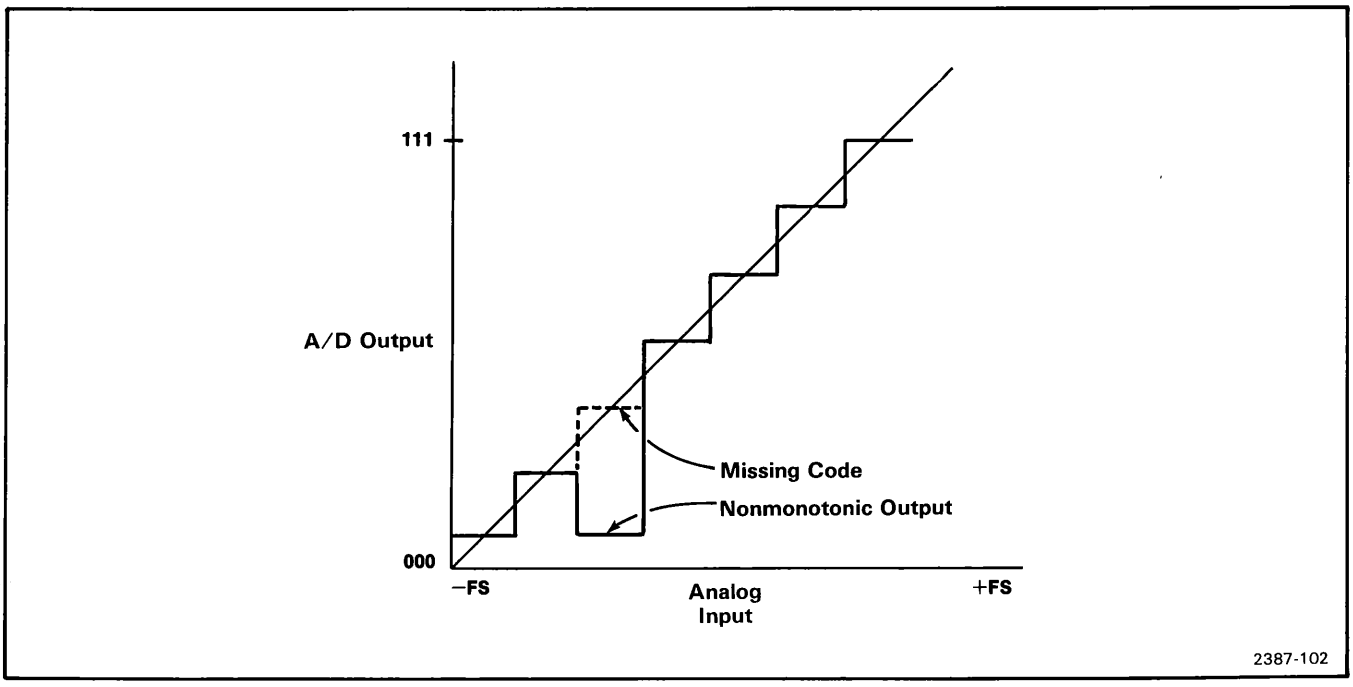


Figure 1-2. An example of missing output codes and nonmonotonicity.

interval switching for all intervals greater than five nanoseconds is perfectly coherent by the previously stated definition.

A Time Measurement Accuracy specification is included as a performance requirement to check the overall sampling accuracy of the 7612D. If the measured value (as measured by the procedure given in the performance check procedure in section 5) is within the limits given in Table 1-2, the instrument is operating properly, and coherence is ensured.

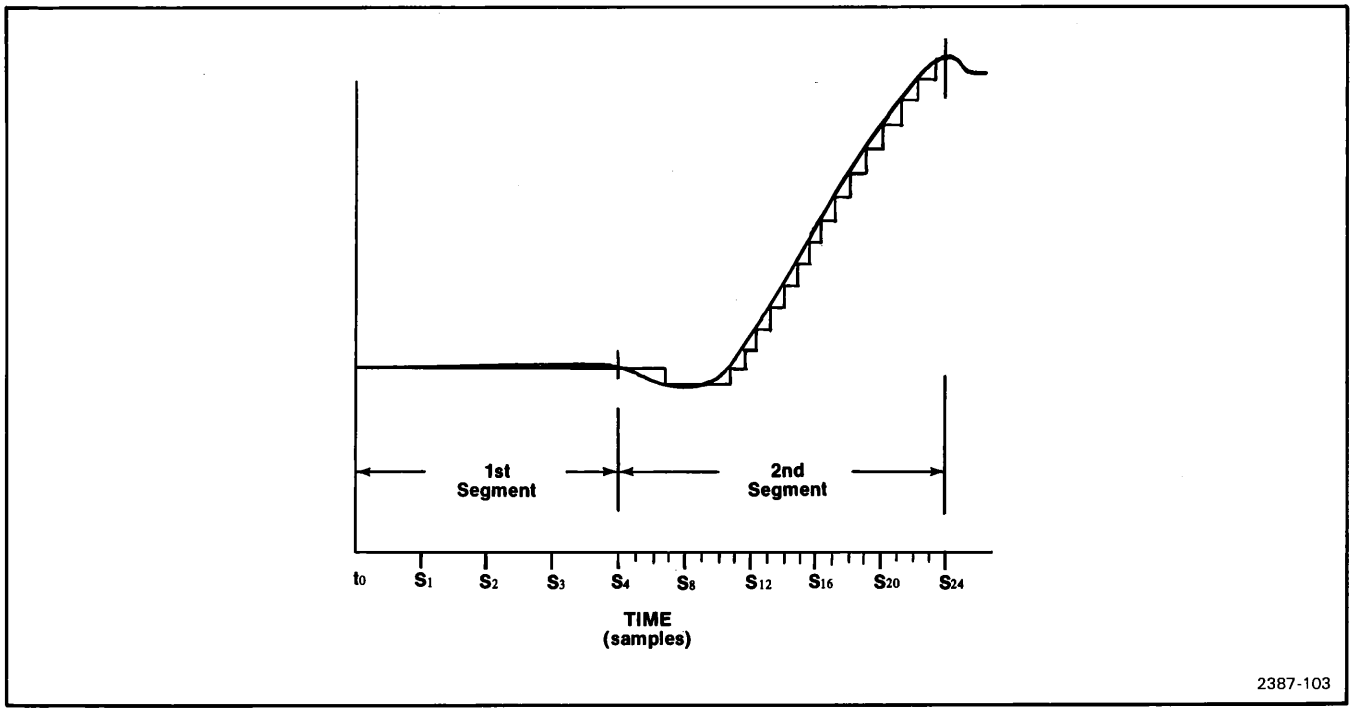


Figure 1-3. Two coherent samples showing sample-interval switching.

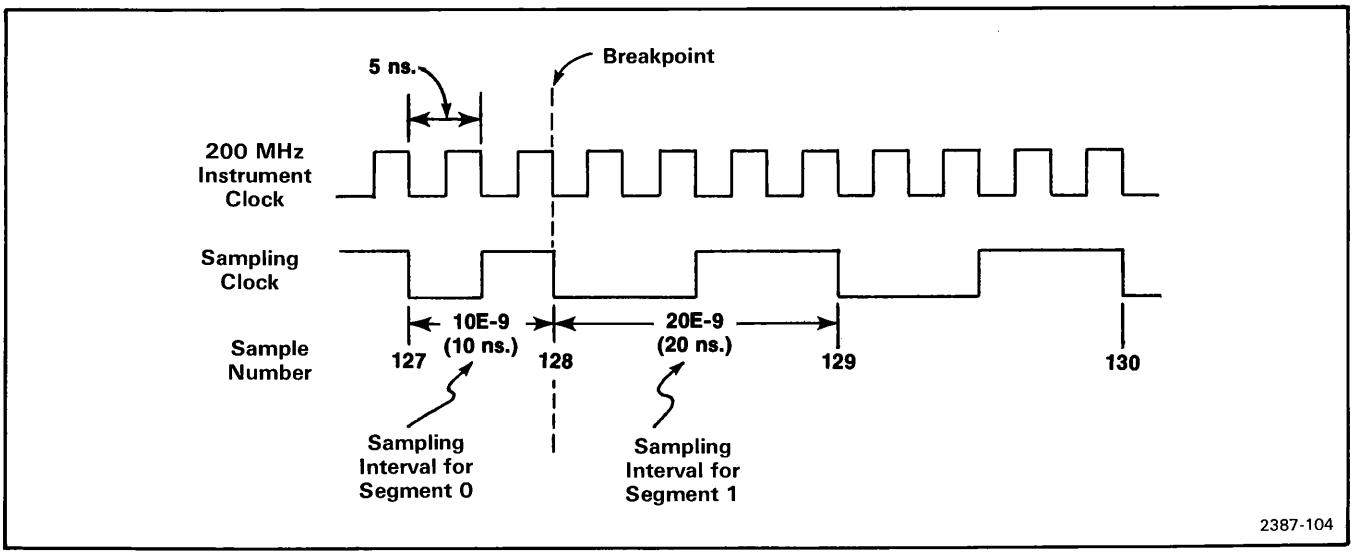


Figure 1-4. Timing for a sample-interval change in the 7612D.

CHARACTERISTICS

Electrical characteristics of the 7612D are listed in Tables 1-2 and 1-3. To be valid, the following conditions apply:

1. The 7612D and its plug-in units must have been calibrated at an ambient temperature between +20 and +30 degrees C.

2. The 7612D and its plug-in units must be allowed to warm up for at least 30 minutes with all covers installed.

3. The calibration of the 7612D must be checked according to the performance check procedure given in section 5 within each 1000 hours of operation or every six months if operated infrequently. Any adjustments that cause performance outside the limits allowed by the calibration procedure must be readjusted. The plug-in units must also be calibrated within their calibration intervals.

4. The 7612D and its plug-in units must be operated within their specified environmental limits (Table 1-4). In some cases, an electrical characteristic applies only to a limited temperature range or must be derated to apply to the entire temperature range. These cases are noted in the tables. Statements in the Performance Requirements column are verified in the performance check procedure (refer to section 5), except where special equipment or software is required. In these cases, the characteristic may be checked at any Tektronix field service center.

Statements listed in the Supplemental Information column are not verified in the calibration procedure.

Physical characteristics are listed in Table 1-5.

TABLE 1-2
Electrical Characteristics

Characteristics	Performance Requirements			Supplemental Information
A/D CONVERTER PERFORMANCE				
Accuracy[1]	Signal Freq.	S/N Ratio	No. of Effective Bits	
	300 kHz 20 MHz 80 MHz	42.0 dB 32.0 dB 20.0 dB	7.8 6.0 4.0	Measured with 7A19 Amplifiers; digitized output = 128 levels p-p. Measured at 25° C.
Monotonicity	Monotonic at 300 kHz.			
VERTICAL DEFLECTION SYSTEM				
Bandwidth 7612D Only (signal applied differentially at plug-in connector)	90 MHz, -3dB.			See Table 1-3 for system specifications.
Aberrations-Response to 192 LSB Positive Step 7612D Only (signal applied differentially to plug-in connector)	+4% or -4%, total, 4% peak-to-peak.			
Low-Frequency Step Response	Less than ±1%, total 1% peak-to-peak tilt or overshoot.			Excluding first 300 ns. 0° to 40°C.

[1]**The procedures for verifying this characteristic require special equipment and/or software. As such, it is not checked in the Performance Check Procedure given in the 7612D Service Manual. The characteristic can be checked at any designated Tektronix field service center.**

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristics	Performance Requirements	Supplemental Information
A AND B TIME BASES		
Clock		
Internal Rate	200 MHz ±0.0035%.	0° to +40° C ambient. Tested at +25° C.
Stability, Long-Term		10 ppm/year.
External Clock In		
Frequency Range	Less than or equal to 200 MHz.	
Input Level		ECL levels.
Input Impedance		50 ohms nominal.
Rise and Fall Times	Less than or equal to 1 ns.	
Pulse Width	2.5 ns minimum.	
Internal Clock Out		CLOCK OUT will drive one additional 7612D EXT CLOCK IN connector.
Time Measurement		
Accuracy	±0.0035%.	For all sampling intervals slower than 5 nanoseconds when sample interval switching is used.
Stability		10 ppm/year.
Sampling Interval (SI) Internal Clock A		Can be selected within the range of 5 ns to 1s. Allowable values are given by this formula: $SI=(5\ ns)(X \bullet 10^{y})$ where X=1,2,4,6,8,...,20 and y=0,1,...,7.
External Clock		External clock period multiplier values within the range of 1 to 200×10^{6} can be selected. Allowable values are given by this formula: $SI=(CLOCK)(X \bullet 10^{y})$ where x=1,2,4,6,8,...,20 and y=0,1,...,7.
Interval Switching		Sample Interval can be switched coherently between segments for all sampling intervals slower than 5 ns with 1 to 14 segments allowed per record.
Postrigger		Selectable in integer multiples of eight from eight to the record length. (Requires selection of only one record.)
Pretrigger		Selectable multiples of eight samples from zero to 16 less than the number of samples in the first segment. (The instrument acquires one full record of pretrigger data at the sampling rate of the first segment before becoming triggerable when in the pretrigger mode.)

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristics	Performance Requirements			Supplemental Information
A AND B TIME BASES (CONT)				
Triggering Ambiguity[2]	±1 sample ambiguity in recognizing the trigger. One sample maximum recognition between channels.			Using same trigger channel for both time bases.
TRIGGERING				
Trigger Sensitivity to Repetitive Signals	Triggering Frequency Range	Minimum Signal Required		
Coupling:		Internal	EXT	
AC	40 Hz to 50 MHz	20 LSB	100 mV	
	50 MHz to 100 MHz	44 LSB	100 mV	
AC HF REJ	40 Hz to 50 kHz	20 LSB	100 mV	AC or DC HF REJ does not trigger on 50 MHz sine waves with amplitude of 64 LSB internal or 0.15 V external.
DC	DC to 50 MHz	20 LSB	100 mV	
	50 MHz to 100 MHz	44 LSB	100 mV	
DC HF REJ	DC to 50 kHz	20 LSB	100 mV	
LEVEL Range, 1 kHz sine-wave input				
Internal	At least −128 to +127 LSB.			
EXT	At least −1.28 V to +1.27 V.			
External Trigger Input				
Maximum input				40 volts peak (1/2 watt max).
Input R and C				50 ohms, less than 5 pF.
A AND B MEMORIES				
Size				2048 eight-bit words per channel.
Format				May be partitioned into: 1 record of 2048 words, 2 records of 1024 words, 4 records of 512 words, 8 records of 256 words. (Each record requires a separate trigger.)

[2]The procedure for verifying this characteristic requires special equipment and/or software. As such, it is not checked in the Performance Check Procedure given in the 7612D Service Manual. The characteristic can be checked at any designated Tektronix field service center.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristics	Performance Requirements	Supplemental Information
EXTERNAL CONNECTORS		
Connectors 1,2,3, and 4 Front-to-Rear Feed Through		Connect respective front- and rear-panel connectors via 50-ohm coaxial cables. 50-ohms characteristic impedance ±2%.
POWER SUPPLY		
Input Line Voltage Range		
115 Volts Nominal	90 to 132 V ac.	Selected by rear-panel Line Selector assembly.
230 Volts Nominal	180 to 250 V ac.	
Line Frequency	48 to 440 Hz.	Does not normally require customer verification. Satisfactory operation verified at the factory.
Power Consumption maximum (including plug-in units	400 watts, 5 A at 60 Hz, 115 V ac line (fused at 8 A, fast-blow).	
Remote Control		
Actuate	Requires TTL low level (<0.8V) applied between center conductor and outer conductor to turn power supply on.	
Enable	Provide TTL low level (<0.8V) between center and outer conductor approximately 150 milliseconds after power up. Maximum sink current is 16 mA.	
IEEE 488 INTERFACE		
Data Connector	Conforms to IEEE Standard 488-1975.	
Signal Levels		Conforms to IEEE 488-1975.
Signal Timing		Conforms to IEEE 488-1975.
Data Transfer Rate Maximum		710 kilobytes/sec.
Waveform Transfer Time Minimum		8.35 ms for one 2048-point record, assuming no controller rate-reduction.
X-Y-Z Analog Display Output of Waveform Data		Eight-bit resolution.
X and Y	1 volt peak-to-peak 100 kilohms or greater; adjustable from 0.75 to 1.3 volts.	±3% into
Z	Zero volts blanked, 1 volt unblanked into 100 kilohms or greater. Blanked between data points. Z out, X and Y 50 ohms, ±5%.	

TABLE 1-3
Electrical Characteristics of 7612D System

Plug-in Amplifier	Performance Feature	Minimum Deflection Factor	Bandwidth	Rise Time (Calculated)	Relative Accuracy[1]
7A11	Low-capacitance FET probe built-in	5 mV/div	90 MHz[2]	4.4 ns[2]	2%
7A13	Differential input; dc offset	1 mV/div	65 MHz	6.0 ns	1.5%
7A16A	1-megohm input	5 mV/div	90 MHz[2]	4.4 ns[2]	2%
7A16P	Programmable 50-ohm input	10 mV/div	80 MHz[2]	4.4 ns[2]	2%
7A18	Dual-channel, 1-megohm input	5 mV/div	65 MHz[2]	6.0 ns[2]	2%
7A19	Wide bandwidth 50-ohm input	10 mV/div	90 MHz[2]	4.4 ns[2]	3%
7A22	Differential input	10 V/div	1 MHz ±10%	350 ns ±9%	2%
7A24	Dual-channel, bandwidth 50-ohm input	5 mV/div	90 MHz[2]	4.4 ns[2]	2%
7A26	Dual-channel 1-megohm input	5 mV/div	90 MHz[2]	4.4 ns[2]	2%
7A29	Dual channel, wide bandwidth	10 mV/div	90 MHz[2]	4.4 ns[2]	2%

[1]**Applies to all deflection factors when the plug-in gain is set at the deflection factor designated on each plug-in. The calibration signal must be supplied by an external calibrator whose accuracy is within 0.25%.**

[2]**+20° to +30° C only. 80 MHz bandwidth, 5.0 ns risetime from 0° to +40° C.**

TABLE 1-4
Environmental Characteristics

Characteristics	Description
Temperature	
Operating	0° to +40° C.
Nonoperating	-62° to +85° C.
Cooling	
Thermal Output	1,400 BTUs/hour, maximum.
Airflow Required	120 cubic feet/min at +20° C at sea level.
Humidity, Operating	Up to 95%, relative.
Altitude	
Operating	-6 to +4,570 meters (-250 to +15,000 feet).
Nonoperating	-76 to +15,200 meters (-250 to +50,000 feet).

TABLE 1-5
Physical Characteristics

Characteristics	Description
Size	Fits standard 19" rack. Figure 1-5 illustrates the outside dimensions of the 7612D.
Net Weight	24.95 Kg (55 lbs).

ACCESSORIES

The following accessories are supplied with the 7612D:

1 ea ..... Operators Manual
1 ea ..... Service Manual
1 ea ..... Detachable Power Cord, 2.4 meters (8 feet)
1 ea ..... Rack Slides with hardware
1 ea ..... IEEE 488 bus cable, 2 meters (6.6 feet)

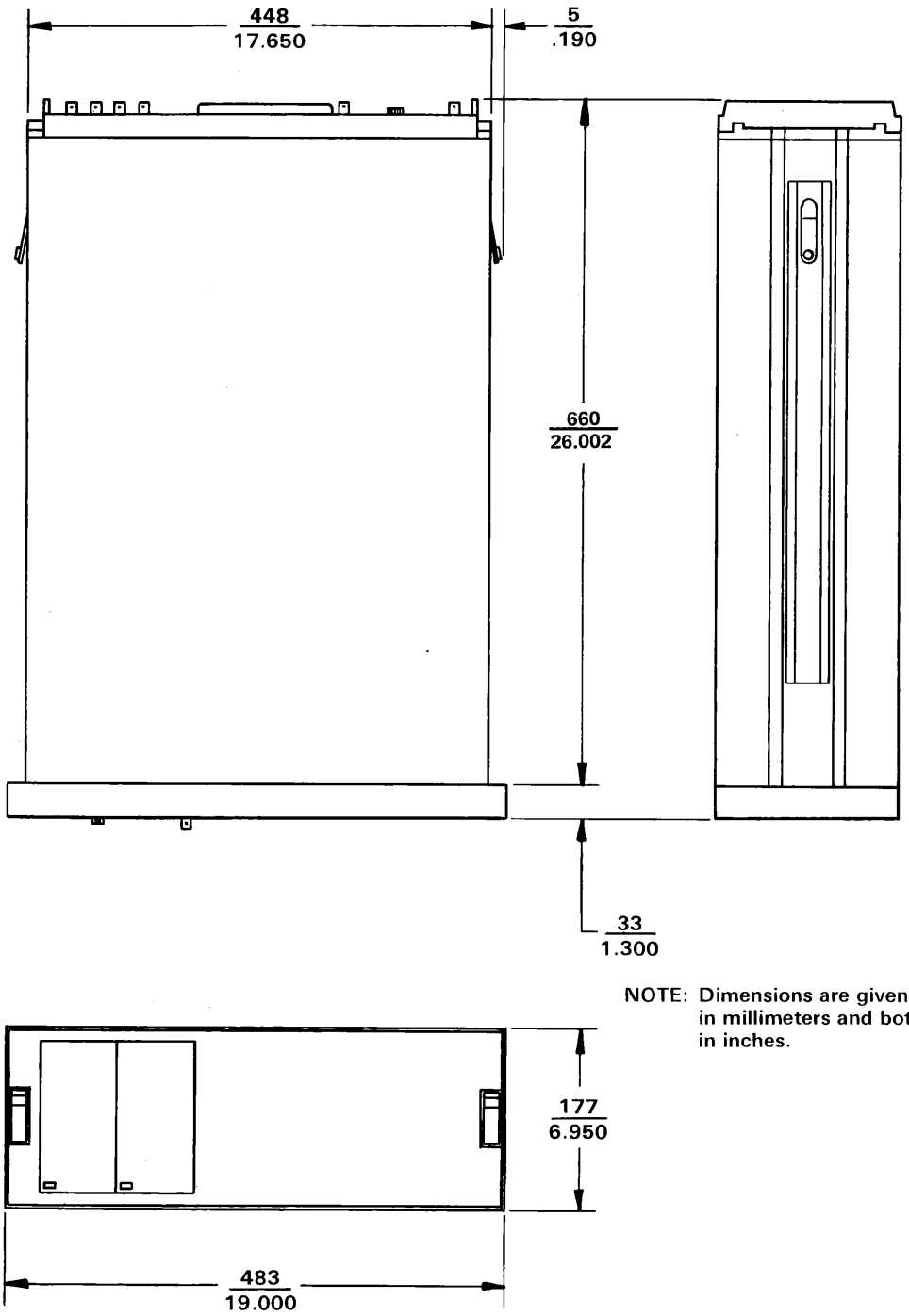


Figure 1-5. Dimensions of 7612D.

OPERATING AND PROGRAMMING

This section describes the 7612D controls and connectors, provides detailed instructions for local (front-panel) operation of the 7612D, and gives detailed information about programming the 7612D. The programming part has five subparts. The first subpart is an introduction to the IEEE 488 bus. The second subpart discusses the IEEE 488 interface functions implemented in the 7612D. The third subpart describes remote-control messages, with emphasis on the command set. The fourth subpart tells of instrument status, warning messages and error messages. The fifth and final subpart gives programming examples.

OPERATING

The 7612D is based on the Tektronix 7000-series plug-in concept. The plug-in units have their own controls; see their Operators manuals for descriptions of these controls and for instructions about operating the plug-in units. Although some of the plug-in controls are referenced in this manual, they are not fully described, nor are full operating instructions given here.

CONTROLS, CONNECTORS AND INDICATORS

FRONT PANEL

The 7612D front-panel controls, connectors, and indicators are divided into four main groups:

1. Instrument Function
2. Time Base and Trigger Control
3. Trigger Functions
4. Connectors

The front-panel functions are color-coded to simplify front-panel operation; instrument control functions are in the gray and yellow shaded areas, trigger functions are shaded in green, and time-base functions are shaded in blue.

Instrument Function

Figure 2-1 shows the instrument control section of the front-panel. The numbers in the following descriptions correspond to those used in Figure 2-1.

1. **ON/OFF.** Turns the 7612D power on or off if the rear-panel PRINCIPAL POWER SWITCH is on. The rear-panel ACTUATE connector overrides the ON/OFF switch. ON/OFF lights when the instrument is on.

2. **CHANNEL A.** Selects the A channel to be programmed by subsequent time-base and trigger-function entries. Also causes the current settings for channel A to be displayed on the front panel.

3. **CHANNEL B.** Selects the B channel to be programmed by subsequent time-base and trigger-function entries. Also causes the current settings of channel B to be displayed on the front panel.

4. **COPY.** Copies the settings from the selected time base to the other time base. If, for example, time base A is selected (CHANNEL A button lit), pressing the COPY button will copy all settings from time-base A to time-base B. If time-base B is selected, pressing the COPY button will copy the time base settings of time-base B into time-base A.

5. **ARM A.** Arms the A time base. If any changes were made to the time-base A settings since the last arm operation, the validity of the settings is first verified. If any errors are found during verification, a warning message is displayed in the RECORD LENGTH indicators. When the ARM operation is complete, the time base becomes triggerable.

6. **ARM B.** Arms the B time base. If any changes were made to the time-base B settings since the last arm operation, the validity of the settings is first verified. If any errors are found during verification, a warning message is displayed in the SAMPLES indicators. When the ARM operation is complete, the time base becomes triggerable.

7. **B TRIG AFTER A.** Sets the 7612D to B TRIGgerable AFTER A mode. In this mode, time-base B becomes triggerable after the first record of A is acquired. If only time-base B is armed, it will not trigger until A is armed and has acquired one record of data. MAN TRIG will not trigger time-base B until this condition is satisified.

8. **CLK.** Selects the internal or external clock as the clock source for both channels. When set for INTernal, the button lights and the SAMPLE INTERVAL function selects a sample period in seconds. When set to EXTernal, the SAMPLE INTERVAL function selects a period multiplier for the externally supplied clock signal.

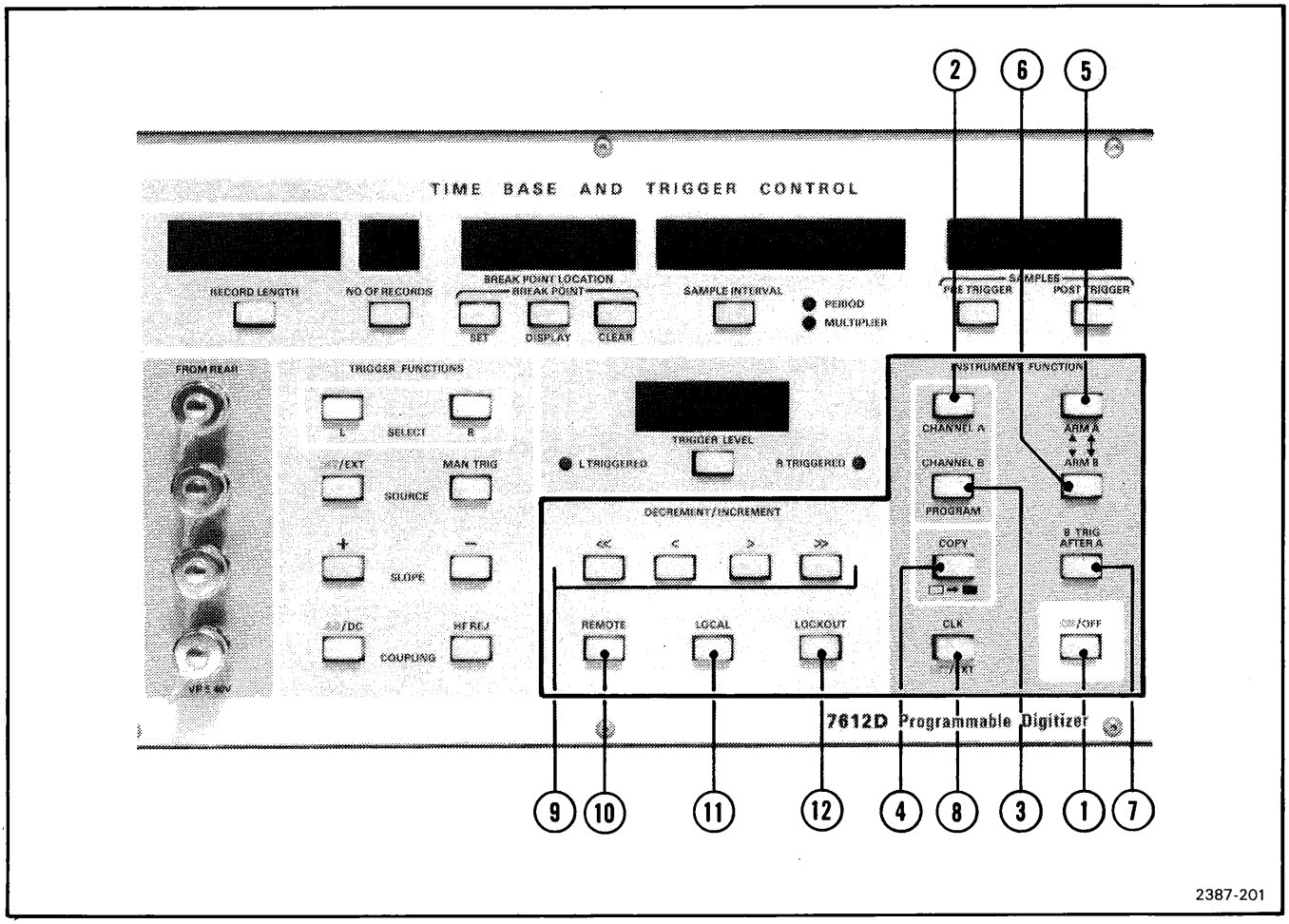


Figure 2-1. Functions of front-panel instrument controls.

9. **DECREMENT/INCREMENT.** Allows the user to decrement or increment the current value for a selected time base or trigger parameter. The value is decremented or incremented only through valid values, and it does not "wrap around"; when the value reaches its upper or lower limit, it stops decrementing or incrementing.

   For example, to set a new record length, the user presses RECORD LENGTH. This selects the record length parameter so that it can be modified with the DECREMENT/INCREMENT buttons. The value can be cycled through all of the settings that are valid for the current state of the instrument. When any button other than DECREMENT/INCREMENT, ON/OFF, or LOCAL is pressed, the new value is entered. If the instrument goes to remote state before another button is pressed, the previously selected value is automatically entered.

   The << and >> buttons cause the value to be decremented or incremented at a faster rate than the < and > buttons.

10. **REMOTE.** Lights to indicate when the 7612D is set to remote state by the IEEE 488 bus system controller. When REMOTE is pressed and the system controller has enabled the Remote Request function (REM ON command), the 7612D requests service from the controller and reports remote request status.

11. **LOCAL.** Returns the 7612D from remote state to local state unless the system controller has set the instrument to remote with lockout state. Lights when in local state.

12. **LOCKOUT.** Lights to indicate that the 7612D is in local with lockout state or remote with lockout state.

When pressed, the LOCKOUT button causes the instrument primary and secondary IEEE 488 bus addresses to be displayed in the RECORD LENGTH and SAMPLES indicators, respectively.

The normal front-panel display can be restored by pressing any button except ON/OFF or LOCAL.

Time Base and Trigger Control

Figure 2-2 shows the time base control section of the front-panel. These buttons program the time bases for memory partitioning, sample intervals, and pre- and post-trigger modes. The numbers in the following description correspond to those used in Figure 2-2.

13. **RECORD LENGTH.** When pressed, the length of the record(s) for the selected time base can be set with the DECREMENT/INCREMENT buttons. Lights when selected.

    The display shows the length of the record(s) for the currently selected time base.

14. **NO OF RECORDS.** When pressed, the number of records for the selected time base can be set with the DECREMENT/INCREMENT buttons. Lights when selected.

    The indicator displays the number of records for the currently selected time base.

15. **SET.** When pressed, a new breakpoint location can be set with the DECREMENT/INCREMENT buttons. The breakpoint is set in all records in the selected time base.

16. **DISPLAY.** Causes the existing breakpoint(s) and the corresponding sample interval(s) to be displayed. The DECREMENT/INCREMENT buttons allow the user to cycle through all the existing breakpoints. The DISPLAY function also selects the breakpoint to be cleared with the CLEAR button. Breakpoints can be cleared only after they are DISPLAYed. Breakpoints can be displayed and cleared from the front panel in local state, but they can be displayed only in remote state.

17. **CLEAR.** Clears the breakpoint displayed on the BREAKPOINT LOCATION display. The sample interval from the preceding breakpoint is applied to all samples up to the next breakpoint. The breakpoint is cleared in all record(s) in the selected time base. Breakpoints must be selected with the display function before they can be cleared.

    The display indicates the location (sample number) of the breakpoint currently being set, examined, or cleared. The CLEAR function is disabled in remote state.

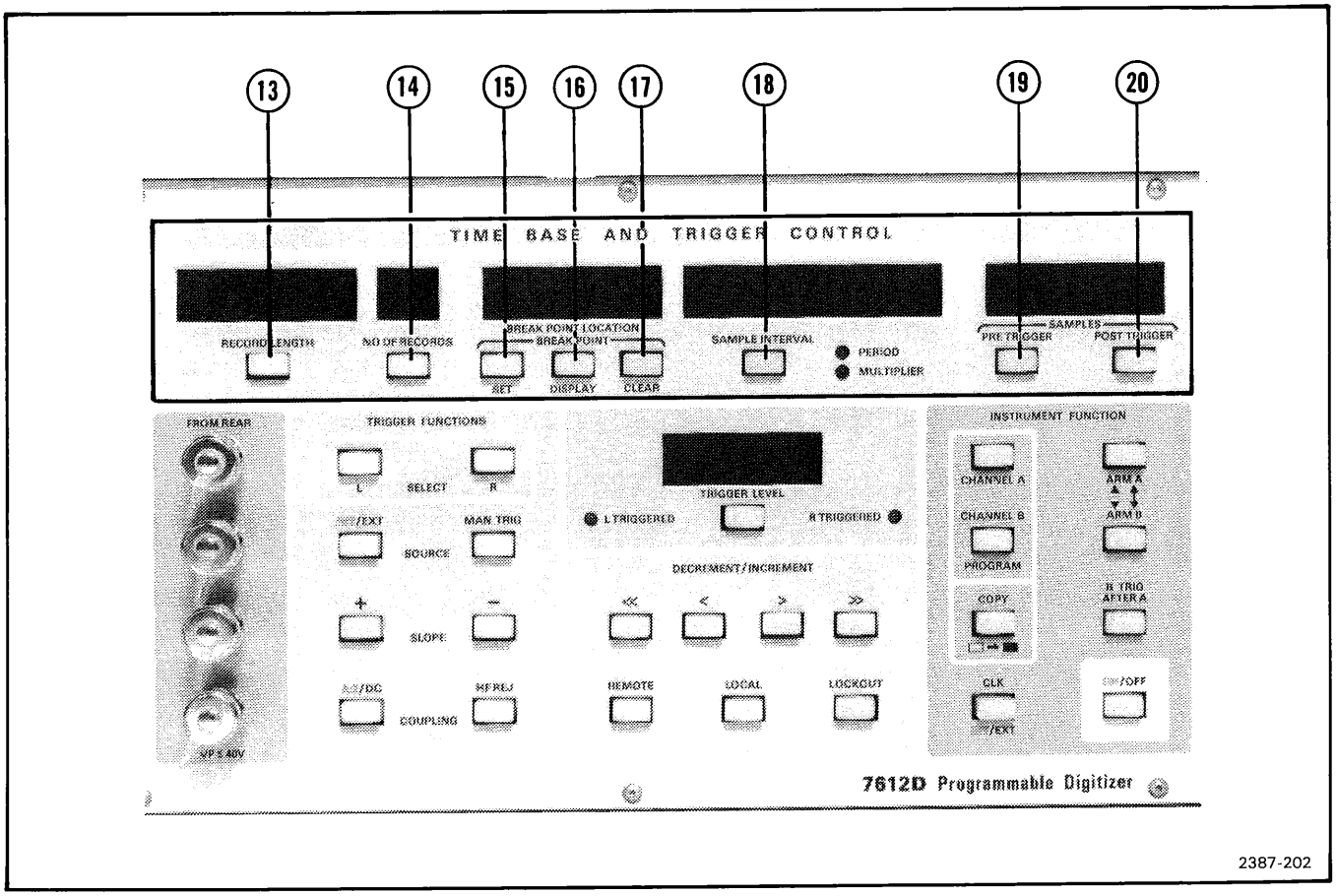


Figure 2-2. Functions of front-panel time-base controls.

18. **SAMPLE INTERVAL.** Sets the sample interval or external clock period multiplier for all samples after the displayed breakpoint and up to the next breakpoint (or the end of the record).

    The display indicates the sample interval or external clock period multiplier for all samples from the selected breakpoint to the next breakpoint or the end of the record, whichever comes first.

    The PERIOD indicator lights when the internal clock is selected and the value shown in the SAMPLE INTERVAL display is the period in seconds. MULTIPLIER Lights when the external clock input is selected, and the value in the SAMPLE INTERVAL display is the external clock period multiplier.

19. **PRE TRIGGER.** When pressed, the number of pre-trigger samples to be stored for the selected time base can be set with the DECREMENT/INCREMENT buttons. The range of values is from zero to 16 less than the number of samples in the first segment.

20. **POST TRIGGER.** When pressed, the DECREMENT/ INCREMENT buttons set the number of samples after the trigger that are ignored before the instrument begins storing data. Allowable post-trigger values range from eight to the record length. When POST TRIGGER mode is selected, only one record may be selected for that channel. If more than one record is selected, the instrument reports a warning error and sets the number of records to one.

Trigger Functions

The trigger control functions program the trigger level, source, slope, and coupling parameters. Figure 2-3 shows the trigger controls.

21. **TRIGGER LEVEL.** When pressed, the trigger level for the currently selected trigger channel can be set by the DECREMENT/ INCREMENT buttons. The display indicates the trigger level value for the currently selected trigger channel.

22. **L AND R TRIGGERED.** Lights to indicate that the corresponding trigger channel has received a valid trigger.

23. **SELECT L.** Selects the left trigger channel for programming by subsequent trigger function entries. Also causes the left trigger channel to be used as the trigger source for the time base currently being programmed. The trigger level for the left channel is displayed in the TRIG LEVEL indicators.

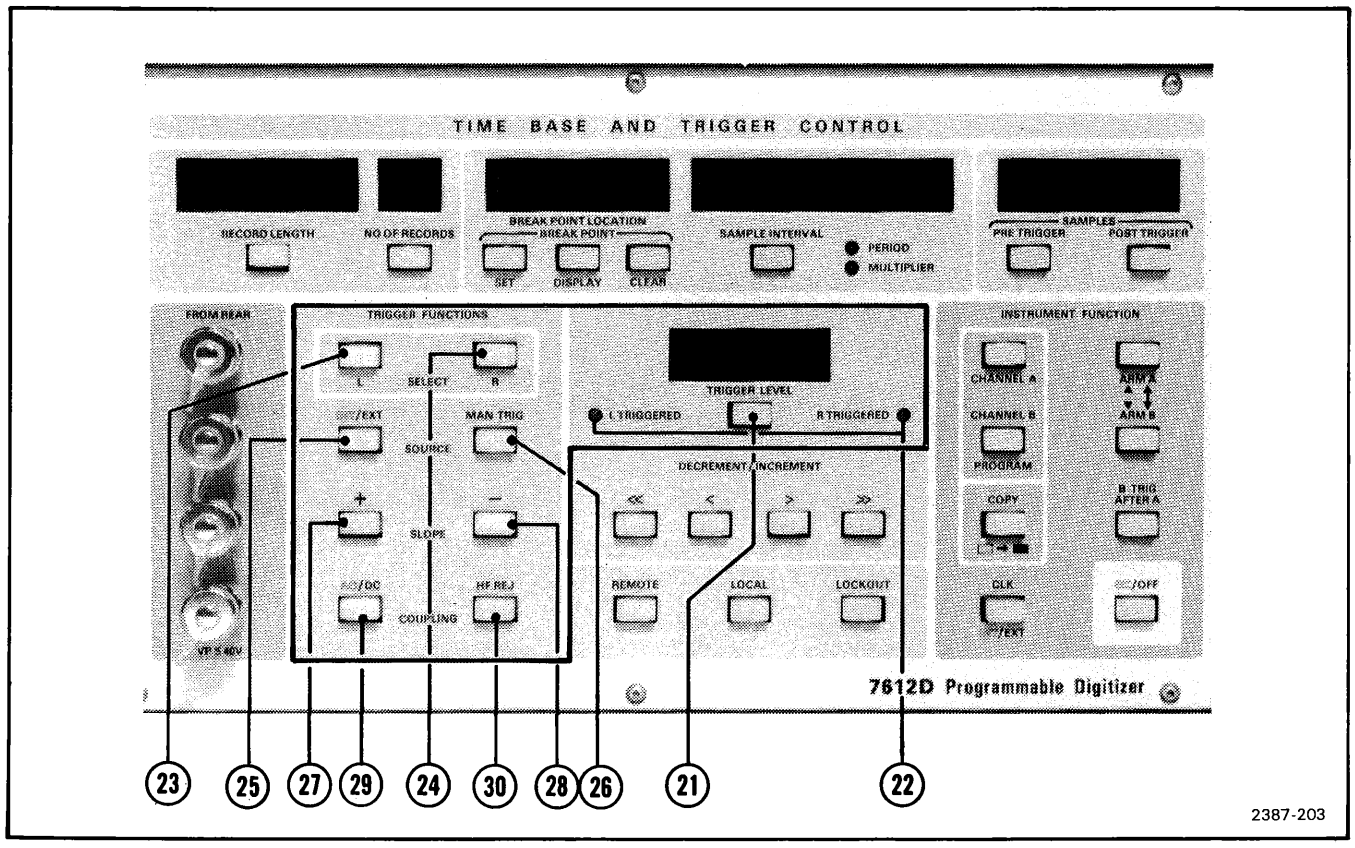


Figure 2-3. Functions of front-panel trigger controls.

24. **SELECT R.** Selects the right trigger channel for programming by subsequent trigger function entries. Also causes the right trigger channel to be used as the trigger source for the time base currently being programmed. The trigger level for the right channel is displayed in the TRIGGER LEVEL Indicators.

25. **INT/EXT SOURCE.** Selects internal or external source for the trigger signal. Lights when INTernal is selected.

26. **MAN TRIG SOURCE.** Causes the currently armed channel(s) to trigger if the input signal is not out of range. If the signal is out of range (off the top or bottom of the EBS target), the MAN TRIG will not trigger the time base(s). MAN TRIG does not affect the trigger function settings. One record of data is acquired for each MAN TRIG. If multiple records are selected, one MAN TRIG per record is required to manually complete acquisition.

27. + **SLOPE.** Sets the selected trigger channel to trigger on the positive slope of the waveform. Lights when selected.

28. − **SLOPE.** Sets the selected trigger channel to trigger on the negative slope of the waveform. Lights when selected.

29. **AC/DC COUPLING.** Selects ac or dc coupling of the triggering signal. Lights when ac is selected.

30. **HF REJ.** When selected, trigger signal frequencies above about 50 kHz are attenuated. Lights when selected.

Connectors

The four front-panel bnc connectors provide straight-through connection to the corresponding rear-panel connectors via 50 Ω cables.

REAR PANEL

The rear-panel controls and connectors are shown in Figure 2-4. The numbers in the following descriptions refer to the figure.

1. Connectors 1, 2, 3, 4

Rear-panel connectors 1, 2, 3, and 4 provide straight-through connection to front-panel connectors 1, 2, 3 and 4, respectively.

2. L Trig (Left External Trigger)

Input connector for the left channel external trigger signal. Terminated in 50 Ω.

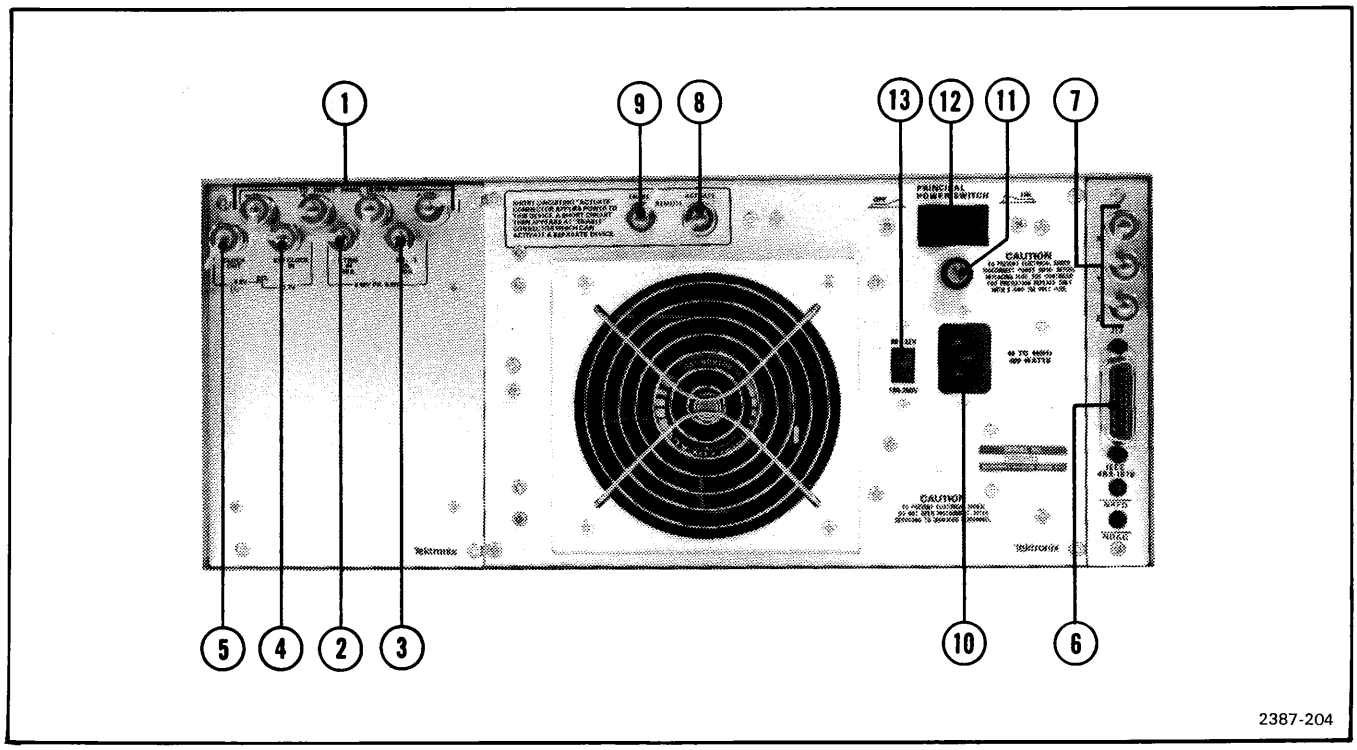


Figure 2-4. Rear-panel connectors and switches.

3. R Trig (Right External Trigger)

Input connector for the right channel external trigger signal. Terminated in 50 Ω.

4. EXT CLK In

An ECL-level external clock signal applied to this connector drives the A and B time bases when external clock is selected.

5. CLK Out

The ECL-level internal clock signal is available at this connector. This output is active in external or internal clock modes.

6. IEEE 488-1975

Provides connection to the bus specifed in IEEE Standard 488-1975.

7. X,Y,Z

Provides X-Y-Z analog equivalents of the waveform data stored in memory for display on a suitable XYZ monitor. (Refer to section 1 for XYZ output specifications.)

8. Actuate

A TTL low applied between the center and outer conductors turns the 7612D power supply on. When the signal goes high, the power supply turns off.

9. Enable

Applies a TTL low between center and outer conductors shortly after the instrument is powered-up. This allows the power control of the 7612D to be daisy-chained with similar instruments in a system.

10. Power Connector

CAE-22 three-prong power connector; IEC coded.

11. Fuse

Replaceable fuse for ac line power.

12. Principal Power Switch

Power line switch that controls line input power to the 7612D power supply.

13. Line Voltage Selector

Selects 115 V ac or 230 V ac operation.

OPERATING THE 7612D

INTRODUCTION

Before operating the 7612D, check the environmental and physical specifications at the end of Section 1; the operating temperature and airflow requirements of the instrument must be met. Be sure nothing is blocking the fan intake (screen on rear panel) or the air exhaust holes on the sides of the instrument.

PLUG-IN UNITS

The 7612D accepts two Tektronix 7000-series plug-in amplifiers. These can be selected to tailor bandwidth, input impedance, and other characteristics of the 7612D to your application. See the specifications in Section 1 for recommended plug-in units and their performance in the 7612D.

When selecting probes, match the probe impedance to the input impedance of the amplifier.

CAUTION

Always turn off the 7612D power before removing or installing plug-in units to prevent damage to the circuitry.

Install amplifier plug-in units in both plug-in compartments. Programmable or nonprogrammable plug-ins may be used in any combination.

XYZ DISPLAY

An XYZ monitor connected to the rear-panel XYZ outputs provides a convenient method of visually setting up the instrument. The 7612D automatically displays the contents of both data memories after each acquisition. During acquisition and while the microprocessor is busy executing commands from the front-panel or IEEE 488 bus, the display refresh is disabled. This may cause some normal display flicker during the execution of front panel or IEEE 488 commands. No scale factor readout is displayed on the XYZ monitor.

The XYZ display has two parts. The upper part displays the contents of channel A and the lower part displays channel B.

APPLYING POWER

The 7612D power cord must be connected to an outlet with a securely grounded protective-ground contact and the correct single-phase voltage. Instructions for connecting power to the instrument are given in Section 4.

For either the front-panel ON/OFF switch or the rear-panel ACTUATE connector to power-up the instrument, the PRINCIPAL POWER SWITCH must be turned on.

WARNING

To avoid electric shock, be sure that the protective ground circuit is not interrupted. A poor or missing ground circuit can allow the chassis to float to hazardous potentials. Be sure that the power cord, plug, and outlet provide a secure path to earth (ground) for the protective ground circuit of the 7612D.

Press the ON/OFF button or apply a TTL active low on the ACTUATE connector. The button should light and the fan should start. The microprocessor performs a self-test at power-up that requires about three seconds to complete. If the test fails, the microprocessor displays an error message on the front panel that indicates the fault (unless the fault is in the hardware required to display the message).

When the test is completed, the front-panel indicators and buttons come up in their default states. The EBS tubes require about 30 seconds to warm up before data can be reliably acquired.

THE ACQUISITION PROGRAM

An acquisition sequence or "program" stored in the 7612D for each time base controls data acquisition. These programs consist of the number of records, length of record(s), breakpoint locations, sampling intervals and trigger parameters for each channel. At power-up, the settings for both time bases are:

NO OF RECORDS 1
RECORD LENGTH 2048
BREAK POINT LOCATION . 0
SAMPLE INTERVAL . . . . . 5 ns
TRIGGER MODE . . . . . Pre-Trigger (0 samples)

The default acquisition program can be modified from the front panel in local state or over the IEEE 488 bus in remote state. At power-up, the PROGRAM CHANNEL A button lights to indicate that any changes in the time base parameters will affect the A time base. Pressing CHANNEL B causes subsequent time base entries to modify the program for channel B.

The power-up state also lights SELECT L, indicating that the left trigger channel has been assigned to time base A. The trigger for time base A will be derived from the settings in the left trigger channel. Any modifications to the trigger parameters will affect the left trigger channel. Pressing SELECT R will assign the right trigger channel to the currently selected time base and cause subsequent trigger function entries to modify the right trigger channel parameters. The left trigger channel gets its internal trigger signal from the left plug-in. The right trigger channel gets its internal trigger signal from the right plug-in. The power-up settings for both trigger channels are:

SOURCE . . . . . Internal
SLOPE . . . . . Positive
COUPLING . . . . . AC
HF REJ . . . . . Off
LEVEL 0

ARMING THE TIME BASE

The 7612D time bases must be armed before they can be triggered to start an acquisition. Figure 2-5 shows a simplified flow chart of the Arm operation.

If any of the time base settings have been modified since the last arming, the first step is to check the validity of the new settings. Conflicts, such as breakpoints set beyond the record length, are corrected with record length having the highest priority (the record length is never changed to resolve a conflict in the settings). If conflicts are found, warning messages that describe the conflict and how the settings are modified to resolve it are reported on the front panel and over the IEEE 488 bus.

The second step in the process is also performed only when the time base settings have been modified. In this step, the settings are loaded from the acquisition program into the time-base hardware. The time required to perform these first two steps varies slightly with different time base settings, but a typical verify and load process takes about 50 ms.

The next step is to initialize the hardware for acquisition. This step takes about 300 μs, and is performed at each Arm whether the time base settings are changed or not.

If the time base is set to PRE TRIGGER Mode, one full record of pre-trigger data is acquired before the time base becomes triggerable. The time required for this acquisition can be calculated by multiplying the number of samples in the record (record length) times the sample interval for the first segment. All pre-trigger samples are acquired at the sampling interval of the first segment. This pre-trigger acquisition is repeated before each record when multiple records are selected.

When the pre-trigger acquisition is complete, the time base becomes triggerable. The next valid trigger initiates acquisition. If POST TRIGGER mode is selected, the pre-trigger acquisition step is skipped.

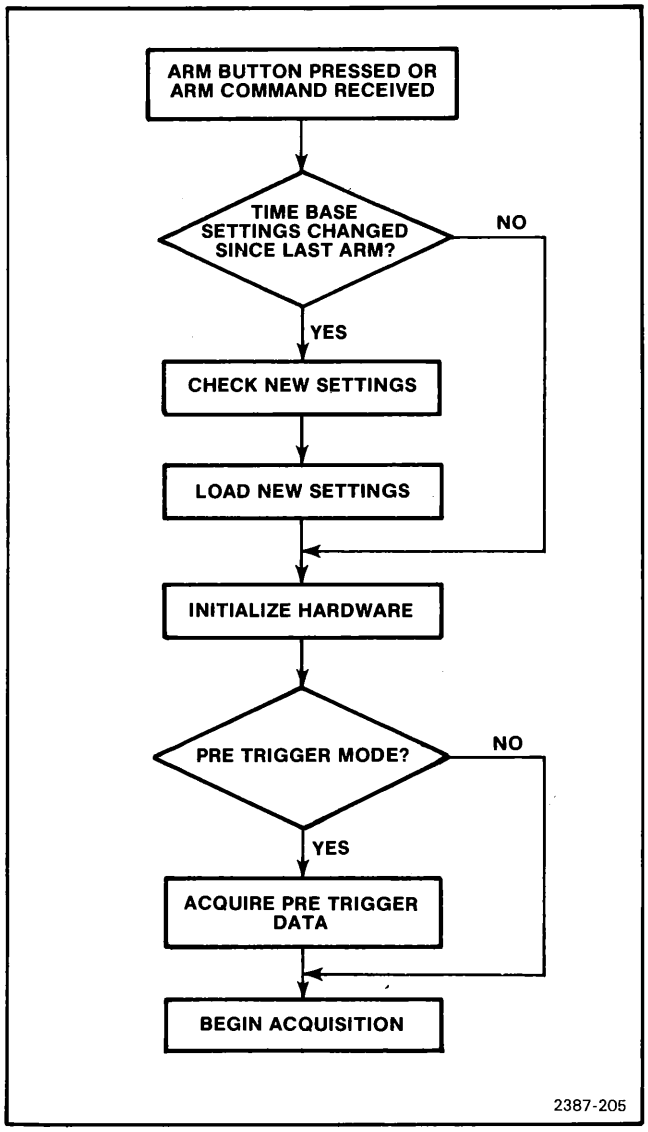


Figure 2-5. Flow chart of the Arm process.

ACQUIRING A BASE LINE

1. Check that a compatible XYZ monitor is connected to the 7612D. For instructions on connecting the monitor, see Section 4.

2. Power up the 7612D and allow it to warm up for a few minutes.

3. Turn on the monitor and set it for normal intensity.

4. Ground the inputs of both amplifier plug-in units.

5. Press ARM A and ARM B simultaneously. The ARM buttons should light, indicating that the instrument is armed and triggerable.

6. Press MAN TRIG to trigger the time bases. The instrument acquires one record of 2048 samples for each channel. Two flat lines should appear on the XYZ monitor and the ARM buttons should go out.

7. If the base lines do not appear, check the connections and adjustments of the monitor. Then re-arm the time bases and press MAN TRIG again.

8. If the lines still do not appear, check the Position controls on the plug-in units, and repeat the previous steps.

SETTING THE TRIGGERING FUNCTIONS

The 7612D has two independent trigger channels. Triggering parameters such as level, slope, source, and coupling can be individually programmed. The trigger channels receive analog trigger signals from the plug-in units, an external source, or the MANual TRIGger switch on the front panel. If the programmed trigger conditions are met, the trigger circuits generate digital trigger signals for the time bases.

Each time base can be programmed to use either trigger channel as a trigger signal source. At power-up, Time Base A is set to receive its trigger from the left trigger channel, and Time Base B is set to receive its trigger from the right channel. The user may change these assignments by pressing the SELECT Left or Right buttons while setting up the instrument. The selected trigger channel is assigned to the time base currently being programmed, and all subsequent trigger function entries modify that channel's parameters.

All of the trigger functions except LEVEL are selected by pressing a single button as indicated on the front panel. The trigger level is set by pressing TRIGGER LEVEL and decrementing or incrementing the value with the DECREMENT/INCREMENT buttons. The selected value does not take effect until another button is pressed, or the instrument goes to remote state. If the trigger channel is receiving a valid trigger, the corresponding L or R TRIGGERED light comes on.

At this point, a brief review of the trigger functions may be helpful. The following discussion describes each trigger function and its use.

Source

The source button selects the internal (signal from the plug-ins) or external trigger signal as the trigger source. In most applications, the internal signal from the plug-in units provides an acceptable trigger source. The pre- and post-trigger modes can be used to vary the time relationship be-

tween the trigger and the acquired signal. The external source can be used where external synchronization is needed.

The external trigger signal is applied to the rear-panel L or R TRIG connectors. These connectors may be looped through from the front panel with a short 50 Ω coaxial cable from the TRIG connectors to the number 3 and 4 connectors on the rear panel. This allows the external trigger to be applied to the corresponding front-panel connectors.

Coupling

The COUPLING button selects ac or dc coupling of the trigger signal. When ac coupling is selected (the power-up default), any dc level on the signal is ignored and frequencies below about 30 Hz are attenuated. In general, ac coupling can be used for most applications. However, if the time base is to be triggered on a low-frequency signal or dc level, dc coupling may provide better triggering.

DC coupling provides more stable triggering on low-frequency signals. Remember that the plug-in Position control affects the trigger level with dc coupling.

HF REJ

When HF REJ (High Frequency REJect) is on (button lit), trigger signal frequencies above about 50 kHz are attenuated. This provides a means of filtering complex or noisy signals to provide more stable triggering.

Slope

The SLOPE buttons determine whether the trigger occurs on the positive or negative slope of the trigger signal. The exact level at which the trigger occurs is set by the LEVEL parameter.

Trigger Level

The TRIGGER LEVEL parameter sets the amplitude level on the trigger signal at which the trigger occurs. The level ranges from +127 to −128, corresponding to the eight-bit resolution of the instrument (256 discrete levels). The point of triggering will depend on the method of coupling the trigger signal. If the trigger signal is dc coupled and the TRIGGER LEVEL is set to +127, a trigger will occur when the signal reaches the top of the EBS tube target area. If the trigger signal is ac coupled and the TRIGGER LEVEL is set to +127, a trigger will occur when the input is 127 levels greater than the average level of this signal. A setting of 0 means that the trigger occurs when the signal crosses through zero. If the SLOPE is set to +, the time base triggers when the trigger signal passes through the selected level on the positive slope of the signal. If SLOPE is set to −, the time base triggers at the selected level on the negative slope of the signal.

SETTING UP A SIMPLE ACQUISITION PROGRAM

Now let's set up a simple acquisition program to acquire four 512-point records of a sine wave in channel A. For a repetitive input signal such as a sine wave, all records will be identical (they will start at the same trigger point).

1. Install plug-in units and power-up the instrument as discussed in previous steps.

2. Set the plug-in amplifier Volts/Div control to 0.5 volts/division.

3. Connect a sine-wave generator to the channel A amplifier input and adjust the generator controls for about four volts peak-to-peak output amplitude at 1.5 kHz.

4. Press CHANNEL A to program time base A. (The acquisition could just as easily be set up for time base B by pressing CHANNEL B and performing the following steps. We use channel A as an example).

5. Press RECORD LENGTH. The button lights to indicate that the function has been selected and can be cycled through valid values with the DECREMENT/INCREMENT buttons.

6. Press and hold the < or << buttons until the value in the record length display is 512.

7. Press NO OF RECORDS and increment the value to 4. Notice that the number of records will not increment past 4, because four 512-point records fill the entire data memory (2048 points).

8. Press SAMPLE INTERVAL and increment the value to 1 μs (1E-6). For this example, we will acquire the entire record at this sampling interval, so no breakpoints are needed.

9. Check that the trigger functions are set as follows:

   SOURCE . . . . . Internal
   SLOPE . . . . . Positive (+)
   COUPLING . . . . . AC
   HF REJ . . . . . Off

10. Check that the L TRIGGERED light is on. If not, adjust the trigger level by pressing the TRIGGER LEVEL button. Increment or decrement the value and press the TRIGGER LEVEL again to load the new level. (Pressing any button except DECREMENT/INCREMENT, ON/OFF, or LOCAL loads the new value.) Repeat this procedure until the L TRIGGERED indicator lights and stays on.

11. Recheck the settings made in the preceding steps. The settings can be changed in any order as long as the resulting settings do not conflict. If they do conflict

(e.g., setting the record length to 2048 when four records are set up), the instrument modifies the settings (with record length as highest priority) to resolve the conflict. (In the case of setting the record length to 2048, the number of records will be set to one.)

12. Press ARM A. The instrument checks the validity of the settings and, if errors are found, a warning or error message is displayed on the front panel. Otherwise, the channel becomes triggerable. On the next valid trigger, the instrument acquires the first 512-point record at a 1 μs sampling interval. Then it waits for another trigger. When the next trigger occurs, it acquires a second 512-point record, and so on until all four records are acquired.

13. The XYZ monitor will display four identical waveforms, as shown in Figure 2-6. Notice that all waveforms start at the same trigger point. All four records are displayed successively on one line, starting with record zero.

14. If the display is clipped on the top or bottom of the waveform, adjust the plug-in Position control or decrease the output amplitude of the generator as required. Press ARM to acquire and display the new data. Repeat this step until the display is similar to Figure 2-6.

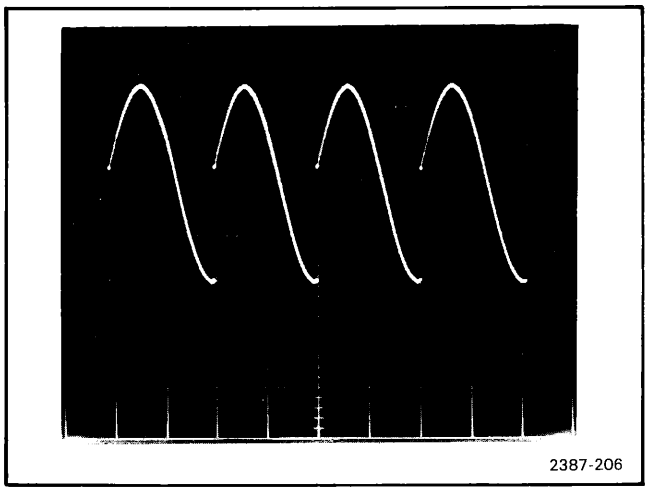


Figure 2-6. XYZ monitor display of four 512-point records of a 1.5 kHz sine wave.

SETTING BREAKPOINTS

In many situations, a small part of a waveform is of particular interest (e.g., the rising edge of a fast pulse), but the remainder of the waveform also contains useful information. Sampling at a high rate to provide good time resolution during the rising edge of the pulse produces a large amount of unnecessary data during the slower parts of the waveform (e.g., the flat top of a pulse). The 7612D provides a simple means of changing the sampling interval during an acquisition to expand the important part(s) of a waveform, while recording the remainder at a lower sampling interval.

For example, if we want to measure the rise time and width of a square-wave pulse, the fast rising edge could be sampled at a 50 nanosecond rate. When the pulse has reached maximum amplitude, the sampling interval might be increased to 1 μs to acquire the slower part of the waveform.

A sampling interval change is marked by a **breakpoint** set with the front-panel BREAKPOINT buttons in local state or with the SBPT (Set BreakPoinT) command in remote state. Three front-panel buttons are provided to set, display, or clear breakpoints. Breakpoints can be set at any integer multiple of eight samples from 16 to eight less than the record length. Remember that all records are identical, so breakpoints apply to all records in the selected channel.

Breakpoints divide the records into **segments**. A segment contains all the samples from the specified breakpoint to the next breakpoint (or the end of the record). One breakpoint at sample zero defines the first segment (segment 0). This breakpoint is always present and cannot be cleared.

The following example illustrates the use of breakpoints and sample interval switching to measure the rise time or pulse width of a long pulse. To reproduce the example, a square-wave generator with a controlled rise time of about 0.1 μs is required (such as the TEKTRONIX FG 504 40 MHz Function Generator).

1. Connect the square-wave generator to the inputs of both plug-in amplifiers with a bnc T connector. Set their Volts/Div controls to 0.5 and adjust the generator for about three volts peak-to-peak output.

2. Set the generator frequency to 600 Hz.

3. Press PROGRAM CHANNEL B.

4. Press RECORD LENGTH and set the value to 2048 with the DECREMENT/INCREMENT buttons.

5. Press NO OF RECORDS. The number of records changes to one automatically (if it was not already set to one) because one 2048-point record fills the waveform memory.

6. Set the sampling interval for the first segment to 1 μs by pressing the SAMPLE INTERVAL button and incrementing the value to 1E-6.

7. Press COPY. This copies the current settings of channel B into channel A. The result is a single record in channel A of 2048 points with no breakpoints and a sampling interval of 1 μs. This will provide a comparison for the waveform acquired with breakpoints in channel B.

8. Now set the breakpoints in channel B. Press SET BREAKPOINT. Increment the value in the BREAKPOINT LOCATION display to 856. Note that the display cycles through multiples of eight samples. If you pass the value, simply decrement back to it with the < or << buttons. The value will not increment beyond 2040, because this is the last multiple of eight which is less than the current record length (2048).

9. Next, set the sample interval for the segment you just defined by pressing SAMPLE INTERVAL. Increment or decrement the value to 50 ns (50E-9).

10. Set another breakpoint at sample number 944 using the procedure given in step 6.

11. Set the sampling interval for this segment to 1 μs, using the procedure described in step 7.

12. Set another breakpoint at sample number 1800 and set the sampling interval for this segment to 50 ns.

13. Finally, set a breakpoint at sample number 1976 and set the sampling interval for the last segment to 1 μs.

14. Before arming the instrument, check the breakpoint locations and sampling intervals with the DISPLAY BREAKPOINT button.

15. Press DISPLAY. The last breakpoint set and its associated sampling interval will be displayed in the BREAKPOINT LOCATION and SAMPLE INTERVAL indicators, respectively.

16. Press the < key twice more to display the next two lower breakpoints and sample intervals. Pressing < again displays the fixed breakpoint at location zero and the sampling interval for the first segment. Figure 2-7 illustrates the memory segments as set in the above steps.

17. If you want to change one of the breakpoints, DISPLAY the desired location, then press CLEAR. The breakpoint is cleared and the sample interval from the preceeding breakpoint is applied to all samples up to the next breakpoint (or the end of the record, if the last breakpoint is cleared). Then, set the new breakpoint as described in step 6.

18. When you are satisfied that the settings are correct, press ARM A and ARM B simultaneously. The instrument checks the validity of the settings and reports any warning or error messages on the front panel.

19. If the trigger conditions are satisfied, the instrument begins acquiring data in both channels. If either channel does not trigger, check the trigger settings and re-ARM both channels.

The display on the XYZ monitor should be similar to Figure 2-8 for channel A. It may not appear the same for channel B if the rise and fall of the square wave do not fall within the narrow segments that are sampled at 50 ns. By carefully adjusting the generator frequency (or moving the breakpoints) and repeatedly arming channel B, you should find a point where the rise and fall are within these windows and the display is similar to Figure 2-8 (this process may be tedious). In practice, a computer can acquire the waveform and calculate the exact breakpoint locations and sampling intervals for best results.

When the leading and trailing edges of the pulse are expanded with breakpoints, an accurate measurement of rise and fall times and pulse width can be made in a single acquisition. All sampling intervals are derived from the highly stable 200 MHz internal clock, and the sample interval switching is coherent (the last sample of a segment is the time origin of the following segment) at all sampling intervals except 5 ns. As a result, time measurements of long periods can be made with 10 ns resolution (worst case).

USING THE COPY BUTTON

In some cases it may be desirable to set up the same or similar acquisition programs in both 7612D channels. The

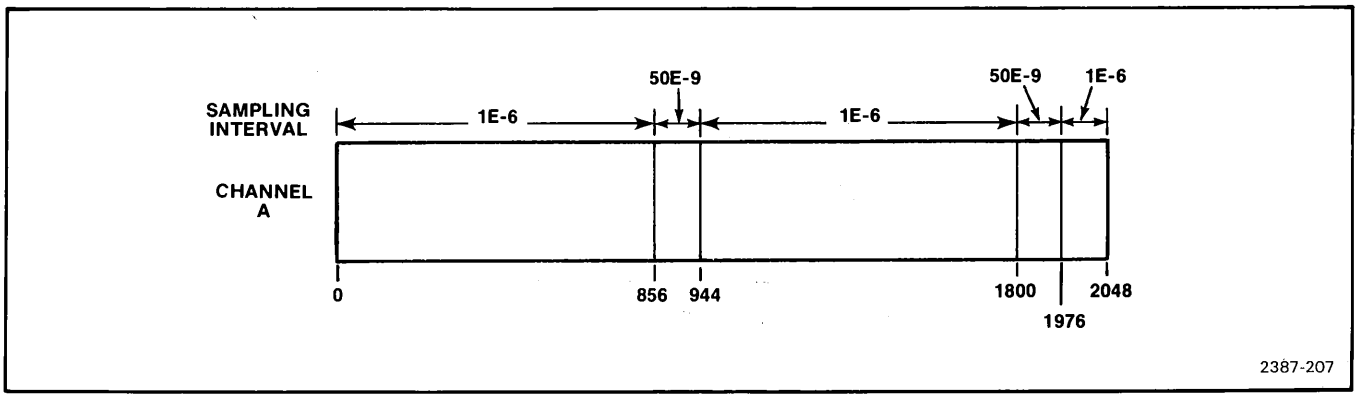


Figure 2-7. Memory segmenting for the breakpoints set in the example procedure.

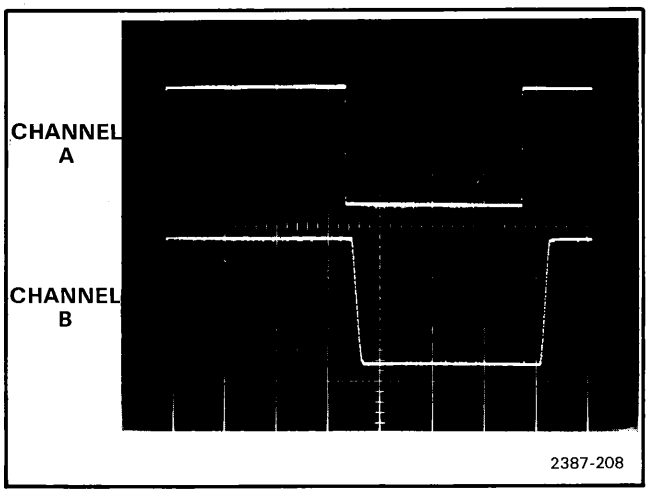


Figure 2-8. XYZ monitor display for the breakpoint example.

COPY button provides a simple means of copying all the time-base settings from one channel to the other. When the COPY button is pressed, the settings of the selected channel are copied to the unselected channel. All previous settings in the unselected channel are lost. If, for example, you wish to copy the settings of channel A to channel B, select channel A by pressing CHANNEL A. Then press COPY. The instrument control functions (e.g., CLK, B TRIG AFTER A, etc.) are unaffected by a COPY.

PRE-TRIGGER MODE

It is frequently necessary to acquire part of a signal that occurs before the trigger event. For example, the leading edge of a transient pulse may be used to trigger an acquisition. To capture the full leading edge, some samples must be stored just before the trigger occurs. The Pre-Trigger mode causes the 7612D to store a programmed number of samples before the trigger event.

To visualize the pre-trigger process, think of a record of 7612D data memory as a pipeline, as shown in Figure 2-9. Data is acquired and stored in the waveform memory, entering the pipeline from the right. As the acquisition progresses, new data entering from the right pushes the previous data toward the left end of the pipeline.

In Pre-Trigger mode, the 7612D begins acquiring pre-trigger data when the time base is armed. Triggers are ignored during this period. Pre-trigger data is acquired at the sampling interval selected for the first segment and stored in the waveform memory "pipeline." When a full record of pre-trigger data has been acquired, the time base becomes triggerable, but pre-trigger data acquisition continues until a trigger is received. The new pre-trigger data entering the pipeline forces old data out at the other end. (New data actually over-writes old data in the data memory; the pipeline is only a convenient analogy.)

Data is continuously acquired and circulated through the pipeline until a trigger occurs. Then, data is acquired for each of the segments in the record at the selected sampling interval. This data enters the pipeline, pushing the pre-trigger data to the left. The acquisition stops when the selected number of pre-trigger samples and the samples acquired after the trigger fill the record as shown in the figure.

This process is repeated for each record in the channel.

The pre-trigger value is set with the front-panel PRE TRIGGER button or with the MODE PRE command in remote state. The range of valid values is from zero to 16 less than the first segment (or the record length when no breakpoints are set). All pre-trigger data is acquired at the sample interval of the first segment.

1. To select the pre-trigger mode from the front panel, press PRE TRIGGER and increment the value with the DECREMENT/INCREMENT buttons to the desired set-

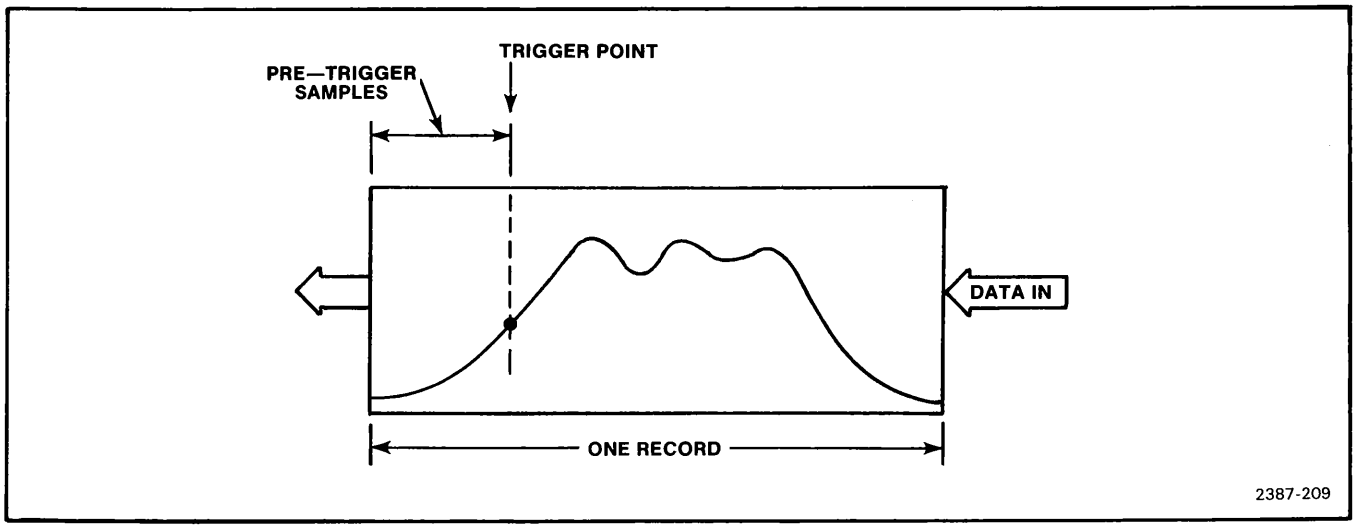


Figure 2-9. Illustrating the Pre-Trigger mode as a pipeline.

ting (the power-up default value is zero samples). Note that the value cannot be incremented beyond 16 less than the length of the first segment (or the record length).

2. ARM the selected time base. Remember that the instrument acquires one full record of data at the interval programmed for the first segment before becoming triggerable. Any triggers that occur during this hold-off period are ignored.

3. The waveform displayed on the XYZ monitor will be shifted to the right by the programmed number of pre-trigger samples. The selected number of samples are stored before the trigger event.

POST-TRIGGER MODE

If the signal of interest occurs significantly after the trigger event, post-trigger mode can be used to delay the start of acquisition from the trigger. In this mode, a programmed number of samples is ignored before data storage begins. (These samples serve only as a delay timer; they do not occupy space in data memory.) Figure 2-10 illustrates a waveform acquired with post-trigger mode. Post-trigger can be implemented only when the number of records is set to one. Selecting post-trigger mode with more than one record generates a warning message on the front panel and sets the number of records to one. The range of valid values is from eight to the record length.

1. To select post-trigger mode, be sure that the number of records is set to 1.

2. Press POST TRIGGER and increment the value in the SAMPLES display to the desired value. The value cannot be incremented beyond the record length.

3. Arm the selected time base. The instrument begins storing data after it is triggered and the programmed number of samples have been taken.

The effects of pre- and post-trigger modes can be illustrated by feeding identical signals to the vertical inputs of both channels, and programming the time bases with identical settings (use the COPY button). Then, set time-base B to pre-trigger mode. The number of samples selected is not important, as long as it is large enough to make a visible difference between the channel A and channel B data. Arm both time bases and compare the XYZ displays. The channel B data will begin at the programmed number of samples before channel A, as shown in Figure 2-11.

Repeat this procedure, setting channel B for post-trigger mode. Be sure the time bases are set for one record. The acquired waveform from channel B will appear delayed by the programmed number of samples from channel A data.

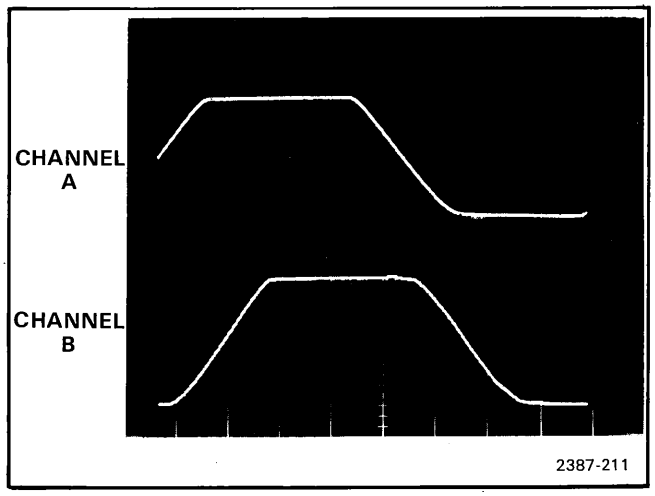


Figure 2-11. The effects of Pre-Trigger mode on an XYZ display. The top trace (channel A) is set to pre-trigger zero samples, and the bottom trace (channel B) is set to pre-trigger 128 samples.

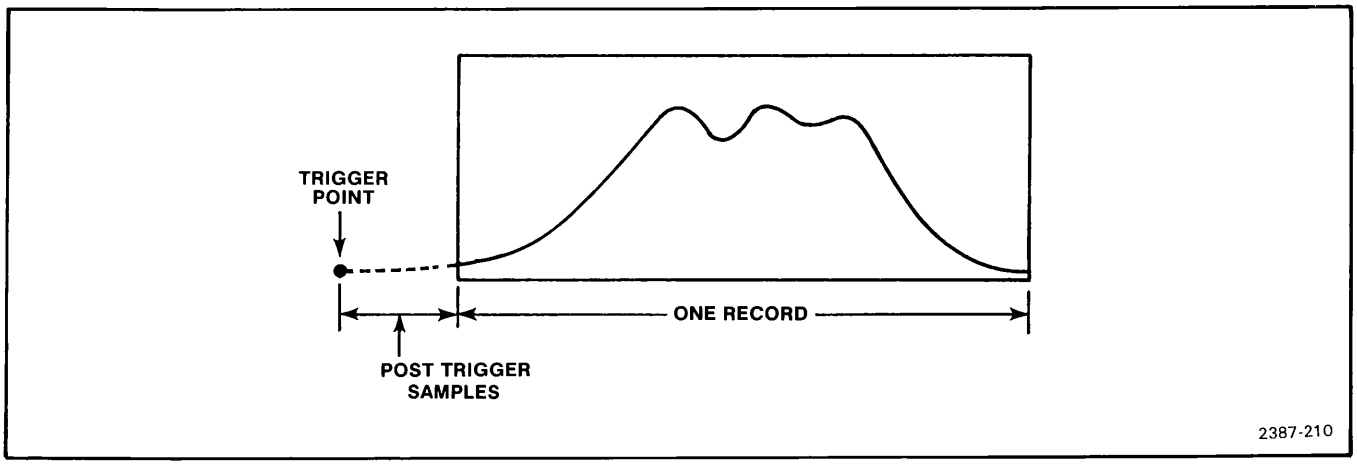


Figure 2-10. The effects of using Post-Trigger mode.

B TRIGGERABLE AFTER A MODE

This mode provides a means of inhibiting channel B trigger until the first record of channel A is acquired. When selected, the B time base becomes triggerable after the first record of A is acquired. The B channel trigger conditions must be satisfied to actually trigger the time base. After the first record, both time bases act independently, requiring a separate trigger for each record, as illustrated in Figure 2-12.

If only channel B is armed with B Triggerable After A mode selected, time base B will not accept a trigger until channel A is armed and has acquired its first complete record. If only channel A is armed, it triggers normally, but channel B does not trigger until armed.

USING AN EXTERNAL CLOCK

An external sampling clock, applied to the rear-panel EXT CLK IN connector, can drive the 7612D time bases. The clock signal must be at ECL levels and conform to the rise- and fall-time specifications given in section 1. The clock source is selected with the front-panel CLK button. When the button is dark, the external clock signal is selected; when the button is lit, the internal clock signal is selected.

The selected clock source applies to both channels; one channel cannot be driven by the internal clock with the other driven by the external clock. When the external clock is selected, the MULTIPLIER indicator (below the SAMPLE INTERVAL display) lights, indicating that the SAMPLE INTERVAL function selects a period multiplier for the external clock signal. If, for example, a 1 MHz (1 μs period) clock is applied, selecting a period multiplier of 1 results in a 1 μs sampling interval. A multiplier of 1000 (1E+3) results in a one millisecond sampling interval. The effective sampling interval is calculated as follows:

SI=(External Clock Period)$\times$(External Clock Period Multiplier)

The external clock input allows the 7612D to synchronously sample a signal with respect to the externally supplied clock. The period of the clock signal need not be consistent. However, the period multiplier simply divides the external clock frequency, so for a period multiplier of 10, a sample is taken on every tenth pulse regardless of the period of the individual pulses.

The external clock-period multiplier is set by pressing the SAMPLE INTERVAL button and decrementing or incrementing to the desired value. The range of valid values is 1 to 200 $\times$ 10^6.

FRONT-PANEL WARNING AND ERROR MESSAGES

The 7612D front panel is controlled by the system's 6800 microprocessor. The microprocessor system makes the front panel "smart" to minimize the possibility for error. Occasionally, however, the user may set a parameter that conflicts with the other previously programmed settings. For example, assume the record length for the time base A is set to 1024 and a breakpoint is set at sample number 656. If the user now decides to change the record length to 512, the breakpoint at 656 is beyond the record length. When the record length is entered, all breakpoints above the record length are deleted and warning message 501 is displayed in the RECORD LENGTH indicators to warn the operator that those breakpoints were deleted.

Tables 2-1 and 2-2 summarize the front-panel warning and error messages. These messages are a subset of the messages sent over the IEEE 488 bus in response to the ERR? query (see Description of Commands, ERR? in this section).

The warning messages in Table 2-1 are generated when the instrument finds a conflict while performing the verification step of the ARM command or when returning from remote state to local state. They indicate unique combinations of four possible conditions. The table shows the combinations and the associated warning messages.

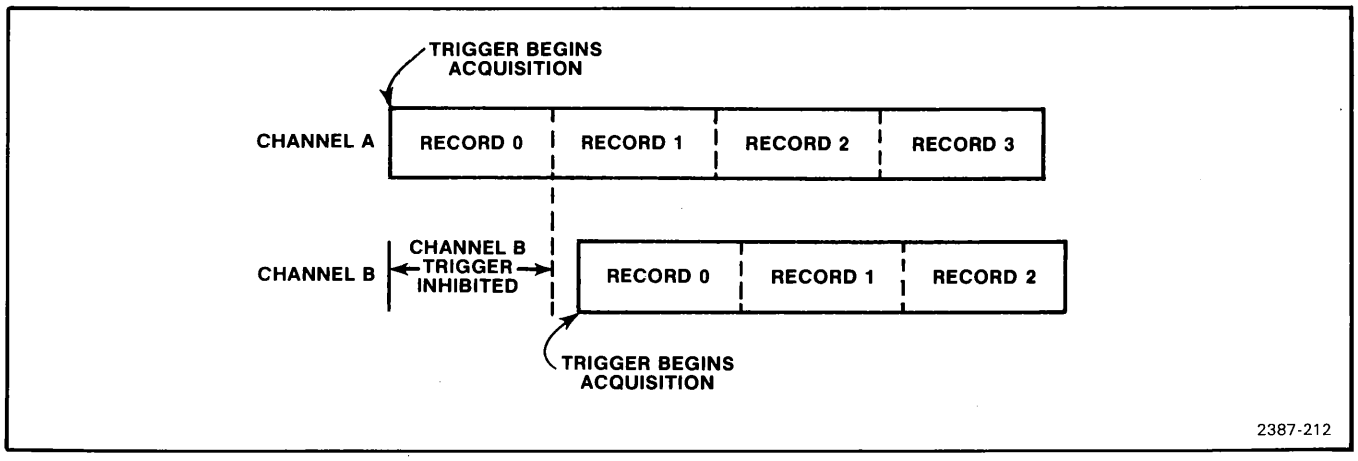


Figure 2-12. The use of B Triggerable After A mode.

TABLE 2-1
Execution Warning Message

CHANNEL A	CHANNEL B	PRE TRIG	POST TRIG	NO. OF REC	BRK PTS
501	511	0	0	0	1
502	512	0	0	1	0
503	513	0	0	1	1
504	514	0	1	0	0
505	515	0	1	0	1
506	516	0	1	1	0
507	517	0	1	1	1
508	518	1	0	0	0
509	519	1	0	0	1

Pre Trig

1 indicates that the number of pre-trigger samples has been set to 16 less than the length of the first segment.

Post Trig

1 indicates that the number of post-trigger samples has been set to the record length.

NO OF REC

1 indicates that the number of records has been set to one because the channel is in post-trigger mode.

BRK PTS

1 indicates that all breakpoints greater than or equal to the record length were deleted.

NOTE

Error messages reported in the front-panel RECORD LENGTH and SAMPLES displays do not affect the normal values for these parameters. The front panel returns to its normal state when any button (except ON/OFF or LOCAL) is pressed.

The internal error and warning messages are displayed if the instrument detects an error during self-tests. Table 2-2 summarizes these messages. Error 601 is a warning error only; the instrument remains functional, but the problem should be investigated and remedied as soon as possible. The other messages are disastrous errors. In some cases, the instrument may be incapable of displaying the error message because the error occurred in the hardware used to display the message. In any case, the problem should be referred to a qualified service person.

TABLE 2-2
Internal Error Messages

MESSAGE NUMBER	DESCRIPTION
301	ROM found at wrong address.
302	RAM failed self-test.
303	Interrupt fault.
304	Check-sum error in ROM found.
305	Data transmitter failed to begin or complete in allotted time.
601*	Instrument failed to trigger properly in power-up test.

***This is a warning message only.**

LOCAL CONTROL IN AN IEEE 488 SYSTEM

When the 7612D is interfaced to an IEEE 488 system there are special considerations for local operation. Some pointers are given here for operation under these circumstances.

The 7612D goes to local state automatically at power-up. All local operating controls are active and the LOCAL button lights. An IEEE 488 bus controller can then set the instrument to remote state. In remote state, front-panel controls that do not affect the state of the instrument or data memory are enabled. For example, DISPLAY BREAKPOINT functions in local or remote states, but the ARM buttons are disabled when in remote state. The ON/OFF, LOCAL, and REMOTE buttons are active and the REMOTE button lights. Local control can be restored by pressing LOCAL.

To prevent local control, the IEEE 488 bus controller can set the 7612D to remote with lockout state. The instrument operates exactly as it does in remote state, except that pressing LOCAL does not restore local control. In this state, the REMOTE and LOCKOUT buttons light. More detailed information on the LOCKOUT state is provided in the programming part of this section.

The instrument may also be set to local with lockout state. To the operator, the instrument responds the same as in the local state. The LOCAL and LOCKOUT buttons light.

When the 7612D returns from remote to local control, the instrument performs a validity check of the current settings and reports any errors on the front panel. The validity check is identical to the one performed when a time base is armed. Therefore, when returning from remote to local, be sure the settings are valid.

The instrument returns to local state with the settings left from the remote state. No settings are changed unless conflicts are found in the validity check.

ACQUIRING DATA

The 7612D is a waveform digitizing instrument. Because it samples the analog input at discrete time intervals, the output data is a collection of values that represent the amplitudes of the input signal at the sampling points. Keeping this fact in mind, and observing a few simple rules when setting up the instrument, will ensure that the digitized data accurately represents the analog input signal.

Selecting a Sampling Interval

It is important to remember that the digitized data is simply a series of numbers stored in waveform memory—not the actual signal. These numbers represent the signal amplitudes at discrete sample points. One value is stored for each sample at the sampling rate programmed for the current segment. Figure 2-13 shows an input waveform and illustrates the digitized data that results.

It is clear that the more samples taken of the input waveform, the more accurately the output data represents the analog signal. A simple example is the input waveform shown in Figure 2-14. Here the analog input signal is a slowly varying signal with a fast noise spike. If the sample interval is considerably longer than the width of the noise spike, the spike may occur between two samples and be completely lost in the digitized data. Decreasing the sampling interval (increasing the sampling frequency) slightly may cause one or two samples to be taken during the spike, but to accurately determine its amplitude and width may require many samples (a very short sampling interval). If the spike is repetitive, a breakpoint can be set to shorten the sampling interval for the duration of the pulse.

Another less obvious problem caused by sampling at too slow a rate is called aliasing. Figure 2-15 illustrates a simple case of aliasing. The input signal is a 20 kHz sine wave. Part b of Figure 2-15 shows the digitized data that results from sampling the sine wave at 200 ns intervals. At this rate, there are approximately 250 samples per cycle of the input signal. This is more than enough data to accurately reconstruct the input signal.

If the sampling interval is increased to exactly match the period of the input waveform (50 μs), the straight line output data would represent a straight line, because all the samples would be taken at the same point on the sine wave. In practice, it is very difficult to match the period and phase of the input signal. Part c of Figure 2-15 shows the case where the sampling interval is slightly longer than the period of the input waveform. Here, the output data represents a sine wave, but not at the original input frequency. Instead, it is a sine wave of the same amplitude as the original, but with a much longer period time. This effect is called aliasing, and it can occur with any input waveform (though it is more difficult to detect with nonsinusoidal waveforms).

We cannot cover the details of the effect here, but it is essential that the user be aware of the problems with insufficient sampling. A general rule to follow is that the input waveform should be sampled at least twice per period. In other words, the sample interval should be no longer than one half of the period of the input waveform. Of course, the higher the sampling rate, the more accurately the output data will represent the analog signal.

Overrange Data

Full-scale vertical deflection for the 7612D corresponds to eight divisions as specified for the vertical amplifier plug-in. For example, a four-volt input signal produces full-scale deflection when the amplifier is set for 0.5 Volts/Division. The XYZ monitor screen displays the data for both channels by displaying channel A data in the top half of the screen and channel B data in the bottom half. As a result, the display amplitude is half the normal amplitude. A six-division signal, for example, produces a three-division display on the monitor.

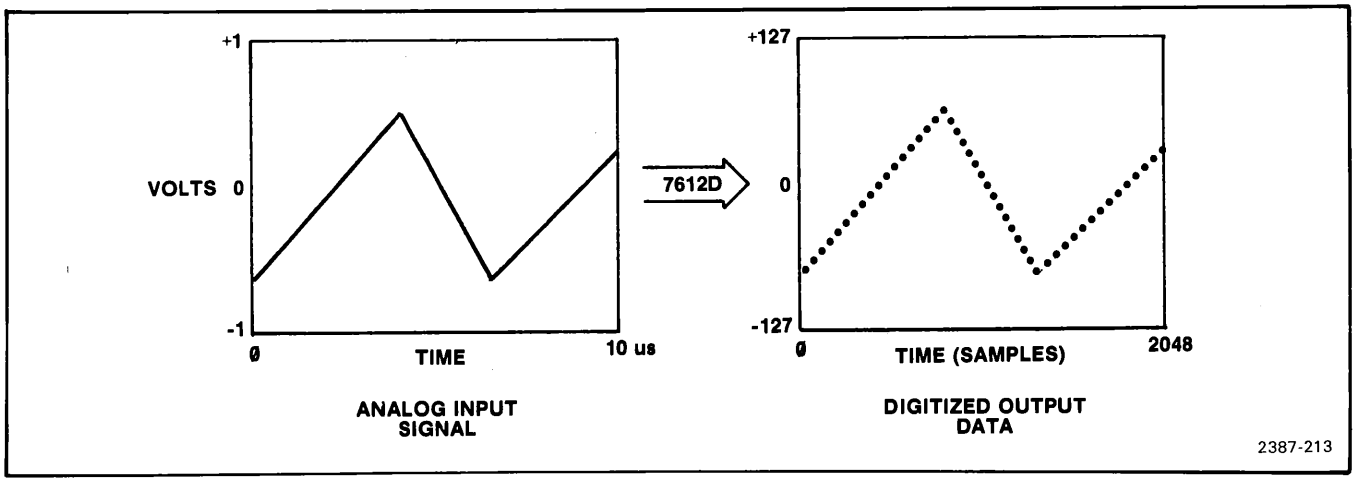


Figure 2-13. An analog input signal and the resultant digitized data.

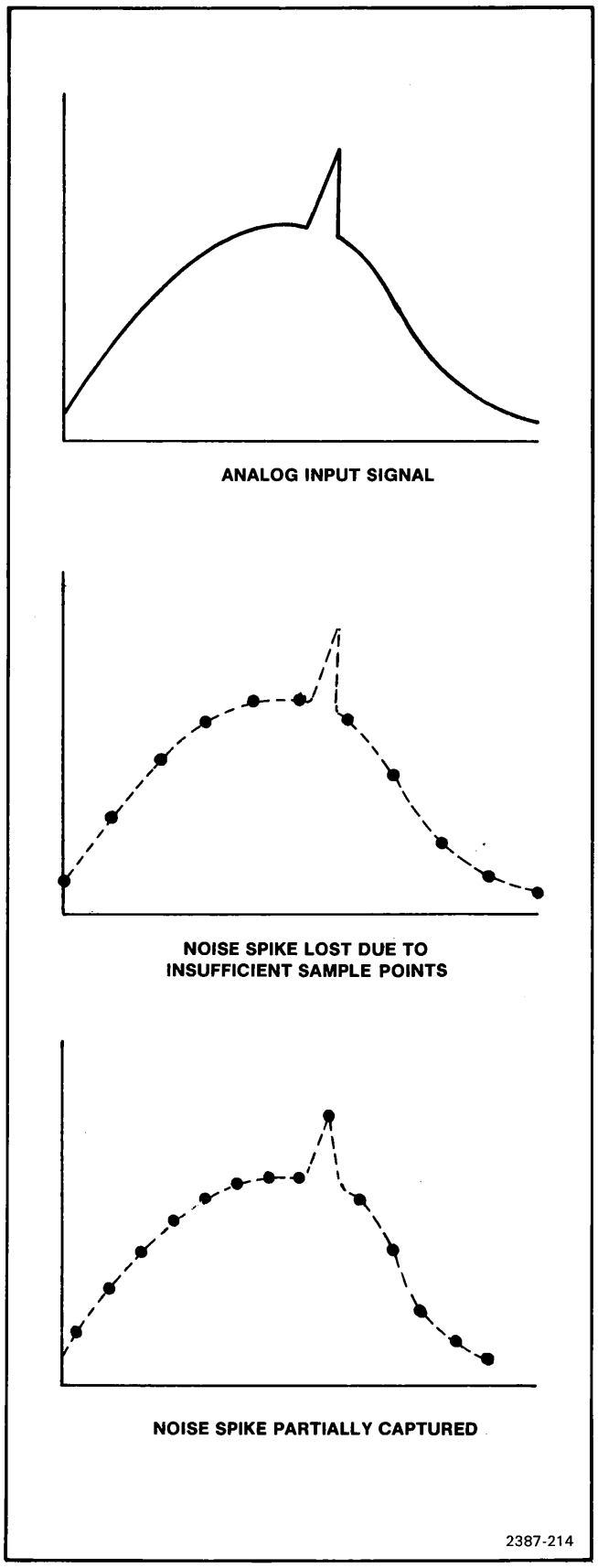


Figure 2-14. The effects of insufficient sampling.

Input signals that are beyond the full scale range of the instrument cause the data byte stored in waveform memory to be set to all 1's for positive overrange and all 0's for negative overrange. These bytes are blanked on the XYZ monitor. As a result, parts of the input waveform that are positioned off the target area appear to be missing on the XYZ display (see Fig. 2-16). An internal jumper can be set to display overrange data at the positive and negative limits of the XYZ display range. In this mode, overrange data appears to be clipped on the display. The data stored in the 7612D data memory is not affected.

Refer to section 4 for instructions on setting this jumper.

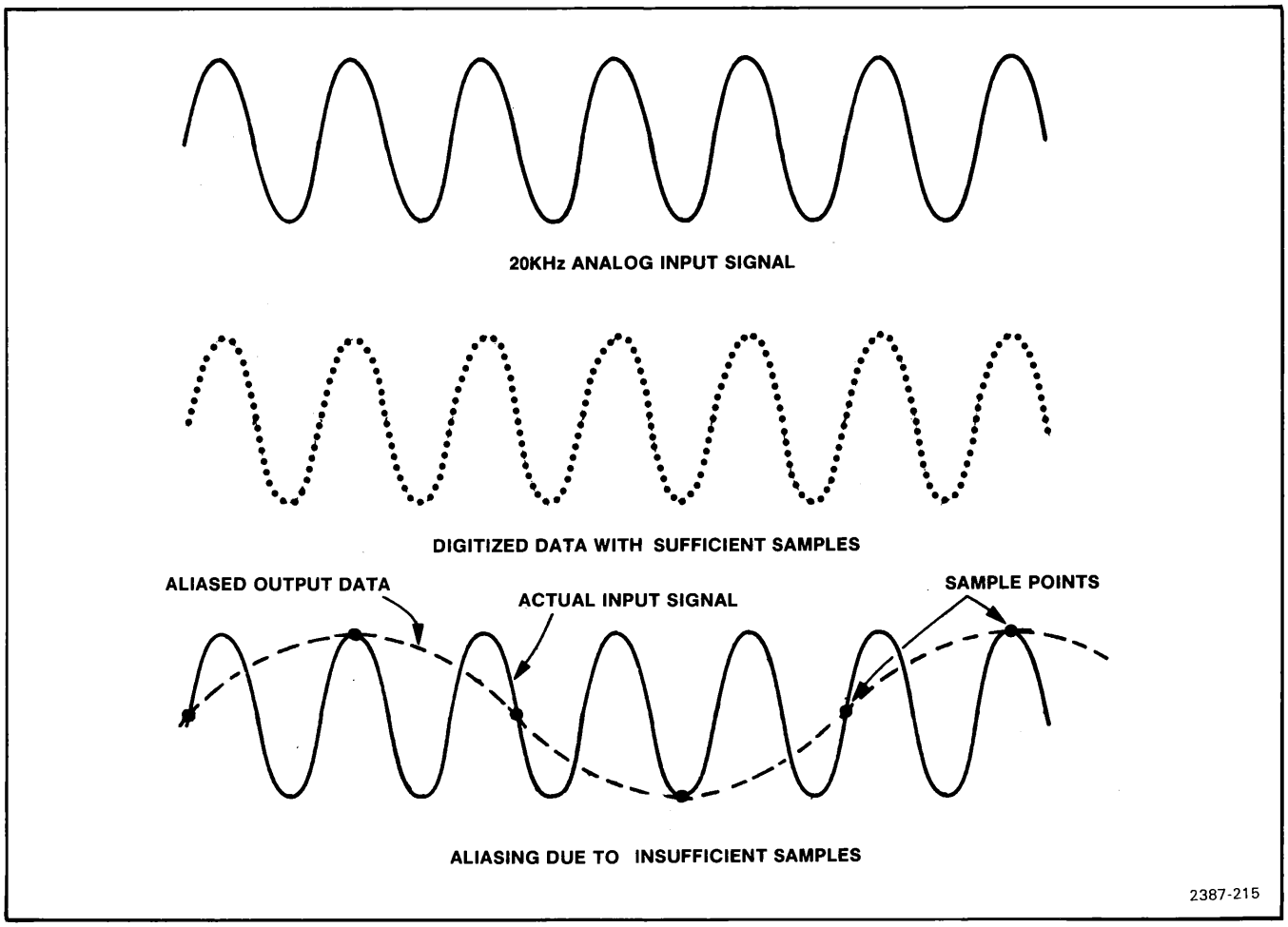


Figure 2-15. Aliasing in the digitized data.

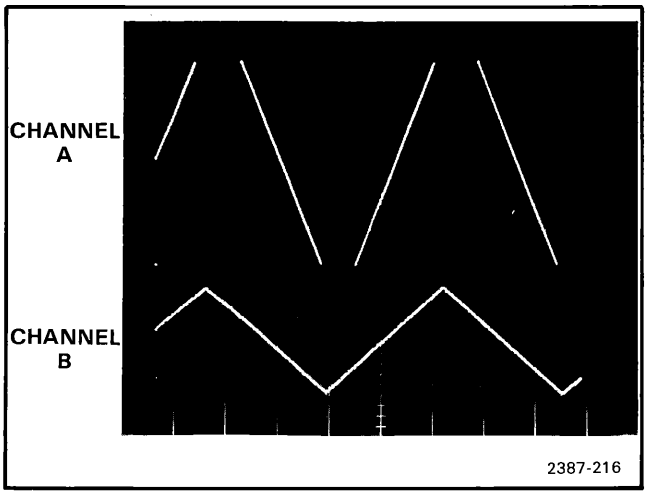


Figure 2-16. Clipping the output data on the XYZ monitor.

PROGRAMMING

INTRODUCTION TO IEEE 488

IEEE Standard 488-1975 describes a general-purpose bus for instrument systems. Called the IEEE 488 bus in this manual, it is also known as the General Purpose Interface Bus (GPIB). Its purpose is to provide an effective communications link over which messges can be carried between instruments in a clear and orderly manner. Instruments designed to operate according to the standard can be connected directly to the bus and operated by a controller with appropriate programming.

NOTE

The 7612D conforms to the 1975 edition of IEEE 488.

IEEE 488 SYSTEM

The bus uses eight data and eight control lines. Information is transferred bit-parallel, byte-serial by an asynchronous handshake. This allows instruments with different transfer rates to operate together if they conform to the handshake state diagrams and other protocols defined in the IEEE standard.

A typical system (Figure 2-17) could include a controller, such as the TEKTRONIX CP4165 Controller with the CP4100/IEEE 488 Interface, a talker, such as a counter or digital multimeter, and a listener, such as a line printer or signal generator. More than one function can be combined in a single instrument. For example, the TEKTRONIX 7612D

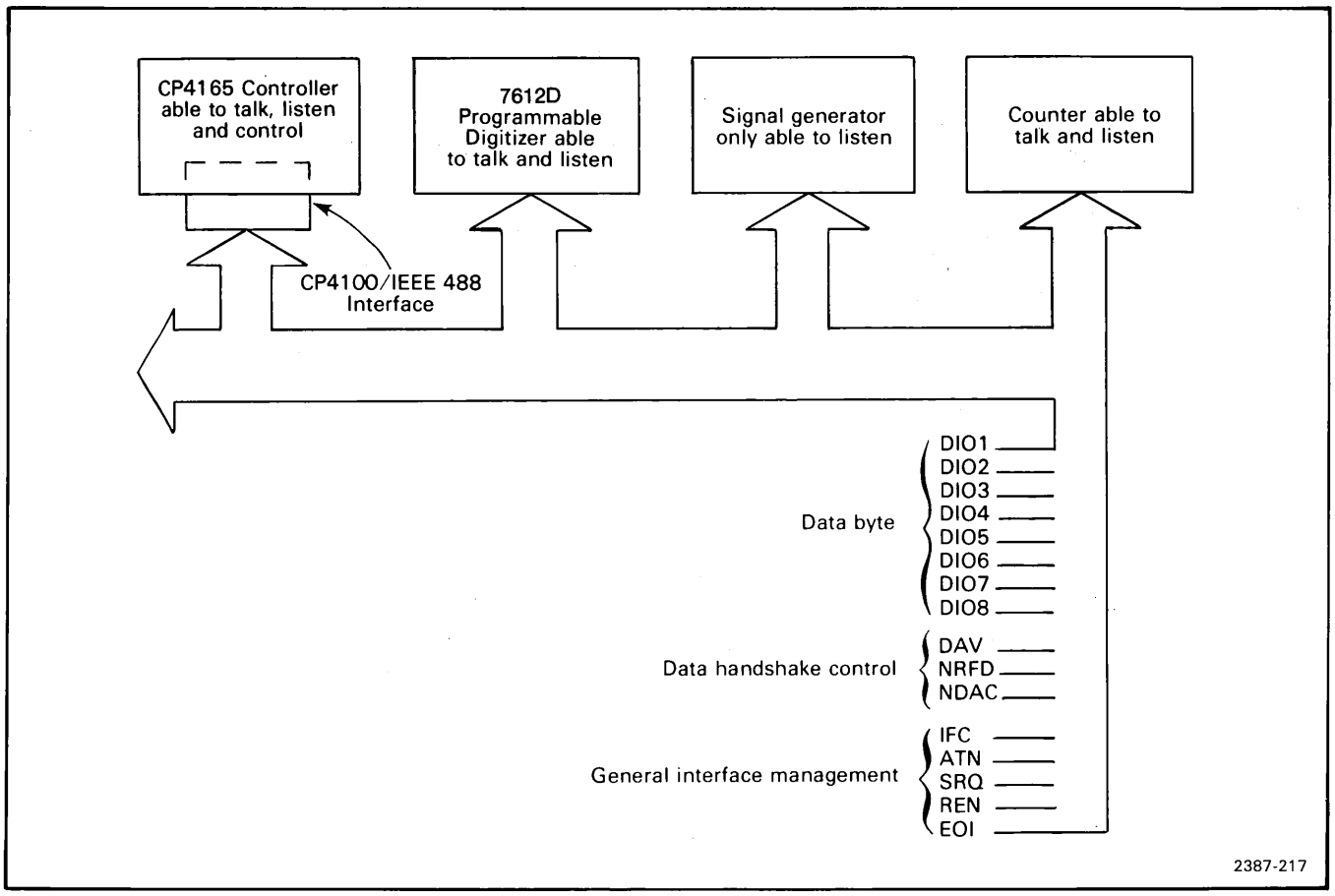


Figure 2-17. An IEEE 488 system showing some typical instruments and the bus signal lines.

Programmable Digitizer has both a listener and talker function. Many instruments, including the 7612D, also implement some or all of the other functions defined in the IEEE 488 standard which allow them to, for example, interrupt the normal sequence of events on the bus, report their status, or initiate a device function simultaneously with other devices on the bus. A complete list of the interface functions implemented in the 7612D is given in Table 2-3, later in this section.

Up to 15 devices, distributed over no more than 20 meters total cable length, can be connected to a single IEEE 488 bus. More than 15 devices can be interfaced if they do not connect to the bus but are interfaced through another device. Such a scheme is used for programmable plug-ins housed in the 7612D mainframe; the 7612D provides the interface between the bus and programmable plug-ins.

IEEE 488 is a flexible system—it works in a star or linear configuration (Figure 2-18). To maintain the bus electrical characteristics, a device load must be connected for each two meters of cable, and one more than half the devices connected at any time must be powered up (IEEE 488, 1975). Although devices are usually spaced no more than two meters apart, they can be separated farther if the required number of devices loads are lumped at any point. Also, if the system includes only the 7612D and a controller, they can be separated by four meters total cable length, because each provides a device load.

Messages on the bus are interface messages or device-dependent messages. Interface messages are used to manage the interface functions of the instrument. They designate talkers and listeners, for example. Device-dependent messages, by contrast, are not used by the interfaces to change their state or configuration, but are passed on to the device functions of the instruments. Such messages can be data, such as a waveform acquired by the 7612D, or remote-control messages, such as the setting of the 7612D's record length parameter.

IEEE 488 BUS SIGNAL LINES

The IEEE 488 bus contains three groups of signal lines: data, handshake, and control.

Eight lines, DI01 through DI08, are used to carry data (message) bytes on the bus.

The asynchronous, three-wire handshake is controlled by these lines:

DAV (data valid)—asserted by the transmitting device.

NRFD (not ready for data) and NDAC (not data accepted)—asserted by the receiving device.

Five interface lines are used for other control functions:

ATN (attention)—specifies how data on the DIO lines is to be interpreted: as interface messages when asserted; as device device dependent messages when unasserted.

IFC (interface clear)—is used to initialize the interface functions of all instruments and return control to the system controller.

SRQ (service request)—is asserted to request service from the controller-in-charge.

REN (remote enable)—allows remote control of devices on the bus.

EOI (end or identify)—indicates the last byte of a message or, when asserted with ATN, polls devices connected to the bus.

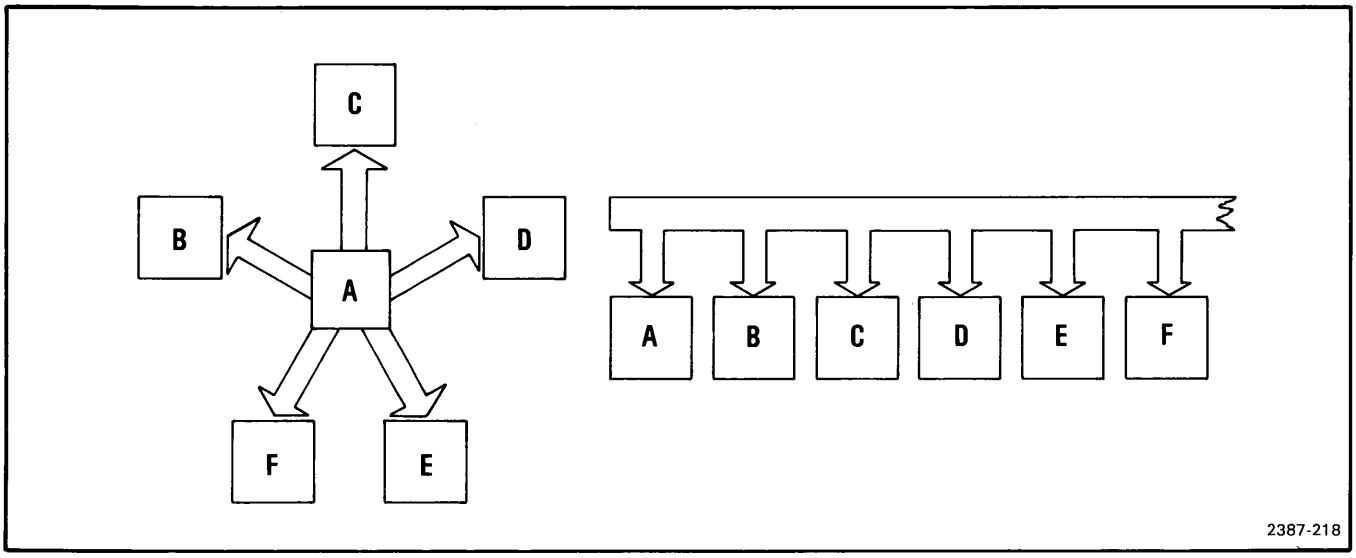


Figure 2-18. An IEEE 488 system can be configured in a star or linear manner without imparing the bus electrical characteristics.

See IEEE Standard 488-1975 (ANSI MC 1.1-1975), IEEE Standard Digital Interface for Programmable Instrumentation, for full definition of these lines and protocol for their use. A brief discussion is presented here.

A BYTE AT A TIME

The data and handshake lines are used for the source and acceptor handshake. Actually, they are two parts of the same handshake. Figure 2-19 shows the states of these lines as they are set by a talker using the source handshake and a listener using the acceptor handshake. The timing diagram relates the electrical signals on the bus to the states of the source and acceptor handshakes. By looking at both, it may be easier to grasp the sequence of the interlocked handshakes than it is to absorb the state diagrams in the standard.

1. To begin, the source goes to the Source GeNerate State (SGNS). In this state, the source is not asserting a data byte on the data lines or DAV. When no bus driver is asserting a line, it rises to the high level set by the bus terminating network. The acceptors are in the Acceptor Not Ready State (ANRS), asserting both NRFD and NDAC. In this condition, NRFD and NDAC are low.

2. The source sets the data byte on the data lines and entering the Source DelaY State (SDYS). If this is the last data byte in the message, the source may assert the EOI line at the same time. The source waits for the data to settle on the lines and for all acceptors to reach the ACceptor Ready State (ACRS).

3. Each acceptor says "I'm ready" by releasing NRFD to move to ACRS. This is one of the points in the handshake designed to accommodate slower listeners. The NRFD line can be thought of as a wired-OR input to the source handshake logic. Any acceptor can delay the source handshake by asserting this line.

4. When the source sees NRFD high, it enters the Source TRansfer State (STRS) by validating the data with DAV. The source then waits for the data to be accepted.

5. When the receiving devices see DAV low, they go to the ACcept Data State (ACDS). Each device asserts NRFD because it is busy with the current data byte and is not ready for another.

6. As each device accepts the data, it releases NDAC to move from the ACDS to the Acceptor Wait for New cycle State (AWNS). Again, all receivers must release the NDAC line for the source to see a high level. When the source sees NDAC high (all have accepted the data), it enters the Source Wait for New cycle State (SWNS).

7. In the SWNS, the source can unassert DAV. This causes the acceptors to proceed to the ANRS, their initial state in the handshake. In ANRS, they assert NDAC.

8. The source continues to the SGNS, its initial state in the handshake. In this state, it can change the data lines to prepare a new byte for transmission.

This is a typical sequence. The exact sequence is defined by the state diagrams in the standard. The only requirement is that different sequences must still conform to the state diagrams.

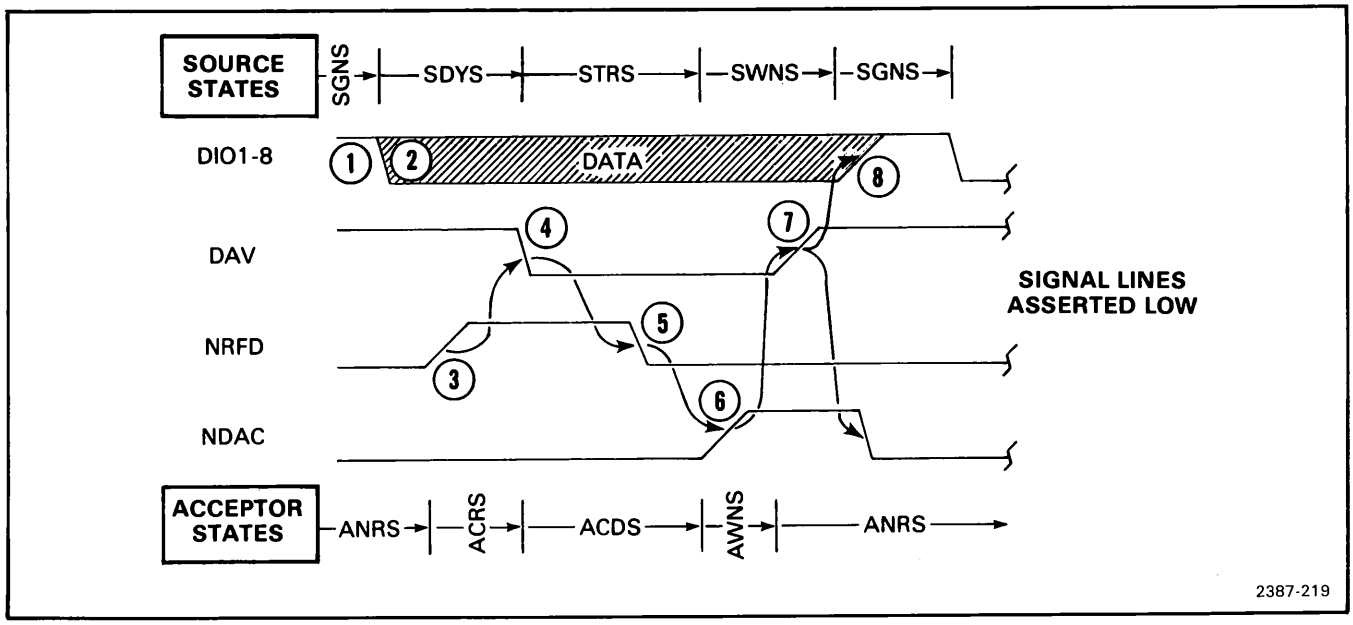


Figure 2-19. Handshake cycle to move a byte over the IEEE 488 bus. The numbers refer to steps in the text.

Although the above sequence involved a talker and listener(s), they're not the only ones allowed to use the handshakes. The source handshake is also used by the controller-in-charge to send system control messages; these are called interface messages to distinguish them from device dependent messages sent from talkers to listeners (see Figure 2-20). The controller asserts ATN to get the attention of all devices on the bus and then uses the source handshake to send interface messages on the data lines.

The interface messages that constitute the controller's vocabulary are defined by the standard. They can be thought of as ASCII codes given new meanings when sent by the controller with ATN asserted.

Three groups of interface messages are reserved for the listen, talk, and secondary addresses. When a device sees its talk address (called My Talk Address) and ATN simultaneously, it must become a talker, for instance. When the controller removes ATN, the device begins the source handshake to transmit its data. Similarly, My Listen Address and ATN tell a device to listen to the data sent by a talker. Secondary addresses provide unique addresses for devices that share a single listen or talk address. In the TEKTRONIX 7612D Programmable Digitizer, for example, secondary addresses select the mainframe or one of its plug-ins, all of which share the same IEEE 488 bus interface and primary bus address.

The controller uses other kinds of interface messages for other tasks. One is the Serial Poll Enable command (SPE) used by the service request interface function. Suppose an instrument is designed to assert SRQ when it has acquired some data. The controller must poll the devices to find the interrupting device because any one (or more than one) can assert SRQ. To conduct the poll, the controller sends SPE, a universal command, and then addresses each device in turn and reads a status byte from each. If the device asserted SRQ, it can code the status byte to tell the controller why.

Parallel Poll Configure (PPC) is an example of an addressed command. It prepares addressed devices to indicate who is requesting service. When ready, the devices respond together. A parallel poll is quicker, but more complicated, than a serial poll. Parallel poll is an optional function not implemented in the 7612D.

Device trigger is another function that uses an addressed command: Group Execute Trigger (GET). The instrument designer decides whether to use this function and for what purpose. The function is not implemented in the 7612D.

The controller issues the Device CLear message (DCL) to initialize internal functions of devices on the bus. A universal command, DCL, applies to all devices. Its effect on each instrument, however, is decided by the designer, who can choose to initialize any device function to any state that suits the purpose of the instrument. When the 7612D receives a DCL message, it resets its input and output buffers and resets the status byte (except power-up).

The interface messages are discussed in more detail later in this section.

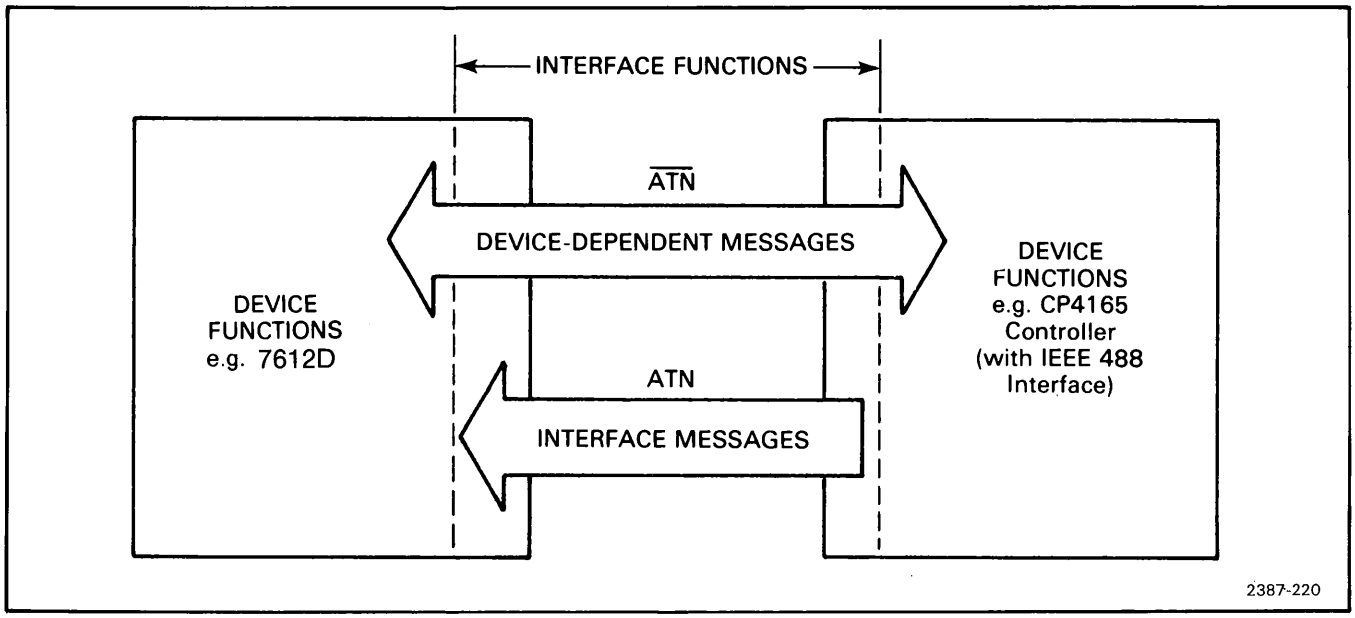


Figure 2-20. The controller-in-charge asserts the ATN line when sending interface messages.

7612D/IEEE-488 INTERFACE

The 7612D can be operated by remote control over the bus specified in IEEE Standard 488-1975. This section describes the functional characteristics of the interface and its response to interface control messages. Because the interface is the link between the IEEE 488 bus and the instrument, an understanding of the interface functions is necessary to effectively program the instrument.

The 7612D is fully programmable; all front-panel functions except ON/OFF can be controlled over the IEEE 488 bus. Waveform data can be transmitted at the maximum rate allowed by the slowest listener. An internal 6800 microprocessor system makes the 7612D friendly. Commands are simple and mnemonic, simplifying the programming task.

The 7612D also provides an interface between the IEEE 488 bus and TEKTRONIX 7000-series programmable plug-ins installed in the 7612D. In effect, the IEEE 488 bus is extended to the plug-ins through the 7612D plug-in interface. The interface and commands for the plug-in units are discussed in their manuals. Only those details which relate to the operation of the 7612D are described here.

IEEE INTERFACE FUNCTION SUBSETS

IEEE Standard 488-1975 identifies the interface function repertoire of a device on the bus in terms of interface function subsets. These subsets are defined in the standard. The subsets that apply to the 7612D are shown in Table 2-3.

How these functions are implemented is explained as part of the description of the commands used to program the 7612D and its response to interface control messages.

ADDRESSING

7612D IEEE 488 bus addresses are selected by internal switches. Primary bus addresses can be set over the full range allowed by the IEEE 488 standard: 32 to 62 (decimal) for My Listen Address (MLA) and 64 to 94 for My Talk Address (MTA). However, the values of the 7612D MLA and MTA are not independent of each other—they share the same lower five bits. If the internal switches are set for a MLA or 33, for instance, MTA is set to 65.

Secondary addresses are used to identify which of the three units (mainframe, channel A plug-in, or channel B plug-in), is addressed by MLA or MTA. The 7612D My Secondary Address (MSA) can be set over the full range allowed by the IEEE 488 standard: 96 to 126 (decimal).

Pressing the LOCKOUT button on the front panel displays the mainframe's primary and secondary addresses in the RECORD LENGTH and SAMPLES indicators, respectively. The lower five bits of the primary address are displayed in the RECORD LENGTH indicators (in decimal). To convert the displayed values to the actual primary addresses, add 32 (decimal) to the displayed value for the MLA and 64 for the MTA. The lower five bits of the mainframe's secondary address are displayed in the SAMPLES display. To find the actual secondary address, add 96 to the displayed value.

TABLE 2-3

7612D Interface Functions

Function	Subset	Capability
Source	SH1	Minimum settling time on handshake the DIO (data) lines before asserting DAV (T[sub]1] in the in the SH state diagram in the standard): ⩾1100 ns for the first byte after ATN is released and ⩾500 ns for the remaining bytes in a message.
Acceptor handshake	AH1	Complete.
Extended talker	TE6	Complete, except instrument cannot be set to talk-only mode locally; includes response to serial poll; requires secondary address.
Extended listener	LE4	Complete except instrument can not be set to listen-only locally; requires secondary address.
Service request	SR1	Complete.
Remote/local	RL1	Complete.
Parallel poll	PP0	No response to parallel poll.
Device clear	DC1	Complete.
Device trigger	DT0	No device trigger capability.
Controller	C0	None.

The bus addresses of programmable plug-ins are also determined by the 7612D MLA, MTA, and MSA. The plug-ins share the 7612D MLA and MTA. The plug-in MSAs are set by the 7612D MSA as follows:

Plug-In Compartment	Plug-in MSA
Channel A7612D	MSA + 1
Channel B7612D	MSA + 2

If the 7612D internal switches are set for a MSA of 97, for instance, the channel A plug-in MSA is 98, and the channel B plug-in MSA is 99. If programmable plug-ins are used, the 7612D MSA should not be set higher than 124 to allow address space for the plug-ins.

Some controllers are programmed for a 7612D primary and secondary address derived from the 7612D's MLA, MTA, and MSA, but not equal in value. With such a controller, primary and secondary addresses are entered in the range of 0 to 30. These addresses are the values of only the lower five bits of MLA, MTA, and MSA. (These are the bits set by internal 7612D switches and displayed when LOCKOUT is pressed.) The program converts these values to the 7612D's MLA when setting data to the 7612D and to the 7612D's MTA when reading data from the 7612D, tagging either with the 7612D's MSA. To do this, the program adds 32 to the primary address to obtain the MLA, 64 to the primary address for the MTA, and 96 to the secondary address for the MSA.

Because the instrument covers must be removed to set the address switches, refer selection to qualified personnel. Instructions are given in section 4 under "Selecting IEEE 488 Bus Address."

REMOTE/LOCAL FUNCTION

The remote/local function of the 7612D and its programmable plug-ins (if installed), is controlled by the IEEE 488 system controller and the front-panel LOCAL button. The instrument may have one of four states: local, remote, local with lockout, or remote with lockout.

Local

The 7612D and programmable plug-ins power-up in local state. To return to local state from remote state, one of the following conditions must occur:

1. The LOCAL button is pressed (when not in remote with lockout state).
2. The remote enable line (REN) changes from asserted to unasserted.
3. The instrument receives the GTL (Go To Local) message while addressed as a listener.

If the 7612D is executing a command or is armed, it waits until finished to return to local. The plug-ins return to local with the 7612D.

When the 7612D returns to local state, it checks the current settings of the instrument for conflicts. The validity check is identical to the one performed when the instrument is armed. Warning or error messages are reported on the front panel (See Warning and Error Messages at the end of this section for a summary of these messages). Then, the LOCAL button lights to indicate that the instrument has returned to local control. All instrument settings (except those that may have been modified as the result of conflicts found during the validity check) remain as they were set in remote state.

The instrument continues to process messages it receives over the bus while in local state, but it does not execute device-dependent commands that affect the state of the instrument or alter the state of data memory. If the instrument receives one of these commands, a 528 execution warning message is issued.

Remote

The 7612D and programmable plug-ins make the local-to-remote state transition when the 7612D receives MLA with ATN and REN asserted. Because the plug-ins and the 7612D share the same MLA, all three switch to remote state whenever the controller addresses either of the plug-ins or the mainframe with REN asserted.

When the 7612D enters the remote state, it lights the REMOTE button, enters the last front-panel entry (if it was not yet entered) into the acquisition program, and leaves all operating parameters as set. Front-panel functions that affect the state of the instrument or data memory are disabled, except for LOCAL, REMOTE and ON/OFF. All front-panel functions that do not affect the state of the instrument or data memory (e.g., DISPLAY BREAKPOINT) remain operational. The front-panel indicators are always active, and they show the current state of the instrument.

Lockout

When the local lockout (LLO) interface message is received with ATN asserted, the 7612D lights the LOCKOUT button and enters the remote with lockout state, or the local with lockout state. Because the remote-local function of programmable plug-ins is slaved to the mainframe, no lockout state is necessary in the plug-ins. When the 7612D receives the LLO message, the plug-ins remain in the state they were in when the message was received.

In remote with lockout state, both REMOTE and LOCKOUT are lighted. There is no change in the condition of operating functions. The front-panel operates the same as in remote state, except that the LOCAL button will not return the instrument to local control.

In local with lockout state, both LOCAL and LOCKOUT are lighted. Because this state allows full local control of the 7612D and plug-ins, it appears the same as the local state to the operator. There is a difference to the programmer, however. When the 7612D receives MLA with ATN asserrted in this state, it goes to the remote with lockout state (assuming REN has not been unasserted), instead of simply going to remote state as usual.

RESPONSE TO INTERFACE CONTROL MESSAGES

The 7612D does not respond to the following interface control messages:

1. PPC—Parallel Poll Configure
2. PPU—Parallel Poll Unconfigure
3. GET—Group Execute Trigger
4. TCT—Take Control

The 7612D does respond to the following interface control messages as described:

GTL—Go To Local. This causes the instrument to go to the local state. In local state, device-dependent messages continue to be accepted by the instrument, but only commands that do not affect the state of the instrument or data memory are executed (e.g. queries).

LLO—Local Lockout. If the 7612D is in the remote state, LLO causes the instrument to lock out all front-panel controls that affect the state of the instrument or data memory, including the LOCAL button. If the 7612D is in local state, the LLO message causes the instrument to lock out front panel controls when the instrument is set to remote state.

SDC, DCL—Selected Device Clear and Device Clear. Either of these messages reset the input and output buffers and reset the status byte (except power-up). These messages also halt the execution of an ALT or REP command when the current acquisition is complete.

SPE, SPD—Serial Poll Enable and Disable. The 7612D has full serial poll capability (see instrument status description).

IFC—Interface Clear. This message resets the interface functions only, not its operating modes. It has the same affect as sending the UNT (UNTalk) and UNL (UNListen) messages.

REMOTE CONTROL MESSAGES

The 7612D remote control messages are device-dependent messages on the IEEE 488 bus. As such, they are not specified in the IEEE standard. Tektronix has developed a Codes and Formats Standard designed to enhance compatibility with other IEEE 488 bus-interfaced instruments. To accomplish this, the standard specifies codes and syntax designed to be unambiguous, correspond to those used by similar devices, and be as simple and obvious as possible. The 7612D conforms to this standard, making it easier for the programmer to write and understand the device-dependent code.

The 7612D responds to device-dependent messages that contain one or both of two types of commands; set commands and query commands. A set command causes the instrument to set an operating parameter or mode, begin an acquisition, or send waveform data over the IEEE 488 bus. A query command causes the instrument to return the status of a specified operating parameter or function.

Remote control messages are sent to the 7612D in ASCII and all responses from the instrument, except for waveform data, are in ASCII. The parity bit is ignored on input and set to zero on ASCII output.

INPUT BUFFERING AND EXECUTION

All input to the 7612D is processed by the internal 6800 microprocessor. A remote control message begins when the 7612D is addressed as a listener, ATN is unasserted, and the transmitting device begins talking. The message ends when the message terminator is detected by the 7612D. The 6800 buffers all messages it receives. It does not begin executing the commands until:

1. The input buffer becomes full, or
2. the message delimiter is received.

When either of these conditions occurs, the instrument sets bit 5 of the status byte, indicating that it is busy. It also asserts the NRFD bus line unless it is unlistened. As a result, no more messages can be sent until all the commands in the input buffer are executed. Then the busy status is reset and the instrument can continue to listen.

The 7612D executes input messages containing multiple commands one command at a time. Commands in a string are handled according to these rules:

1. If a command sets an operating parameter, further commands are not executed until the current command is completed.
2. If the instrument detects an error in a command, the input buffer is cleared and SRQ is asserted to report the error. The status byte is set to indicate an error condition. The exact type of error can be determined with the ERR? query. Warning messages do not cause the input buffer to be cleared. The warning message is reported and command execution continues.

3. If a READ command is received before acquisition for the specified channel is complete, the instrument waits until the acquisition is complete before starting to read. During the wait period, the instrument reports busy status. The instrument may be assigned to talk during this period; however, instead of reporting the usual "talked with nothing to say" message (a single hex byte—FF), it begins talking as soon as the acquisition is complete and the READ command is executed.

4. When the instrument receives a a command requesting output, such as a READ or query command, it remains busy until the response to the last output command is placed in the output buffer. Further input is refused while the instrument is busy. If the 7612D is untalked while transmitting data, it waits to finish the transmission. The controller can interrupt and reset the talker function by sending the UNT message or addressing the 7612D as a listener. However, to reset the instrument's output buffer and clear the busy status, the controller must perform a device clear with the DCL or SDC interface messages.

5. Commands that require output (READ or query commands) may be placed anywhere in a message string, and multiple output commands may be sent in a single message. However, the instrument expects to be addressed as a talker to get the response to each output command. If instead, it receives another set command or is addressed to listen, the output for all remaining commands is abandoned.

COMMAND SYNTAX

Formats given for the set and query commands are intended as guides and are not intended to fully define the format.

The following format symbols are used:

< >	indicates a defined element
[ ]	indicates the element or group of elements is optional and may be omitted
...	follows an element or group of elements that may be repeated

The following delimiters are used to punctuate 7612D commands:

Delimiter	Follows
<space>	Header
<comma>	Argument
<semicolon>	Message unit (command)

When listening, the 7612D responds to either of two messages delimiters:

1. The EOI line asserted concurrently with the last byte in the message whether data, a format character, or a lower-order delimiter such as semicolon. This is the standard delimiter for Tektronix instruments.

2. The ASCII code for line feed (LF) sent as a byte following the message and any format character or lower-order delimiter. This is an alternate delimiter provided for compatibility with some instruments or controllers from other manufacturers.

The 7612D responds to either EOI or LF according to the position of an internal jumper. Because the cover must be removed to set the jumper, refer selection to qualified service personnel; instructions are in section 4 under "Selecting Internal Jumpers."

With EOI selected as the message terminator, any combination of format characters can be inserted at the beginning or end of a message or after a delimiter. Format characters are carriage return (CR), LF, or space.

Format characters can also be used with LF selected as the message terminator. However, the 7612D interprets LF as the end of the message; it holds up the data transfer by asserting NRFD and executes all commands in the buffer before continuing to handshake data.

When talking, the 7612D uses EOI to delimit a message. It asserts the EOI line concurrently with the last byte in the message, normally the message unit delimiter (semicolon). However, if the internal jumper is set for LF as the message delimiter, the 7612D adds CR and LF beyond the normal end of the message (semicolon) and asserts EOI with LF. The 7612D does not source more data until retalked or serial polled. If the 7612D has no message to send when it is talked, it responds with a single data byte, hex value FF—all data lines asserted, along with EOI (when strapped for EOI as the message delimiter). If the instrument is strapped for line feed as the message delimiter, it sends FF, carriage return, and line feed. EOI is asserted with the line feed.

NUMBERS

Numbers are assumed to be ASCII-coded decimal digits (except for waveform data). Three kinds of numbers are used:

Representation	Description
<NR1>	Signed or unsigned integers including 0.
<NR3>	Signed scientific notation.
<N8>	Unsigned integer multiples of 8.

Numbers in NR1 notation are signed or unsigned integers; for positive integers, the plus sign is optional. Examples are:

+127
−64
2048

Numbers in NR3 notation are floating-point numbers expressed in scientific notation. The mantissa includes a deci-

mal point and is preceded by a sign. The exponent following the mantissa begins with the character E, followed by a plus or minus sign and then one or more digits for the exponent of the multiplier. Examples are:

1.37E-3	(for 1.37×10^{-3})
−1.E+4	(for -1×10^{4})
<space>0.E+0	(for 0)

Numbers in N8 notation are integer multiples of eight without a sign. Examples are:

16
64
2040

An explicit definition of the first two number types is given in ANSI x 3.42-1975, "American National Standard for Representation of Numeric Values in Character Strings for Information Exchange."

WAVEFORM DATA I/O

Data can be output by the 7612D at the maximum data rate allowed by the slowest listener or 750 kilobytes/second, whichever is slower. Waveform data is output in binary rather than ASCII. This enables greater throughput, in that data is moved in fewer bytes so data transfers require less bus time.

Waveform data sent in response to a READ, REP, or ALT command is sent in binary block(s) of the following format:

%<BYTE COUNT>[<DATA BYTES>]<CHECKSUM>;

Where:

% is the ASCII percent character.

BYTE COUNT is a 16-bit binary number sent in two bytes, most significant byte first. The value indicates the number of bytes that remain to be transmitted in the block, including the checksum, but not including the message unit delimiter (semicolon).

DATA BYTES are eight-bit binary data values in the range 0 to 255.

CHECKSUM is an eight-bit, twos-complement binary number that is the modulo-256 sum of all preceding bytes in the block excluding the % character.

; is the ASCII semicolon character.

When data is sent in response to a REP or ALT command, all blocks are in this format. However, EOI is asserted with the message unit delimiter (semicolon) between ALT or REP cycle only. It is not asserted with the semicolon that separates the A and B data blocks. For example, when waveform data is sent in response to a REP 2,A,B command, a semicolon separates the A and B data blocks but EOI is not asserted. EOI is asserted with each semicolon that separates the block pairs (i.e. the semicolon that follows the B data blocks).

SET COMMANDS

All commands except those listed as Query-Only commands in Table 3-2 can be used as set commands. The last letter of four-letter headers and arguments can be omitted from set commands.

The format for a single set command is:

<header><space><argument>[<semicolon>]

More than one argument is required for several commands, such as REC (set the number and length of records). For example:

REC<space><argument><comma><argument>[<semicolon>]

The SBPT command (Set BreakPoint and sampling interval) requires at least two arguments, and may have as many as 28. Again, commas separate the arguments.

Examples of single set commands are:

```
TMBS A;
SBPT 128,1.E−6,496,3.E−8;
READ A,1,4;
```

More than one set command can be sent as part of a single message if the commands are separated by semicolons. This requires the following syntax:

<set command><semicolon><set command>
[<semicolon><set command>]...[<semicolon>]

An example of multiple set commands in a single message is:

```
TMBS A;TRIG RIGHT;REC 4,512;ARM A;
```

Multiple READ commands may also be included in a message with other commands. However, the instrument must be addressed to talk for the response to each READ command. For example, the following message might be sent to the instrument:

```
REC 4,512;ARM A;READ A,1;READ A,3;TMBS B
```

The instrument sets the number and length of records and arms time base A. The first READ command is buffered and the instrument waits for channel A's acquisition to complete. Then, it expects to be addressed to talk (the talk address may be sent while the acquisition is in progress). The instrument begins sending the data acquired in record one of channel A as soon as the acquisition is complete and it is addressed to talk. When the transmission is complete, it expects to be addressed again to send the response to the second READ command. Because the response to the READ command will not fit in the output buffer, the instru-

ment remains busy until the data is transmitted. In this condition, the 7612D asserts NRFD and refuses any further input.

When the second transmission is complete, the TMBS B command is executed.

QUERY COMMANDS

Unless noted as a set command only, all commands in Table 2-4 can be used as query commands. A query is executed in either remote or local state. A message that contains only a query command requires the following syntax:

<header><question mark>[<semicolon>]

An example is:

TMBS?

A message can contain multiple queries, just as it can contain multiple READ commands. The set and query commands can be mixed in any order.

However, the instrument must be addressed to talk for the response to each query. If instead, another set command is sent, the response to the remaining query or queries is abandoned.

The 7612D responds to a query with a message similar to the set command format. Unless noted in Table 2-4, the syntax of the reply is:

<header><space><argument><semicolon>

For example, the query:

TMBS?

is answered with (when time base A is selected):

TMBS A;

NOTE

If the 7612D receives a message that is too long for its internal 128-byte input buffer, and the message generates output that is too long for the output buffer (128 bytes), the instrument asserts the IEEE 488 bus NRFD line, preventing any further communication on the bus. A DCL message will clear this condition.

COMMAND SUMMARY

Table 2-4 provides a summary of 7612D commands and arguments. Complete command descriptions are given later in this section.

TABLE 2-4
7612D Command Set

Header	Argument	Description	Notes
		INSTRUMENT COMMANDS	
TMBS	A B	Specify the time base to be programmed or queried by subsequent time base commands (Power-on state is TMBS A).	1
ARM	A B A,B B,A	Arms the time base(s) specified by the argument(s).	1,2
MTRIG		Generates triggers for both trigger channels.	1,2
WRI	ON	Assert SRQ when waveform data is readable.	1
	OFF	Do not assert SRQ when data is readable.	1,3
RQS	ON	Allows the instrument to assert SRQ to request service.	1,3
	OFF	Do not assert SRQ to request service.	1
CLK	INT EXT	Use internal clock for both time bases. Use externally supplied clock for both time bases.	1,3 1
BTA	ON	Triggerable After A mode ON.	1
	OFF	B Triggerable After A mode OFF.	1,3
REP	<NR1>,A	Repeat ARM/READ sequence for A time base n times.	1,2,6
	<NR1>,B	Repeat ARM/READ sequence for B time base n times.	1,2,6
	<NR1>,A,B <NR1>,B,A	Repeat ARM A,B, READ A, READ B sequence for A then B n times.	1,2,6
ALT	<NR1>	Repeats the ARM A, READ A, ARM B, READ B sequence n times.	1,2,6
REM	ON	Assert SRQ when REMOTE pressed.	1
	OFF	Do not assert SRQ when REMOTE is pressed.	1,3
COPY	AB	Copy time base A settings to time base B.	1,2
	BA	Copy time base B settings to time base A.	1,2
	LR	Copy left trigger settings to right trigger channel.	1,2
	RL	Copy right trigger settings to left trigger channel.	1,2

Header	Argument	Description	Notes
		TIME BASE COMMANDS	
REC	<NR1>,<NR1>	Set the number and length of records.	1,6
SBPT	<N8>,<NR3> [,<N8>,<NR3>]...	Set breakpoint locations and the sampling interval for the segment.	1,6
CBPT	[<N8>[,<N8>]]...	Clear all breakpoints or the specified breakpoints.	1,2,6
LTC	L[EFT] R[IGHT]	Specify the trigger channel to be programmed or queried by subsequent trigger function commands. Also selects the trigger channel to be associated with the currently selected time base.	1,3
MODE	PRE,<N8>	Set to pre-trigger by n samples.	1,6
	POST,<N8>	Set to post-trigger by n samples.	1,6

Header	Argument	Description	Notes
		TRIGGER CHANNEL COMMANDS	
SRC	INT	Select internal triggering source.	1,3
	EXT	Select external triggering source.	1
SLO	POS	Set trigger slope to positive.	1,3
	NEG	Set trigger slope to negative.	1
LEV	<NR1>	Set trigger level.	1,6
CPL	AC	Set trigger coupling to ac.	1
	DC	Set trigger coupling to dc.	1,3
HFR	ON	Enable high-frequency reject trigger.	1
	OFF	Disable high-frequency reject trigger.	1,3

Header	Argument	Description	
		DATA TRANSFER COMMANDS	
READ	A[,REC[,SEG]]	Read Data from channel A.	
	B[,REC[,SEG]]	Read Data from channel B.	

Header	Response	Description	Notes
		QUERY-ONLY COMMANDS	
ID?	ID TEK/7612D, V79.1,FYY	Identifies the instrument and firmware version.	
SET?	<CHARACTERS>	Returns all settings.	
ERR?	<NR1>	Returns code for current error condition.	6
NBPT?	<NR1>	Returns number of break-points.	6
HSFA?	<CHARACTER(S)>	Returns the horizontal scale factors for channel A.	
HSFB?	<CHARACTER(S)>	Returns the horizontal scale factors for channel B.	
VSL1?	<CHARACTER(S)>	Returns the vertical scale factors for channel 1 of the left plug-in.	
VSL2?	<CHARACTER(S)>	Returns the vertical scale factors for channel 2 of the left plug-in.	
VSR1?	<CHARACTER(S)>	Returns the vertical scale factors for channel 1 of the right plug-in.	
VSR2?	<CHARACTER(S)>	Returns the vertical scale factors for channel 2 of the right plug-in.	
RDO?	<CHARACTER(S)>	Returns 40 characters of readout information as acquired from plug-ins.	

Header	Argument	Description	Notes
		DIAGNOSTIC COMMANDS	
DEP	<ADRS>,<DATA>	Put Data in the specified 6800 address.	1,4,5
FET	<ADRS>	Fetch Data from the specified 6800 address.	1,4,5
EXEC	<ADRS>	Begin executing at the specified address.	1,4,5

Notes:

1— The set form of this command is not executed in LOCAL state.
The query form (where applicable) is executed in LOCAL or REMOTE.

2— Can be used only as a set command.

3— Power-up condition.

4— Use only as a diagnostic command.

5— ADRS and DATA format is: <H><HEX DIGITS>.

6— <NR1> integers with signs,
<NR3> signed scientific notation,
<N8> an unsigned integer multiple of eight.

ALT (Set only)

Syntax:

ALT <number of times to execute alternate sequence>

Examples:

ALT 5
ALT 0

Discussion:

The ALTernate command allows the user to alternately acquire data from channel A and channel B with minimal controller intervention. Throughput is improved because data can be read from one channel while an acquisition is in progress in the other channel.

The single numeric argument is an NR1-type number that specifies the number of times the alternate sequence is executed. If zero is specified for this argument, the sequence is continuously repeated until the instrument receives a device clear interface message. A negative number for the argument results in a command error.

The flow chart shown in Figure 2-21 illustrates the sequence executed by the ALT command. The instrument passes through the loop the number of times specified by the command argument.

First, the instrument arms channel A. The next valid trigger initiates channel A's acquisition. When channel A finishes its acquisition, channel B is armed and the instrument begins transmitting the data from channel A. Meanwhile, the next valid trigger initiates acquisition in channel B. If data transmission from channel A is completed before the channel B acquisition is complete, the instrument waits for channel B to finish. Then the loop count is decremented and compared to zero. If it is greater than zero, channel A is armed again. When the arm operation is complete, channel A becomes triggerable and channel B begins transmitting its data.

This alternating arm/read sequence continues until it has been executed the number of times specified in the ALT command argument.

The exact timing of this sequence depends on the acquisition time for each channel and the data transmission rate. If the acquisition times for both channels are greater than the data transmission time, the instrument can be configured to digitize data in an almost continuous data-logging mode. However, the restrictions of triggering, arm set-up time and pre-trigger data acquisition still apply.

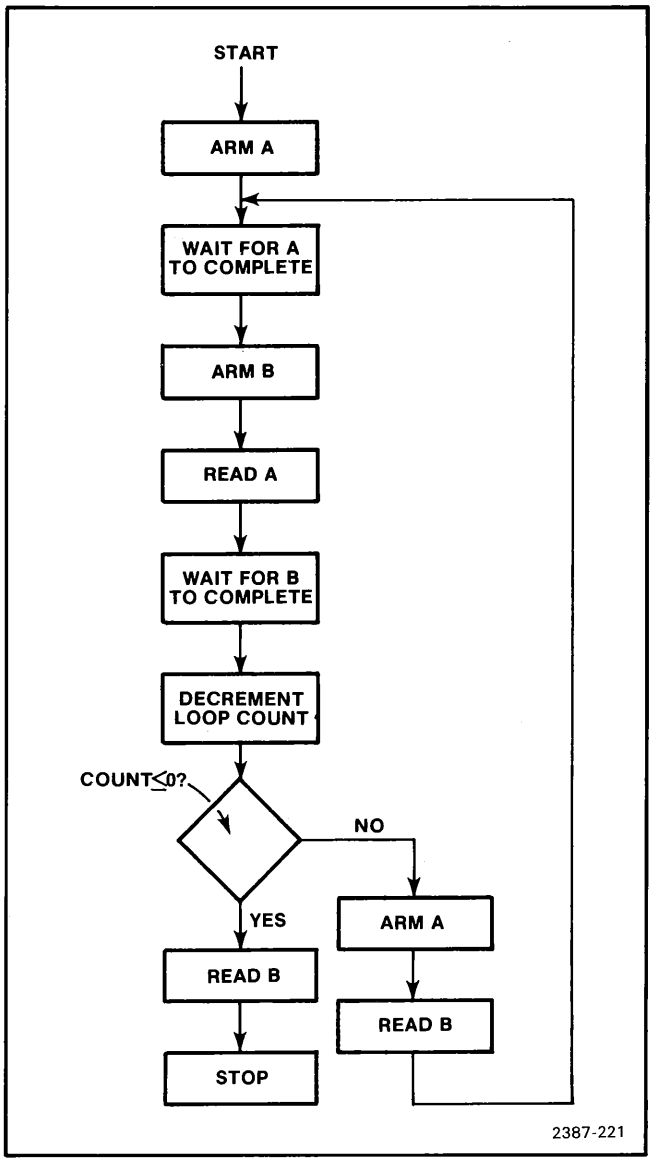


Figure 2-21. A flow chart of the ALT command execution.

ARM (Set only)

Syntax:

ARM { A | B | A,B | B,A }

Examples:

ARM A
ARM B
ARM A,B

Discussion:

The ARM command verifies the time base settings and prepares the channel to accept a trigger. Valid arguments are:

A—ARM time base A.
3—ARM time base B.
A,B, or B,A—ARM both time bases.

If any changes were made to the time base settings since the last ARM was performed, the settings are first checked for conflicts (e.g. breakpoints set beyond the record length, more than one record in post-trigger mode, etc.). If errors are found, the instrument asserts SRQ (if RQS is on) and reports the error. Error messages are also reported in the front-panel RECORD LENGTH display for channel A, and in the SAMPLES display for channel B. The settings are adjusted to resolve any conflicts that are found.

Next, the instrument initializes the time base(s) and, if PRE TRIGGER mode is selected, begins acquiring the pre-trigger samples. These samples are acquired at the sampling interval programmed for the first segment. When the pre-trigger samples are acquired, the instrument becomes triggerable and the next valid trigger initiates acquisition. A complete description of the ARM process is given in **Description of Commands**, in this section.

The ARM command is not executed in local state.

BTA (Set or Query)

Syntax:

BTA { ON | OFF } (set form)
BTA? (query form)

Examples:

BTA ON
BTA OFF
BTA?

Query Response:

BTA ON;
BTA OFF;

Power-up State:

BTA OFF

Discussion:

The BTA command turns B Triggerable after A mode ON or OFF. Valid arguments are:

ON—Sets the instrument to B Triggerable after A mode.This mode causes the B time base to become triggerable shortly after the first record of channel A has been acquired. One restriction is that the pretrigger holdoff for channel B must be satisfied before B will become triggerable.

If PRE TRIGGER mode is selected, one full record of pretrigger data must be acquired before the time base can accept a trigger. These samples are taken at the rate programmed for the first segment in the channel. However, the pre-trigger acquisition begins immediately after arming, so in many cases the pre-trigger acquisition for channel B will be complete by the time channel A finishes its acquisition.

OFF—Disables the B Triggerable after A mode. Both channels trigger independently.

The set form of the BTA command is not executed in local state. The BTA? query is executed in local or remote state. It returns the current state of the BTA function, ON or OFF.

CBPT (Set only)

Syntax:

CBPT[<sample number>[,<sample number>...]]

Examples:

CBPT
CBPT 120
CBPT 520,256

Discussion:

The Clear BreakPoinT command allows the operator to delete one or more breakpoints from all records in the selected channel. A specific breakpoint or breakpoints can be deleted by specifying the breakpoint location(s) in the command arguments. If no arguments are specified, all breakpoints except the fixed one at location zero are deleted.

When a breakpoint is deleted, the sampling interval for the segment preceding the breakpoint is applied to all samples from the preceding breakpoint to the next breakpoint. If all breakpoints are deleted, the sampling interval for the first segment is applied to the entire record.

If a breakpoint specified in a CBPT command does not exist, a 523 execution warning message is issued. The invalid breakpoint argument is ignored and all valid breakpoints in the argument list are deleted.

The CBPT command is not executed in local state.

CLK (Set or Query)

Syntax:

CLK {INT / EXT} (set form)
CLK? (query form)

Examples:

CLK INT
CLK EXT
CLK?

Query Response:

CLK INT;
CLK EXT;

Power-up State:

CLK INT

Discussion:

The Clock command selects the internal or external clock signal as the source for both time bases. Valid arguments are:

INT—Selects the internal 200 MHz clock signal to drive **both** time bases. Sample intervals specified in the SBPT command and returned in the SBPT? query are in seconds. The front-panel PERIOD indicator lights.

EXT—Selects the external clock signal applied to the rear-panel EXT CLK IN connector. Sample intervals specified in the SBPT command and returned in the SBPT query are external clock-period multipliers. The front-panel MULTIPLIER indicator lights.

When the external clock is selected, the instrument multiplies the period of the external clock by the selected multiplier. The period of the external clock signal does not have to be consistent. However, the instrument simply drives the input signal, so for an external clock period multiplier of 10, a sample is taken on every tenth pulse, regardless of the individual period of the pulses.

NOTE

If the external clock signal stops or is removed, the acquisition will not complete. The clock signal must be supplied to complete acquisition.

The set form of the command is not executed in local state. The CLK? query is executed in local or remote state. It returns the current state of the CLK flag, INT or EXT.

COPY (Set only)

Syntax:

COPY {AB | BA | LR | RL}

Examples:

COPY AB
COPY LR

Discussion:

The COPY command allows the user to COPY the settings of one time base or trigger channel to the other time base or trigger channel. Valid arguments are:

AB—Copy the settings of time base A to time base B.

BA—Copy the settings of time base B to time base A.

LR—Copy the settings of the left trigger channel to the right trigger channel.

RL—Copy the settings of the right trigger channel to the left trigger channel.

The time base functions copied with a COPY AB or COPY BA command are:

1. Record length and number of records (REC command)
2. Breakpoint locations and sample intervals (SBPT command)
3. Logical trigger channel (LTC command)
4. Pre- or Post-trigger mode and number of samples (MODE command)

The trigger functions copied with a COPY LR or COPY RL command are:

1. Trigger source (SRC command)
2. Trigger slope (SLO command)
3. Trigger level (LEV command)
4. Trigger coupling (CPL command)
5. High-Frequency Reject (HFR command)

Because the COPY command affects the state of the instrument, it is not executed in local state. The front-panel COPY button performs the same function, but it is executed only in local state.

CPL (Set or Query

Syntax:

CPL {AC | DC} (set form)
CPL? (query form)

Examples:

CPL AC
CPL DC
CPL?

Query Response:

CPL AC;
CPL DC;

Power-up State:

CPL AC

Discussion:

The CouPLing command selects ac or dc coupling of the trigger signal for the selected trigger channel. Valid arguments are:

AC—Select ac coupling of the trigger signal. The dc level of the signal is ignored and frequencies below about 30 Hz are attenuated.

DC—Select dc coupling of the trigger signal. Dc coupling provides more stable triggering of low-frequency signals. Remember that the plug-in Position control affects the trigger level with dc coupling.

The set form of the CPL command is not executed in local state. The query form is executed in local or remote states. It returns the current setting of the coupling parameter for the selected trigger channel, ac or dc.

DEP (Set only)

Syntax:

DEP H <hex address>,H<hex value>

Examples:

DEP H420,H3F
DEP HODC2,H127

Discussion:

The DEPosit command puts a byte into the specified address in internal 6800 microprocessor system. This command allows a service person to put bytes into any of the instrument registers controlled by the 6800, or to enter routines in the 6800 RAM (Random Access Memory) space for diagnostic purposes.

Figure 2-22 shows a memory map of the internal 6800 system. The RAM memory part of the map is expanded to show the free space between the stack and temporary storage used by the operating system. User-written subroutines should be confined to this area.

CAUTION

The use of the DEP command requires an intimate understanding of the 6800 system in the 7612D. Improper use of the command can interfere with the proper operation of the microprocessor system.

The first argument (hex address) specifies the 6800 address into which the data byte will be written. A one- to four-digit hexadecimal number is required, preceded by the letter "H."

The second argument (hex data value) specifies the byte to be written to the specified address. A one- or two-digit hexadecimal number is required, preceded by the letter "H."

ERR? (Query only)

Syntax:

ERR?

Query Response:

ERR 201;
ERR 0;

Discussion:

The ERRor query returns a numeric error code in NR1 notation if an error has occurred since the last ERR? query. If no error has occurred, the code is zero. The error code is not cleared by executing a valid command; the code is unchanged until another error occurs or the ERR? query is executed.

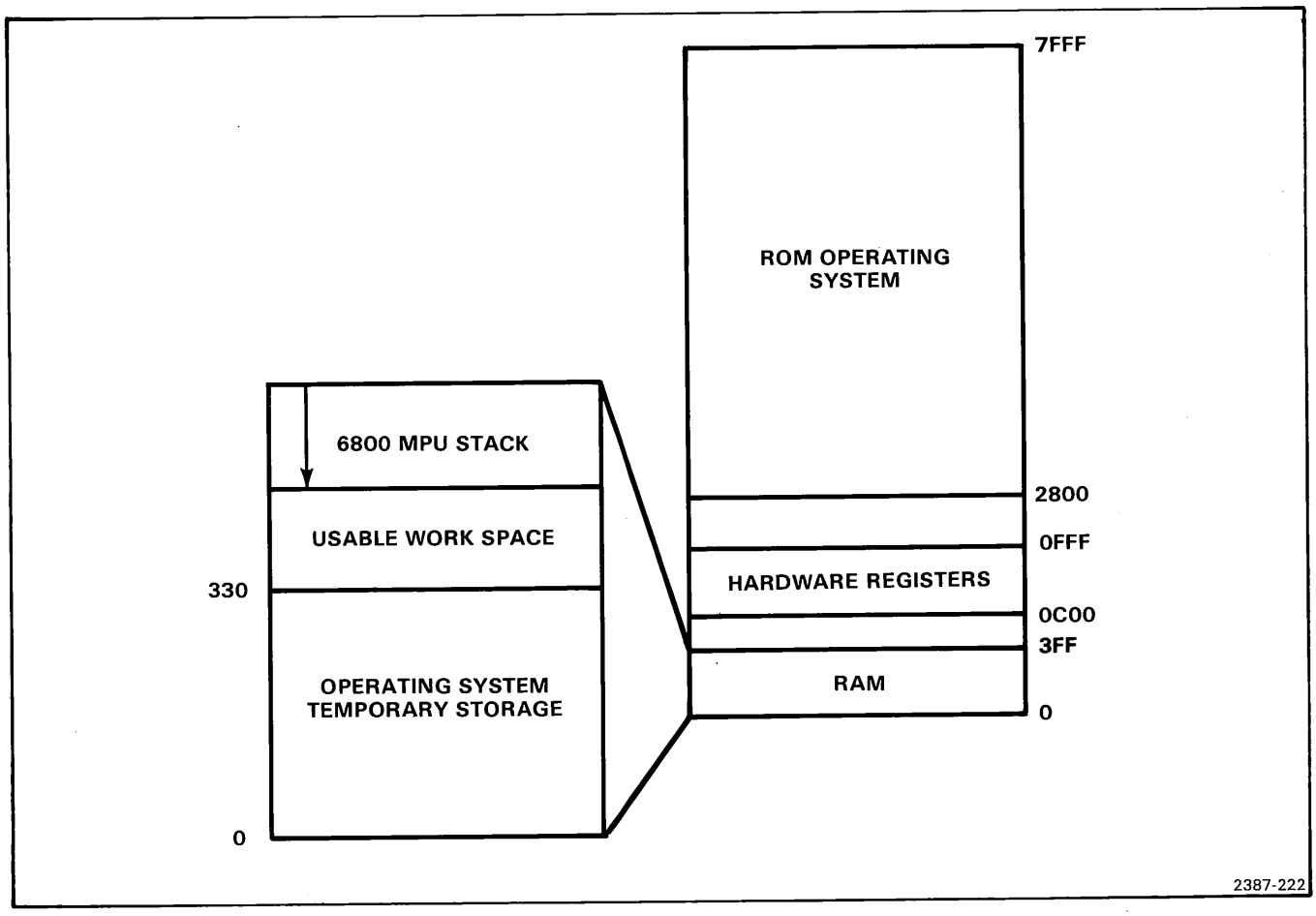


Figure 2-22. Memory map of the 6800 system.

EXEC (Set only)

Syntax:

EXEC H<hex address>

Examples:

EXEC H420

Discussion:

The EXECute command causes the 6800 to perform a JSR instruction to the address specified in the argument. It expects to find a subroutine starting at this address. The subroutine must return control to the operating system with standard subroutine linkage when completed. User-written subroutines should be confined to the free space in the 6800 RAM between the stack and the operating system temporary storage. Refer to the DEP command description for more information.

CAUTION

The use of the EXEC command requires an intimate understanding of the 6800 system in the 7612D. Improper use of the command can interfere with the proper operation of the microprocessor system.

The argument is a one- to four-digit hexadecimal address preceded by the letter "H."

FET (Set only)

Syntax:

FET H<hex address>

Examples:

FET HOC20
FET H3F0

Response:

H18;
HF4;

Discussion:

The FETch command reads a byte from the 6800 address specified in the command argument. The address is specified as one to four hexadecimal digits preceded by the letter "H."

The response is returned in ASCII with an "H" followed by two digits representing the hexadecimal value read from the specified location.

HFR (Set or Query)

Syntax:

HFR {ON / OFF} (set form)
HFR? (query form)

Examples:

HFR ON
HFR OFF
HFR?

Query Response:

HFR ON;
HFR OFF;

Power-up State:

HFR OFF

Discussion:

When the HFR (High Frequency Reject) parameter is ON, frequencies above about 50 kHz are attenuated in the trigger signal. This provides a means of filtering complex or noisy signals to provide more stable triggering. Valid arguments are:

ON—Enable high-frequency reject.
OFF—Disable high-frequency reject.

The set form of the HFR command is not executed in local state. The query form (HFR?) is executed in local or remote states. It returns the current state of the HFR parameter, ON or OFF.

HSFA?. HSFB? (Query only)

Syntax:

HSFA?
HSFB?

Query Response:

REC 1,2048;NBPT 1;SBPT 0,1E-9;MODE PRE,0

Discussion:

The HSFA? query returns the horizontal scale factors for channel A. HSFB? returns the horizontal scale factors for channel B. The scale factors information includes the number and length of records, numbers of breakpoints, breakpoint locations, sampling intervals, and trigger mode. The query response is in ASCII. The length of the message returned depends on the number of breakpoints set up.

ID? (Query only)

Syntax:

ID?

Query Response:

ID TEK 7612D,V79.1,F02

Discussion:

The ID? query returns an identification message for the instrument type and firmware version. The message format is:

ID TEK/7612D,V79.1,FYY

The two digits after the last F indicate the firmware version number.

LEV (Set or Query)

Syntax:

LEV <trigger level value> (set form)
LEV? (query form)

Examples:

LEV 113
LEV −42
LEV?

Query Response:

LEV 113;
LEV −42;

Power-up State:

LEV 0

Discussion:

The LEVel command selects the amplitude level of the trigger signal at which the trigger occurs. Valid trigger level values range from +127 to −128, corresponding to the eight-bit resolution of the instrument. A setting of +127 means that the time base triggers when the signal reaches full-scale amplitude. The trigger occurs at the selected point on the positive slope of the waveform if SLOpe is set to POSitive. The trigger occurs at the selected point on the negative slope of the waveform if SLOpe is set to NEGative.

The set form of the LEV command is not executed in local state. The query form (LEV?) is executed in local or remote states. It returns the current value of the level parameter for the selected trigger channel.

LTC (Set or Query)

Syntax:

LTC { L[EFT] / R[IGHT] } (set form)
LTC? (query form)

Examples:

LTC LEFT
LTC RIGHT

Query Response:

LTC LEFT;
LTC RIGHT;

Power-up State:

LTC LEFT (for channel A)
LTC RIGHT (for channel B)

Discussion:

The Logical Trigger Channel command selects the right or left trigger channel as the trigger source for the selected time base. The trigger parameters programmed for the selected trigger channel are applied to the currently selected time base. Valid arguments are:

R[IGHT]—The currently selected time base receives its trigger from the right trigger channel. The trigger parameters programmed for the right trigger channel (i.e., SLOpe, LEVel, CouPLing) are applied to the currently selected time base.

L[EFT]—The currently selected time base receives its trigger from the left trigger channel. The trigger parameters programmed for the left trigger channel (i.e., SLOpe, LEVel, CouPLing) are applied to the currently selected time base.

Both time bases may be programmed to receive their trigger signal from the same trigger channel. If, for example, both time bases are set for the right logical trigger channel, both time bases receive the same trigger signal and use the same trigger settings.

Be careful not to confuse the trigger SOURCE parameter set for each trigger channel with the LTC command. The SOURCE parameter selects the internal or external trigger signal source for the selected trigger channel. The LTC command applies all of the trigger parameters (including SOURCE) for one trigger channel to the selected time base.

The LTC command provides a convenient way of triggering both time bases simultaneously. Remember, however, that when pre-trigger mode is selected, both time bases must acquire one full record of pre-trigger data before becoming triggerable. As a result, it is possible for the time bases to trigger at different times even though they are receiving their trigger from the same trigger channel. If the record lengths, trigger modes, or breakpoints are different, the time required to acquire the pre-trigger samples may be different, causing one time base to become triggerable before the other. Refer to the **Arming the Time Base** discussion in this section for more complete information on this pre-trigger hold-off.

The set form of the LTC command is not executed in local state. The query form (LTC?) is executed in local or remote states. It returns the current state of the LTC paramter, LEFT or RIGHT.

MODE (Set or Query)

Syntax:

MODE { PRE / POST } ,<no. of samples> (set form)

MODE? (query form)

Examples:

MODE PRE,56
MODE POST,248
MODE?

Query Response:

MODE PRE,24;
MODE POST,248;

Power-up State:

MODE PRE,0

Discussion:

The MODE command selects the triggering mode, Pre-or Post-trigger, for the selected time base. The command arguments specify the trigger mode and the number of pre- or post-trigger samples to be acquired. Valid arguments are:

PRE,<N8>—Sets the 7612D to acquire N samples of pre-trigger data. The number of samples must be an integer multiple of eight from zero to 16 less than the length of the first segment. One full record of pre-trigger samples are acquired at the sampling interval of the first segment. From this data the programmed number of pre-trigger samples are stored; the remainder are discarded.

POST,<N8>—Sets the 7612D to acquire N samples of post-trigger data. The number of samples must be an integer multiple of eight from eight to the record length. In post-trigger mode, only one record may be selected. If more than one record is set up, an execution warning message is issued and the number of records is set to one when the instrument is armed.

When the time base is triggered, the programmed number of post-trigger samples at the sampling interval for the first segment will be ignored before the instrument begins storing data.

The pre- and post-trigger modes provide a convenient method of acquiring data before the trigger event or delaying the start of acquisition after the trigger. More complete information on the use of pre- and post-trigger modes is provided in the **Operating the 7612D** part of this section.

The set form of the MODE command is not executed in local state. The query form (MODE?) is executed in local or remote. It returns the trigger mode (PRE or POST) and the number of samples.

MTRIG (Set only)

Syntax:

MTRIG

Examples:

MTRIG

Discussion:

The Manual TRIGger command causes the Armed time bases to trigger by running the trigger level through its range (+127 to −128). If the input signal is out of the range (off the target), the time base does not trigger.

The MTRIG command has no arguments, and is not executed in local state.

NBPT? (Query only)

Syntax:

NBPT?

Query Response:

NBPT 4;

Discussion:

The NBPT? query returns the number of breakpoints currently set in the selected time base. The value is returned in NR1 format.

RDO? (Query only)

Syntax:

RDO?

Query Response:

RDO "<left chan. 1><left chan. 2>
<right chan. 1><right chan. 2>";

Discussion:

The RDO? query returns 40 characters of readout information as acquired from the plug-in units. The readout information is in ASCII and is divided into four fields, one for each channel of each plug-in. The readout is returned exactly as it is acquired from the plug-in. As a result, some special characters are replaced by ASCII characters. For example, the down arrow that usually indicates inverted polarity in 7000-series readout system is replaced by a minus sign.

The readout is returned enclosed in quotes as shown with spaces separating the fields. Empty fields are filled with spaces.

READ (Set only)

Syntax:

READ {A / B} [,<record no.>[,<seg. no.>]]

Examples:

READ A
READ B,2
READ A,0,3

Discussion:

The READ data command causes the instrument to transmit waveform data to the controller. The entire contents of one channel may be transmitted, or any record or segment may be individually transmitted. The channel (A or B), record number, and segment number are specified as command arguments. If the record and segment arguments are omitted, the entire contents of the specified channel is transmitted.

If included, the record-number argument must be an integer form zero to the number of records less one. The first record is designated record 0. For example, the command READ A,2 returns the waveform data from the third record in channel A.

The third argument (if included) defines the segment number to be read. If the segment number argument is included, a record number must also be specified. Valid segment numbers range from 0 to the number of segments less one. As with record numbers, the segments are numbered starting with zero, so the first segment is segment 0.

If a record number or segment number specified in a READ command does not exist, a 203 execution error message is issued and the command is ignored.

When part of the data memory is unused (e.g., when two records of 256 points are set up), only the valid waveform data is transmitted. Unused parts of data memory are ignored.

The device-dependent status byte (bit 8 of status byte = 0) indicates the state of data memory. When the time base is armed or an acquisition is in progress, waveform data for that channel is not readable. It is good practice to read the status byte before issuing a READ command to find out if the waveform data is readable. Refer to the **Device Dependent Status** discussion for more complete information on the status byte.

If a READ command is issued while waveform data is not readable, the instrument waits when addressed to talk. It begins transmitting as soon as the data becomes readable. Waveform data is transmitted in binary block format as discussed in the **Waveform Data I/O** part of this section.

The READ command does not affect the state of data memory, so it is executed in local or remote states. A READ command may be executed as many times as requried without re-arming the instrument.

REC (Set or Query)

Syntax:

REC <No. of Rec.>,<Length of Rec.> (set form)
REC? (query form)

Examples:

REC 2,1024
REC 8,256
REC?

Query Response:

REC 2,1024;
REC 4,256;

Power-up State:

REC 1,2048

Discussion:

RECord command sets the number and length of the records for the time base selected with the TMBS command. The first argument defines the number of records. Integer values from one to eight are acceptable.

The second argument defines the length of the records. Permissible values are 256, 512, 1024, or 2048 with one restriction: the number of records times the record length cannot exceed 2048 (the maximum record length). Invalid, out of range, or conflicting arguments result in command errors. Refer to the **Warning and Error Messages** part of this section for a complete description of the error messages. All records are the same length.

Specifying a new length or number of records does not affect breakpoints set in the record(s) unless the breakpoints are beyond the new record length. Existing breakpoints are automatically applied to the new record(s). If the new record length causes some breakpoints to be beyond the record boundary, the invalid breakpoints are deleted and an execution warning message is issued.

The set form of the REC command is not executed in local state. The REC? query is executed in local or remote states. It returns the current number and length of records.

REM (Set or Query)

Syntax:

REM {ON / OFF} (set form)
REM? (query form)

Examples:

REM ON
REM OFF

Query Response:

REM ON;
REM OFF;

Power-up State:

REM OFF

Discussion:

The REMote command controls the instrument's response when the front-panel REMOTE button is pressed. Valid arguments are:

ON—Assert SRQ when REMOTE button is pressed if the RQS function is set ON (power-up condition). Set the status byte to reflect the remote request status.

OFF—Do not assert SRQ when REMOTE button is pressed, but set remote request status. This is the power-up condition.

The set form of the REM command is not executed in local state. The query form is executed in local or remote states. It returns the current state of the REM flag, ON or OFF.

REP (Set only)

Syntax:

REP <number of times to repeat>, {A / B / A,B / B,A}

Examples:

REP 4,A
REP 5,A,B
REP 0,B

Discussion:

The REPeat command allows the user to improve throughput when acquiring multiple waveforms by acquiring several waveforms with a minimum of controller interaction. The instrument executes ARM and READ commands the specified number of times for the specified channel(s).

Two arguments are required. The first argument is an NR1-type number that specifies the number of times the ARM and READ sequence is repeated. (For a definition of number types refer to the discussion headed **Numbers** in this section.) If this argument is zero, the 7612D continues to repeat the sequence until it receives a device clear interface message. A negative number for this argument results in a command error.

The second argument specifies the channel or channels that will execute the ARM and READ sequence. Valid arguments are:

A—Repeat the sequence ARM A;READ A the specified number of times.

B—Repeat the sequence ARM B;READ B the specified number of times.

A,B or B,A—Repeats the ARM A,B;READ A;READ B sequence the specified number of times. The waveform data is sent from channel A first, then from channel B, with a semicolon separating the binary data blocks. All waveforms are sent in the binary block form discussed under **Waveform Data I/O** with Blocks separated by semicolons. If the instrument is addressed to talk before an acquisition is complete, data is transmitted when the acquisition completes.

When the A,B or B,A argument is specified, Channel A data is always sent first. If channel A completes its acquisition before channel B, channel A data is transmitted immediately. Data from channel B is transmitted as soon as its acquisition is complete. If channel B finishes before channel A, transmission does not begin until channel A finishes and has completed transmitting its data.

The REP command is not executed in local state.

RQS (Set or Query)

Syntax:

RQS {ON / OFF} (set form)
RQS? (query form)

Examples:

RQS ON
RQS OFF
RQS?

Query Response:

RQS ON;
RQS OFF;

Power-up State:

RQS ON

Discussion:

The RQS (ReQuest Service) command enables or disables the instrument's SRQ function. Valid arguments are:

ON—Allows the instrument to assert SRQ to request service. Bit 7 of the status byte is set when SRQ is asserted.

OFF—Disables the instrument's SRQ function. Because SRQ is never asserted, bit 7 of the status byte is always cleared.

The set form of the RQS command is not executed in local state. The RQS? query is executed in local or remote state. It returns the current state of the RQS function, ON or OFF.

SBPT (Set or Query)

Syntax:

SBPT <location>,<sample interval>
[,<location>,<sample interval>]... (set form)
SBPT? (query form)

Examples:

SBPT 0,10E-9
SBPT 16,1E-6
SBPT 256,40E-7,120,2E-5,520,3E-6

Query Response:

SBPT 16,1E-6;
SBPT 120,2E-5,256,4E-6,520,3E-6;

Power-up State:

SBPT 0,5E-9

Discussion:

The Set BreakPoinT command sets breakpoints and sampling intervals for all records in the selected channel. A breakpoint divides the records into segments. A segment includes all the samples from the specified breakpoint to the next breakpoint or the end of the record. Each segment has an independent sampling interval. Figure 2-23 illustrates the relationship of breakpoints, segments, and records. Remember that all records are identical, so breakpoints apply to all records in the currently selected channel.

The SBPT command arguments are specified in pairs. The first argument of the pair defines the breakpoint location. The location is specified as a sample number, and it must be a multiple of eight from 16 to eight more than the trigger location number in pretrigger mode or 16 in post-trigger mode, or less than the record length (except for the fixed breakpoint at location zero). If the specified location is not a multiple of eight, the number is rounded to the next lower multiple of eight and a 521 execution warning message is issued.

The second argument of the pair defines the sampling interval associated with the breakpoint. The sampling interval applies to all samples from the existing breakpoint to the next breakpoint or the end of the record. The range of valid sampling interval values depends on the selected clock source. When the internal clock source is selected (front-panel CLK button lit), sampling intervals range from 1 second to 5 nanoseconds and are given by the formula:

$S.I. = (5\ ns)(X * 10^{Y})$

Where:

X=1,2,4,6,...,20
Y=0,1,...,7

When the external clock source is selected, the sampling interval parameter represents an external clock period multiplier. The period of the signal applied to the rear-panel EXT CLK connector is multiplied by the selected external clock period multiplier. Valid values range from 1 to 200 $\times$ 10^6 and are given by the formula:

$$S.I. = (Ext\ Clock)(X^* 10^Y)$$

Where:

X=1,2,4,6,...,20
Y=0,1,2,...,7

Again, if the value specified in the command argument is within the valid range but does not conform to the formula, the 7612D sets it to the next lower valid period multiplier and issues a warning message.

Table 2-5 shows all the valid internal clock sampling intervals and their corresponding external clock period multipliers.

Up to 14 breakpoints (14 argument-pairs) may be specified in one SBPT command as along as one of the argument pairs defines the sampling interval for the fixed breakpoint at location zero. The total number of breakpoints cannot exceed 14. If an attempt is made to define more than 14 breakpoints (including the fixed one at location 0), an execution error message is issued and the additional breakpoints are ignored.

If a specified breakpoint already exists, the sampling interval is applied to the existing segment. Otherwise, the breakpoint is set and the sampling interval applies to the new segment.

TABLE 2-5
Internal Clock Sampling Intervals and External Clock Period Multipliers

Interval	Multiplier	Interval	Multiplier
5E-9	1E+0	100E-6	20E+3
10E-9	2E+0	200E-6	40E+3
20E-9	4E+0	300E-6	60E+3
30E-9	6E+0	400E-6	80E+3
40E-9	8E+0	500E-6	100E+3
50E-9	10E+0	600E-6	120E+3
60E-9	12E+0	700E-6	140E+3
70E-9	14E+0	800E-6	160E+3
80E-9	16E+0	900E-6	180E+3
90E-9	18E+0	1E-3	200E+3
100E-9	20E+0	2E-3	400E+3
200E-9	40E+0	3E-3	600E+3
300E-9	60E+0	4E-3	800E+3
400E-9	80E+0	5E-3	10E+5
500E-9	100E+0	6E-3	12E+5
600E-9	120E+0	7E-3	14E+5
700E-9	140E+0	8E-3	16E+5
800E-9	160E+0	9E-3	18E+5
900E-9	180E+0	10E-3	2E+6
1E-6	200E+0	20E-3	4E+6
2E-6	400E+0	30E-3	6E+6
3E-6	600E+0	40E-3	8E+6
4E-6	800E+0	50E-3	10E+6
5E-6	10E+2	60E-3	12E+6
6E-6	12E+2	70E-3	14E+6
7E-6	14E+2	80E-3	16E+6
8E-6	16E+2	90E-3	18E+6
9E-6	18E+2	100E-3	20E+6
10E-6	2E+3	200E-3	40E+6
20E-6	4E+3	300E-3	60E+6
30E-6	6E+3	400E-3	80E+6
40E-6	8E+3	500E-3	100E+6
50E-6	10E+3	600E-3	120E+6
60E-6	12E+3	700E-3	140E+6
70E-6	14E+3	800E-3	160E+6
80E-6	16E+3	900E-3	180E+6
90E-6	18E+3	1E-0	200E+6

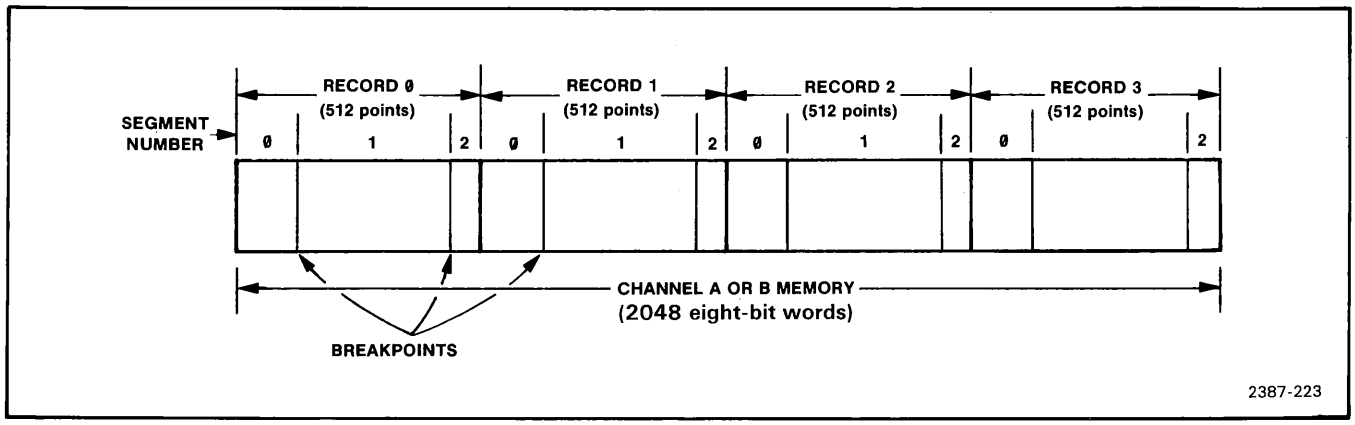


Figure 2-23. An example of memory partitioning showing the relation of records, segments, and breakpoints.

SET? (Query only)

Syntax:

SET?

Query Response:

CLK INT;BTA OFF;WRI OFF;RQS ON;REM OFF;TMBS A;REC 1,2048; SBPT 0,5E-9;MODE PRE,0;LTC LEFT;SRC INT;HFR OFF;CPL AC;LEV 0; TMBS B;REC 1,2048;SBPT 0,5E-9;MODE PRE,0;LTC RIGHT;SRC INT; SLO POS;HFR OFF;CPL AC;LEV 0

Discussion:

The SET? query returns the status of all programmable instrument functions. The query response shown above is for the default settings. The actual response to the query depends on the instrument settings but the order of the settings returned does not change. The message may be longer if more breakpoints are set. Notice that the settings for channel A are reported first, followed by the settings for channel B.

The header (**SET**) sent with all other query responses is omitted in this case. The string can be stored and directly transmitted back to the instrument without modification to restore the "learned" programmable settings. For example, the user may wish to set the instrument up from the front panel and write an application program that learns the settings when the REMOTE button is pressed. These settings can be restored at any time by sending the string stored from the query response.

SLO (Set or Query)

Syntax:

SLO {POS / NEG} (set form)
SLO? (query form)

Examples:

SLO POS
SLO NEG
SLO?

Query Response:

SLO POS;
SLO NEG;

Power-up State:

SLO POS

Discussion:

The SLOpe command selects the slope (positive- or negative-going) on which the time base triggers. The LEVel parameter selects the point on the selected slope at which the trigger occurs. Valid arguments are:

POS—Trigger on the positive slope of the trigger signal.

NEG—Trigger on the negative slope of the trigger signal.

The set form of the SLO command is not executed in local state. The query form (SLO?) is executed in local or remote states. It returns the current setting of the trigger slope for the selected channel, POS or NEG.

SRC (Set or Query)

Syntax:

SRC {INT / EXT} (set form)
SRC? (query form)

Examples:

SRC INT
SRC EXT

Query Response:

SRC INT;
SRC EXT;

Power-up State:

SRC INT

Discussion:

The SouRCe command selects the trigger source for the selected trigger channel. Valid arguments are:

INT—Select the internal trigger signal from the plug-in as the trigger source. This signal usually provides adequate triggering for most normal applications.

EXT—Select the signal applied to the rear-panel L or R TRIG connector as the trigger source.

The set form of the SRC command is not executed in local state. The query form (SRC?) is executed in local or remote states. It returns the current setting of the trigger source for the selected channel, INT or EXT.

TMBS (Set or Query)

Syntax:

TMBS {A / B} (set form)
TMBS? (query form)

Examples:

TMBS A
TMBS B
TMBS?

Query Response:

TMBS A;
TMBS B;

Power-up State:

TMBS A

Discussion:

The set form of the TMBS command selects the time base to be programmed by subsequent time base commands. Valid arguments are:

A—Select time base A to be programmed by subsequent time base commands. When time base A is selected, query commands that return time base settings (e.g., SBPT?) return the settings for time base A. The front panel displays the current state of time base A.

B—Select time base B to be programmed by subsequent time base commands. When time base B is selected, query commands that return time base settings (e.g., SBPT?) return the settings for time base B. The front panel displays the current state of time base B.

The TMBS command is not executed in local state. The TMBS? query is executed in local or remote state. It returns the currently selected time base, A or B.

VSL1?, VSL2?, VSR1?, VRS2? (Query only)

Syntax:

VSL1?
VSL2?
VSR1?
VSR2?

Query Response:

VSL1 +500.E0-3,V, CAL;
VSL2 NONE;

Discussion:

The Vertical Scale factors queries return the scale factors information for the Right or Left plug-in. If dual channel plug-ins are installed, the VSL2? and VSR2? queries return the scale factors for channel two of the left and right plug-ins, respectively. If a single channel plug-in is installed, the VSL2? or VSR2? queries return the word "NONE."

NOTE

The Alternate and Chop modes provided on dual-channel plug-ins, such as the TEKTRONIX 7A26 Dual Trace Amplifier will not operate properly when installed in the 7612D.

The four queries return the scale factors for the plug-in channels as follows:

VSL1? Left plug-in channel 1
VSL2? Left plug-in channel 2
VSR1? Right plug-in channel 1
VSR2? Right plug-in channel 2

WRI (Set or Query)

Syntax:

WRI {ON / OFF} (set form)
WRI? (query form)

Examples:

WRI ON
WRI OFF
WRI?

Query Response:

WRI ON;
WRI OFF;

Power-up State:

WRI OFF

Discussion:

The WRI (Waveform Readable Interrupt) command enables or disables the SRQ interrupt generated when a channel completes its acquisition. Valid arguments are:

ON—Enables the waveform readable interrupt. When an acquisition is complete and the data becomes readable, the instrument asserts SRQ. Bit 3 is set in the device status byte when channel A generated the interrupt; bit 4 is set when channel B generated the interrupt.

OFF—Disables the waveform readable interrupt. Bits 3 and 4 of the status byte are cleared.

The WRI command is not executed in local state. The WRI? query is executed in local or remote state. It returns the current setting of the WRI flag, ON or OFF.

INSTRUMENT STATUS

The 7612D reports a status byte when serial polled by the system controller. The status byte contains the internal status of the instrument. Two main types of status may be reported: System status and device status. System status indicates conditions that are common among all instruments that conform to the Tektronix Codes and Formats Standard (e.g., Command Error). Device status indicates conditions that are unique to a single instrument type.

An example of handling an SRQ and reading the status byte is shown in **Programming Examples**, which follows. The status byte reports errors in general terms. The ERR? query returns a code that more specifically defines the error.

The status byte read from the 7612D during the serial poll contains the following information:

BIT 8 Device status=1; System status=0
7 Service requested
6 Abnormal condition=1; Normal condition = 0
5 Busy
4 Device/system status
3 Device/system status
2 Device/system status
1 Device/system status

Normal condition system status:

BIT	8	7	6	5	4	3	2	1	
	0	1	0	X	0	0	0	1	- Power-on
	0	1	0	X	0	0	1	0	- Remote request

Power-on condition exists after the instrument is powered on. The remote request exists after the REMOTE button is pressed.

Abnormal condition system status:

BIT	8	7	6	5	4	3	2	1	
	0	1	1	X	0	0	0	1	- Command Error
	0	1	1	X	0	0	1	0	- Execution Error
	0	1	1	X	0	0	1	1	- Internal Error
	0	1	1	X	0	1	0	0	- Power-Fail Error
	0	1	1	X	0	1	0	1	- Execution Warning
	0	1	1	X	0	1	1	0	- Internal Error Warning

Command Error indicates that the 7612D has received a command that it cannot understand or implement under any circumstances. The command does not affect the state of the instrument.

Execution Error indicates that the 7612D has received a command that it understands but cannot implement due to the current state of the instrument. The command does not affect the state of the instrument.

Internal Error indicates an internal hardware failure.

Power-Fail Error indicates that a power failure is imminent or that an internal analog supply has failed. The instrument remains capable of responding to a serial poll for at least 10 ms. If a power failure occurs and the power is restored, this condition is replaced by the power-on condition.

Execution Warning indicates that the instrument has found a conflict in the settings and has changed the settings for the specified channel to resolve the conflict. This warning may also alert the user to potential problems with a particular setting combination.

Internal Warning indicates that the instrument has detected an internal error. The instrument remains operational, but the source of the problem should be found and corrected as soon as possible.

Device dependent status. Device dependent status is reported only when there is no system status to report.

BIT	8	7	6	5	4	3	2	1	
	1	X	0	X	0	0	0	0	- Neither channel is readable.
	1	X	0	X	0	X	0	1	- Channel A data is readable.
	1	X	0	X	X	0	1	0	- Channel B data is readable.
	1	X	0	X	X	X	1	1	- Both channels are readable.

Bit 3 is set if a waveform readable interrupt is generated by channel A; bit 4 is set when channel B generates the interrupt.

WARNING AND ERROR MESSAGES

Warning Messages

The first 18 warning messages describe errors that occur as the result of conflicting settings (e.g., breakpoints set beyond the record length). These warnings indicate unique combinations of four possible conditions. Table 2-6 shows the combinations and the associated warning messages. The eight remaining execution warning messages are summarized in Table 2-7. Table 2-8 shows the internal warning message.

TABLE 2-6
Execution Warning Message

Channel		Pre	Post	No of	Brk
A	B	Trig	Trig	Rec	Pts
501	511	0	0	0	1
502	512	0	0	1	0
503	513	0	0	1	1
504	514	0	1	0	0
505	515	0	1	0	1
506	516	0	1	1	0
507	517	0	1	1	1
508	518	1	0	0	0
509	519	1	0	0	1

PRE TRIG—1 indicates that the number of pre-trigger samples has been set to 16 less than the length of the first segment.

POST TRIG—1 indicates that the number of post trigger samples has been set to the record length.

NO. OF REC.—1 indicates that the number of records has been set to one because the channel is in post trigger mode.

BRK. PTS.—1 indicates that all breakpoints greater than or equal to the record length were deleted.

TABLE 2-7
Execution Warning Messages

Message Number	Description
521	Numeric argument is set to next lower number divisible by eight.
522	Sample interval or external clock-period multiplier is reset to first valid lower value.
523	Breakpoint not found in CBPT command.
524	BTA is on and only time base A is armed.
525	BTA is on and only time base B is armed.
526	<NR1> number is greater than 65535. The value is truncated.
527	Attempt to clear breakpoint zero is ignored.
528	Attempt to execute a command that changes settings or data memory is ignored in local state.

TABLE 2-8
Internal Warning Message

Message Number	Description
601	Instrument failed to trigger properly in power-up test.

Error Messages

The Error Messages returned by the ERR? query are divided into four groups: Command Error messages, Execution Error messages, Internal Error messages, and Power-Fail Error messages. Tables 2-9 through 2-12 summarize these messages.

TABLE 2-9
Command Error Message

Message Number	Description
101	Invalid command header
102	Invalid argument string
103	Nonnumeric argument found where a numeric argument is required
104	Invalid hexadecimal argument
105	Missing argument

TABLE 2-10
Execution Error Message

Message Number	Description
201	Maximum number of breakpoint exceeded
202	Negative argument invalid
203	Argument out of range
204	Invalid record length
205	Conflicting arguments
206	Invalid sampling interval or external clock period multiplier

TABLE 2-11
Internal Error Message

Message Number	Description
301	ROM found at wrong address
302	RAM failed self-test
303	Interrupt fault
304	Checksum error found in ROM
305	Data transmitter failed to begin or complete in allocated time.

TABLE 2-12
Power-Fail Error Message

Message Number	Description
401	Power failure is imminent

PROGRAMMING EXAMPLES

INTRODUCTION

Programming examples for several common 7612D operations, including a serial poll, setting and querying a 7612D function, and reading waveform data from the instrument are given here. These examples show program segments from TEK SPS BASIC V02 as well as the actual traffic on the IEEE 488 bus. The TEK SPS BASIC program segments shown are not intended to be complete programs, nor are they intended to be operational in themselves; they are provided as examples only. The type of controller and software you are using will determine the syntax of the program lines required to execute these functions.

The bus traffic required to execute the operations, with the exception of some bytes automatically inserted by TEK SPS BASIC, will be similar to that shown in the examples, regardless of the controller and software type. Notice also that many of the addressing and control operations are implemented by high-level TEK SPS BASIC commands, making the programming task much simpler. The task is simplified even more when the features of TEK SPS BASIC are fully utilized. Separate software manuals provide detailed information on using TEK SPS BASIC to drive instruments on the IEEE 488 bus.

Traffic on the IEEE 488 bus was recorded byte-by-byte using the TEKTRONIX 7D01 Logic Analyzer and DF2 Display Formatter in a Tektronix 7000-series oscilloscope. Comments are inserted to the left of the 7612D output to identify the byte(s) being output. The first column (excluding the comments) shows the state of the ATN (ATteNtion) line. The mnemonic appears when ATN is asserted and the column is left blank when ATN is not asserted. The second column is decoded from the DI01-8 data lines. When ATN is asserted, data on these lines is interpreted as addressed commands, universal commands, or bus addresses. Bus addresses are identified as being from the Listen Address Group (LAG), Talk Address Group (TAG), or Secondary Command Group (SCG). Interface messages such as UNTalk (UNT), UNListen (UNL), and Serial Poll Enable (SPE), are decoded and the mnemonic displayed. Bytes transferred when ATN is not asserted are assumed to be ASCII.

The third column shows the value of the data byte transferred. The value is a hexadecimal number if preceded by a dollar sign ($); it is a decimal number if there is no dollar sign. In the case of bus addresses, the lower five bits are decoded as a decimal number. The IEEE 488 standard identifies these bits at T1 through T5 for the talk address, L1 through L5 for the listen address, and S1 through S5 for the secondary address. Columns four, five, and six represent the state of the EOI, SRQ and REN lines, respectively.

These examples were obtained using a TEKTRONIX CP4165 Controller as system controller connected to a 7612D. The CP4165 included a CP4100/IEEE 488 Interface and was operated with TEK SPS BASIC V02 software with the low-level IEEE bus 488 driver. To guarantee a clear communication path, the software untalks and unlistens all devices both before and after transmitting and receiving messages. This results in some unnecessary UNT and UNL bytes. The extra bytes cause no harm, but are not always necessary for communication.

The 7612D was set to assert and recognize EOI as the message terminator as discussed under **Command Syntax** earlier in this section. The lower five bits of the 7612D bus addresses were set to zero. Therefore, in these examples, the 7612D and plug-in talk and listen addresses are shown as 00. The 7612D secondary address is shown as 00.

All bus traffic originated by the 7612D is printed in bold.

POWER-UP SRQ

When the 7612D powers up, it asserts SRQ and reports power-up status when serial polled. The following sample shows how a power-up SRQ can be handled. The technique could also be applied to other SRQs. The example shows only the code to acquire the status byte; decoding the status and taking appropriate action are application dependent.

```
10 SIFCOM @0,"SPE"
20 GET SB FROM @0,64,96
30 SIFCOM @0,"SPD"
```

Line 10 sends the universal command "SPE" to all devices connected to interface number 0. This tells the instruments on the bus that have serial poll capability to prepare to send their status byte. Next, the 7612D (set to talk address 64, mainframe secondary address 96) is addressed to talk by the GET statement in line 20. When the ATN line is unasserted, the 7612D puts its status byte on the bus. The GET statement takes the status byte and puts it in the variable SB. Finally, line 30 sends the Serial Poll Disable (SPD) command to end the serial poll process. The application program can then decode the status byte and take appropriate action.

Commands are included in TEK SPS BASIC that simplify the serial poll process considerably. The low-level commands are used here to illustrate the process. Refer to the appropriate software manuals for more information on these commands.

The bus traffic that results from these three lines is shown below. The UNTalk and UNListen messages are inserted by the GET statement to ensure a clear communication path. Remember that only the lower five bits of the primary address are shown in the third column, so a 00 is displayed for addresses of 32, 64, and 96.

ATN	SPE	$18	SRQ REN
ATN	UNT	$5F	SRQ REN
ATN	UNL	$3F	SRQ REN
ATN	TAG	$00	SRQ REN
ATN	SCG	$00	SRQ REN
(status byte)	A	$41	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	SPD	$19	REN

SET/QUERY

In the following example, the number and length of records is set and then verified by a query.

```
10 PUT "REC 4,512;REC?" INTO @0,32,96
20 GET A$ FROM @0,64,96
```

The PUT statement in line 10 addresses the 7612D to listen and sends the set and query commands as a single message. Line 20 addresses the instrument to talk, gets the query response, and puts it in the string variable A . The resulting bus traffic is shown below.

ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	LAG	$00		REN
ATN	SCG	$00		REN
	R	$52		REN
	E	$45		REN
	C	$43		REN
		$20		REN
	4	$34		REN
	,	$2C		REN
	5	$35		REN
	1	$31		REN
	2	$32		REN
	;	$3B		REN
	R	$52		REN
	E	$45		REN
	C	$43		REN
	?	$3F	EOI	REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	TAG	$00		REN
ATN	SCG	$00		REN
(query response)	R	$52		REN
	E	$45		REN
	C	$43		REN
		$20		REN
	4	$34		REN
	,	$2C		REN
	5	$35		REN
	1	$31		REN
	2	$32		REN
(message delimiter)	;	$3B	EOI	REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN

READ A

This example illustrates a simple READ operation. Data from all records of channel A is requested and sent as a single binary block. The format of the block is identical regardless of the number of records set up. The low-level SPS BASIC statements that might be used to execute this operation are shown below.

```
10 PUT "READ A" INTO @0,32,96
20 GET J FROM @0,64,96
30 IFDTM @0,"PAK","HBF"
40 GET BC FROM @0,64,96
50 INTEGER WA(BC-2)
60 IFDTM @0,"UNP"
70 GET WA FROM @0,64,96
80 GET J,J FROM @0,64,96
```

Line 10 addresses the 7612D to listen and sends the READ command. Then line 20 gets the first byte of the response, which is the binary data header (percent sign). The routine could check that the character is a percent sign, but in this example it is ignored.

The next two bytes of the 7612D's response are the byte count, sent high-byte first, so line 30 sets the interface data transfer mode to pack both bytes into a single variable, high-byte first. Line 40 gets both bytes and puts the result in the variable BC. The integer array that will contain the waveform data is dimensioned in line 50 to the byte count less 2. The byte count includes the checksum byte, which we do not want as part of the array, and TEK SPS BASIC arrays are dimensioned starting with 0 as the first element. As a result, for a byte count of 2049 there will be 2048 data bytes, and the array is dimensioned to 2047.

Line 60 resets the data transfer mode to unpacked and line 70 gets the waveform data and puts it in array WA. Finally, line 80 gets the last two bytes, the checksum and message unit delimiter (semicolon). Both bytes are ignored in this case, but they could be used for error checking.

The bus traffic that results from these BASIC statements is shown below. Most of the waveform data block is omitted to save space.

ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	LAG	00	REN
ATN	SCG	00	REN
	R	$52	REN
	E	$45	REN
	A	$41	REN
	D	$44	REN
		$20	REN
	A	$41	EOI REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(binary data header)	%	$25	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(byte 1 of byte count)	BS	$08	REN
(byte 2 of byte count)	SOH	$01	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(waveform data)	NAK	$95	REN
	SYN	$96	REN
	SYN	$96	REN
	SUB	$9A	REN
	—	—	—
	—	—	—
	—	—	—
	ETX	$03	REN
	EOT	$04	REN
	ENQ	$05	REN
	ACK	$06	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(checksum)	5	$35	REN
(message delimiter)	;	$3B	EOI REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN

This routine does not check for waveform readable status. If the waveform data is not readable when a READ command is executed, the instrument waits when it is addressed to talk. It begins transmitting as soon as waveform data becomes readable. A simple routine could be added before the READ to check the device-dependent status for waveform readable condition. Refer to the **Instrument Status** discussion for more information on the device-dependent status byte.

ALTERNATE

An example of using the ALT command is given here. This program segment is designed to be part of a data-logging routine that accepts data from the instrument and writes it to a disk file or other high-speed device. The example is written in TEK SPS BASIC, but, for the purpose of example, does not use many of the high-level features available.

```
10 PUT "ALT 0" INTO @0,32,96
20 GET J FROM @0,64,96
30 IFDTM @0,"PAK,"HBF"
40 GET BC FROM @0,64,96
50 DELETE WA
60 INTEGER WA(BC-2)
70 IFDTM @0, "UNP"
80 GET WA FROM @0,64,96
90 GET CS,J FROM @0,64,96
100 REM ** THE ROUTINE TO WRITE DATA TO THE **
110 REM ** LOGGING DEVICE GOES HERE **
—
—
—
150 GOTO 20
```

Line 10 sends the ALT command to the 7612D. The zero argument tells the instrument to continuously repeat the alternate sequence until it receives a DCL (Device Clear) interface message. When the first acquisition is complete, line 20 gets the binary data header (percent sign) and line 30 sets the interface data transfer mode to get the two-byte binary byte count. The byte count is acquired by line 40 and stored in the variable BC. Then the integer array WA is deleted to ensure that it is always properly dimensioned. Next, the array is dimensioned to the byte count less two (to leave out the checksum byte and account for the fact that BASIC arrays are dimensioned starting with zero).

Line 70 resets the data transfer mode to unpack and line 80 gets the waveform data from the instrument. Finally, line 90 gets the checksum and semicolon bytes.

As soon as channel A's acquisition is completed, channel B begins acquiring data. The acquisition in channel B progresses while data is being read from channel A.

At this point in the BASIC program, a data logging routine could be added to record the data on a disk or other device. When the data is recorded, the loop is repeated, starting at line 20. The loop is repeated indefinitely since zero was specified for the ALT command argument.

If a nonzero value is specified in the ALT command, the loop must be executed twice the number of times specified, because each ALTernate cycle sends two blocks of data—one for channel A and one for channel B.

The bus traffic for two passes through the BASIC loop looks like this:

ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	LAG	00	REN
ATN	SCG	00	REN
	A	$41	REN
	L	$4C	REN
	T	$54	REN
		$20	REN
	0	$30	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(A semicolon)	%	$25	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(byte count)	BS	$08	REN
(byte count)	SOH	$01	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(A data)	SOH	$01	REN
	STX	$02	REN
	STX	$02	REN
	ETX	$03	REN
	ETX	$03	REN
	ENQ	$05	REN
	—	—	REN
	—	—	REN
	—	—	REN
	NAK	$95	REN
	SYN	$96	REN
	SUB	$9A	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(A checksum)	5	$35	REN
(A delimiter)	;	$3B	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN
(B semicolon)	%	$25	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	UNT	$5F	REN
ATN	UNL	$3F	REN
ATN	TAG	00	REN
ATN	SCG	00	REN

(byte count)	BS	$08		REN
(byte count)	SOH	$01		REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	TAG	00		REN
ATN	SCG	00		REN
(B data)	ETX	$03		REN
	ETX	$03		REN
	—	—		REN
	—	—		REN
	—	—		REN
	—	—		REN
	—	—		REN
	GS	$9D		REN
	SUB	$9A		REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
ATN	TAG	00		REN
ATN	SCG	00		REN
(B checksum)	+	$2B		REN
(B delimiter)	;	$3B	EOI	REN
ATN	UNT	$5F		REN
ATN	UNL	$3F		REN
—	—	—		—
—	—	—		—
—	—	—		—

Notice that the binary block format is identical to a normal READ operation except that EOI is asserted at the end of each ALTernate cycle, and not between Channel A and B data blocks.

THEORY OF OPERATION

This section of the manual describes the circuitry in the 7612D Programmable Digitizer. The description begins with a discussion of the instrument, using the block diagram shown in Figure 3-1, and then continues in detail, showing the relationships between the stages in each major circuit. Schematics of all major circuits are given in Section 8, Diagrams and Circuit Board illustrations. Stages are outlined on the schematics with wide shaded lines; the stage names are in shaded boxes. Refer to the appropriate diagram along with the Troubleshooting Chart in Section 4, Installation and Maintenance, throughout the following discussion.

BLOCK DIAGRAM DESCRIPTION

The following discussion presents the overall concept of the 7612D before the individual circuits are discussed in detail. A block diagram of the 7612D is shown in Figure 3-1. The number within the diamond in each block refer to the diagram of the same number in the Diagrams and Circuit Board Illustrations section.

Figure 3-1 is a simplified block diagram of the 7612D. The diagram indicates signal and data flow in the instrument and shows the relationship of the microprocessor system (MPU) to the parts of the instrument it controls. Figure 3-1 also shows the relationship existing among blocks that represent the schematic diagrams.

ANALOG SIGNALS

The analog input signals from the plug-in units are coupled to the instrument through the Plug-In Interface. The differential outputs of the Plug-In Interface drive the Deflection Amplifiers, which, in turn, drive the vertical deflection plates of the EBS tubes. Because the ribbon electron beam covers the entire target horizontally, no horizontal deflection is necessary.

The Plug-In Interface also carries the analog trigger signals for the trigger generator circuits. The trigger generator circuits accept the signals from the plug-in units or the rear-panel TRIG IN connectors and generate digital trigger signals for the time bases. Trigger parameters such as level, slope, coupling, and source are set by the 6800 microprocessor on the basis of front-panel input or commands received on the IEEE 488 bus.

Circuits are included to accurately position the beam and control its alignment with the target and its rotation with respect to the vertical diode stripes on the target. The High Voltage Supply generates the minus 10 kV accelerating potential and the focus potentials for the EBS tubes.

DATA FLOW

The eight-bit gray code outputs from the tubes are continuously sampled at five-nanosecond intervals by the strobed Hybrid Comparators. The Time Base selects and stores data values at the programmed sampling interval. When the internal clock is selected, all valid sampling intervals are integer multiples of the basic five-nanosecond interval. If, for example, a sampling interval of 20 ns is selected, every fourth data value from the comparators is stored in the Data Memory; the unused values are ignored. If external clock is selected, the sampling intervals are integer multiples of the external clock signal. The Time Bases also control data storage by providing the memory addresses, clock signals, and select signals for the Data Memory.

Data is stored in the memory in gray code format. On output the data is converted to binary by the Translator board. It is then sent over an internal high-speed data bus to the IEEE 488 interface for output to an XYZ monitor or to the IEEE 488 bus.

INSTRUMENT CONTROL

The MPU system is the instrument master controller. it accepts and decodes commands from the front panel or from the IEEE 488 bus and sets instrument operating parameters in response to these commands. The MPU also controls the IEEE 488 interface and provides an interface to programmable plug-in units.

In Local state, the MPU monitors the front-panel buttons, and controls the front-panel display. When a parameter (such as sample interval) is being modified with the DECREMENT/INCREMENT buttons, the microprocessor cycles through only those values that are valid for the current state of the instrument. It also verifies the validity of the settings when the instrument is armed and reports error messages on the front panel and over the IEEE 488 bus.

In Remote state, commands are accepted from the IEEE 488 bus. The front panel remains operational, but front-panel inputs that would modify the state of the instrument or data memory are not executed.

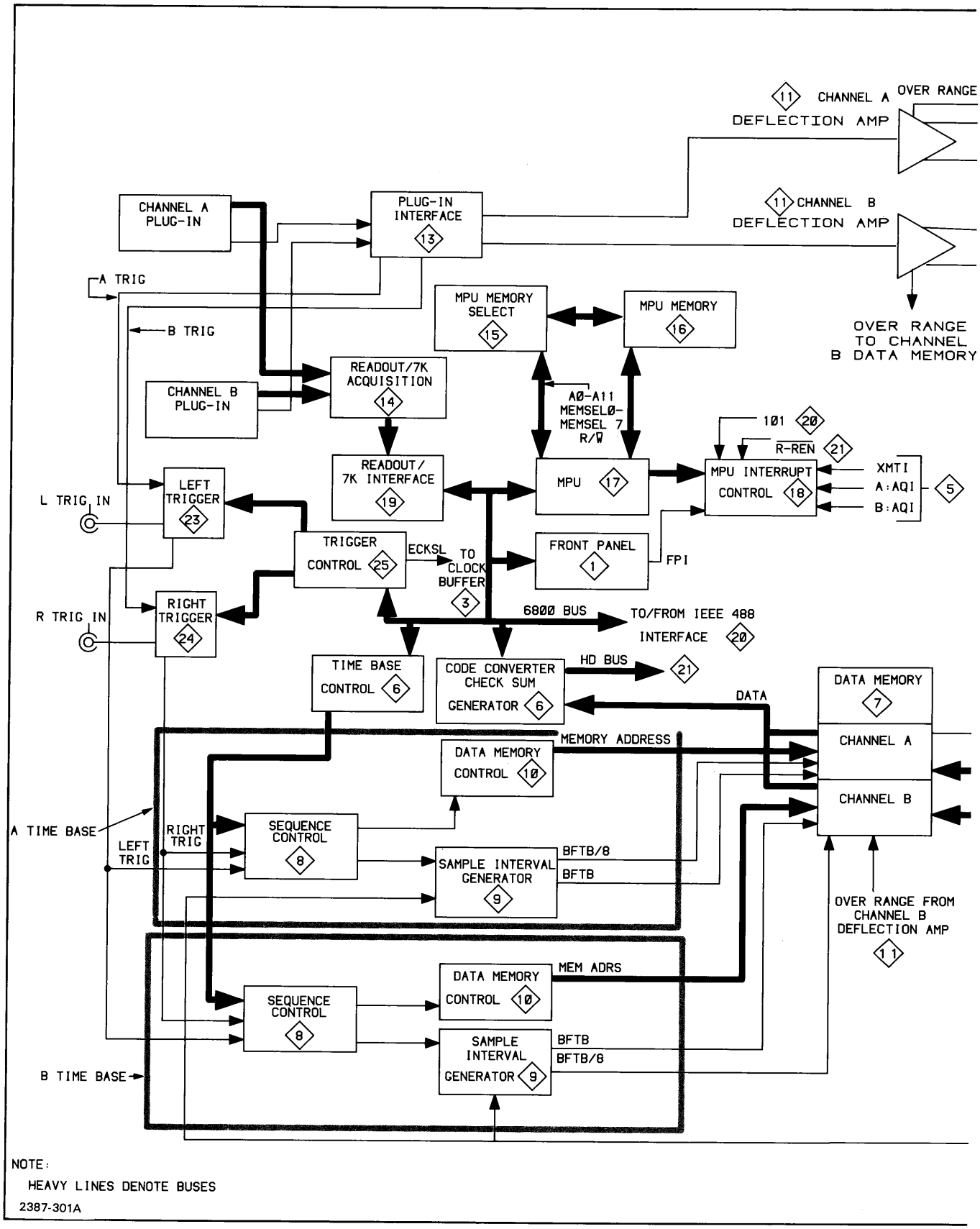


Figure 3-1. Block diagram of 7612D.

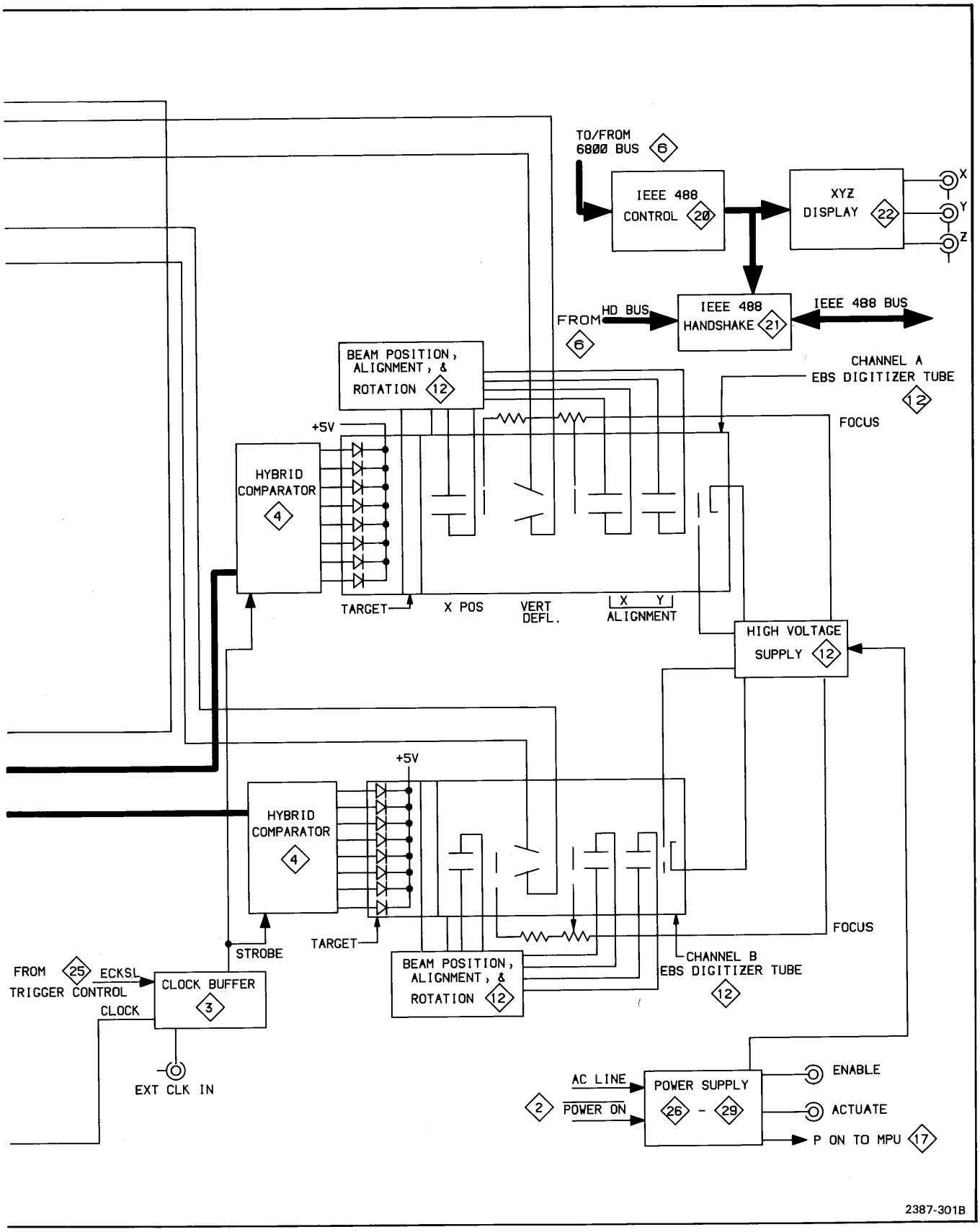


Figure 3-1 (cont). Block diagram of 7612D.

The MPU performs several other tasks. It acts as an interface for programmable plug-ins; all plug-in I/O passes through the MPU (MicroProcessing Unit) and is carried to the plug-ins via the 7K MPU Bus shown in Figure 3-1. The MPU also performs a power-up test of the instrument, monitors the states of the power supplies, and initiates a refresh of the XYZ display.

POWER SUPPLY

The 7612D Power Supply provides regulated voltages for its own analog and digital circuitry and for the plug-in units. It also supplies the drive for the High Voltage and Hybrid Comparator Supplies. In addition to the front-panel ON/OFF switch, remote control of the supply is provided through two rear-panel connectors. The supply can be turned on and off by applying a TTL-level signal to the REMOTE ACTUATE connector. The REMOTE ENABLE output can, in turn, control the REMOTE ACTUATE input for another similar instrument. When set to OFF, the rear-panel PRINCIPAL POWER switch disconnects the power supply from the ac line power. When the PRINCIPAL POWER switch is set to ON, the 7612D can be turned on by the front-panel ON/OFF switch or by a TTL low at the rear-panel REMOTE ACTUATE connector.

THE ACQUISITION SYSTEM

BLOCK DIAGRAM

The acquisition system in the 7612D accepts digital data from the EBS tubes, selects samples from this data at the programmed rate, stores the data, and controls the sampling interval and triggering. Figure 3-2 shows a block diagram of the acquisition system. Each channel contains one EBS tube, Hybrid Comparator, Time Base, and Data Memory (two memory boards per channel).

When the electron beam strikes a diode target in the EBS tube, that diode conducts, generating a current that is sensed by the Strobed Hybrid Comparators mounted on the end of the EBS tube. The output of the comparators is a differential eight bit ECL-level data word that defines the vertical position of the beam on the target. The comparators sample the output from the target at a constant 5 ns rate, and send their output data to the Data Memory through the High-Speed Shift Registers.

The Time Base accepts clock signals from the Clock Buffer and generates the memory addresses and chip select signals that control the Data Memory. Data
from the comparators is clocked into the data memory shift registers at the programmed sampling interval. Unused samples from the comparators are ignored. After eight samples have been shifted in, the contents of the shift registers are latched and stored in the Data Memory.

The MPU controls the Time Base. The Translator Board interfaces the microprocessor system and the Time Base. The MPU programs the Time Base for number and length of records, breakpoints, sampling intervals, and trigger mode. When the front-panel ARM button is pressed or the ARM command is received on the IEEE 488 bus, the MPU checks the validity of the time base settings, loads the settings into the time-base hardware (if the settings have changed since the last ARM operation), and initiates the acquisition.

When the acquisition is complete, the MPU controls the output of waveform data to the XYZ monitor or over the IEEE 488 bus in response to a READ, ALT or REP command.

AN INTRODUCTION TO ECL LOGIC

Many of the time base and memory functions implemented in the 7612D operate at speeds beyond the capability of ordinary TTL (Transistor-Transistor Logic), which is limited in most cases to about 50 MHz. The Emitter Coupled Logic (ECL) family provides high-speed logic elements and systems capable of operating beyond 200 MHz. Because the ECL family uses a basic gate structure that is fundamentally different from the well-known TTL gate, many people are unfamiliar with the characteristics of this high-speed logic family.

This discussion gives a brief overview of ECL concepts as an aid to understanding the operation of the 7612D time base and data memory. More complete information on the design and application of the ECL family is available in most manufacturer's ECL data books.

The Basic ECL Switch

At the heart of every ECL circuit is a current source whose output is steered through one of two transistors connected as a differential amplifier. Figure 3-3 shows a basic ECL switch. If the input voltage on the base of transistor Q1 is higher than the voltage the base of Q2, almost all the current flows through Q1. The V_{C1} output drops toward the negative supply V_{EE}, while the V_{C2} output goes to V_{CC}. Because the switching is accomplished by steering current instead of saturating and cutting off transistors as TTL logic does, the effects of junction capacitance and storage time are minimized and the switching speed is increased dramatically.

The input signal required to switch the gate is very small because the collector current in each transistor changes exponentially with a change in base voltage. A difference of base voltage as little as 250 mV can cause essentially all the collector current to flow through the transistor with the higher base voltage. In practice, the required input signal is made larger to improve noise immunity and to allow for normal differences between gates.

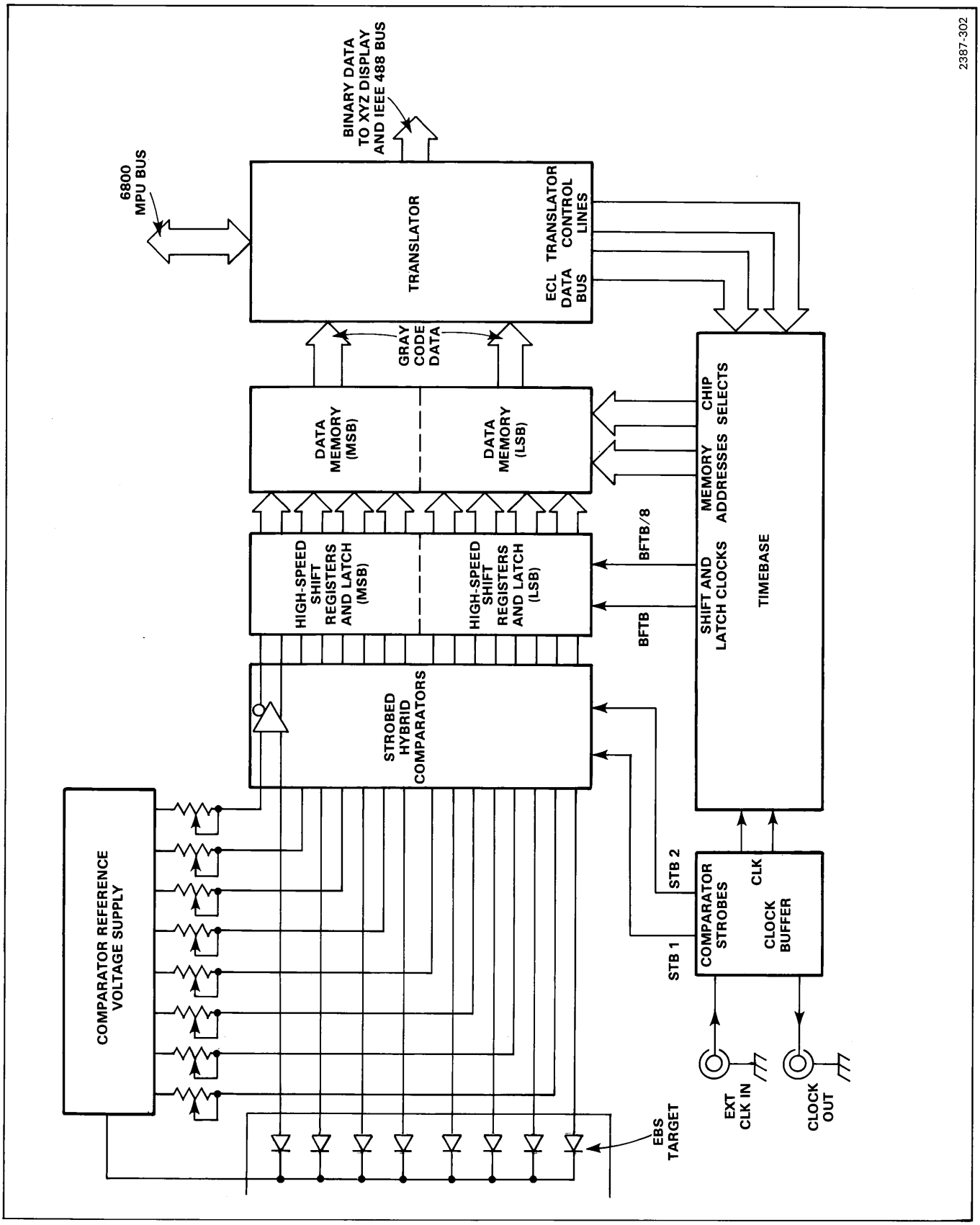


Figure 3-2. Block diagram of the acquisition system.

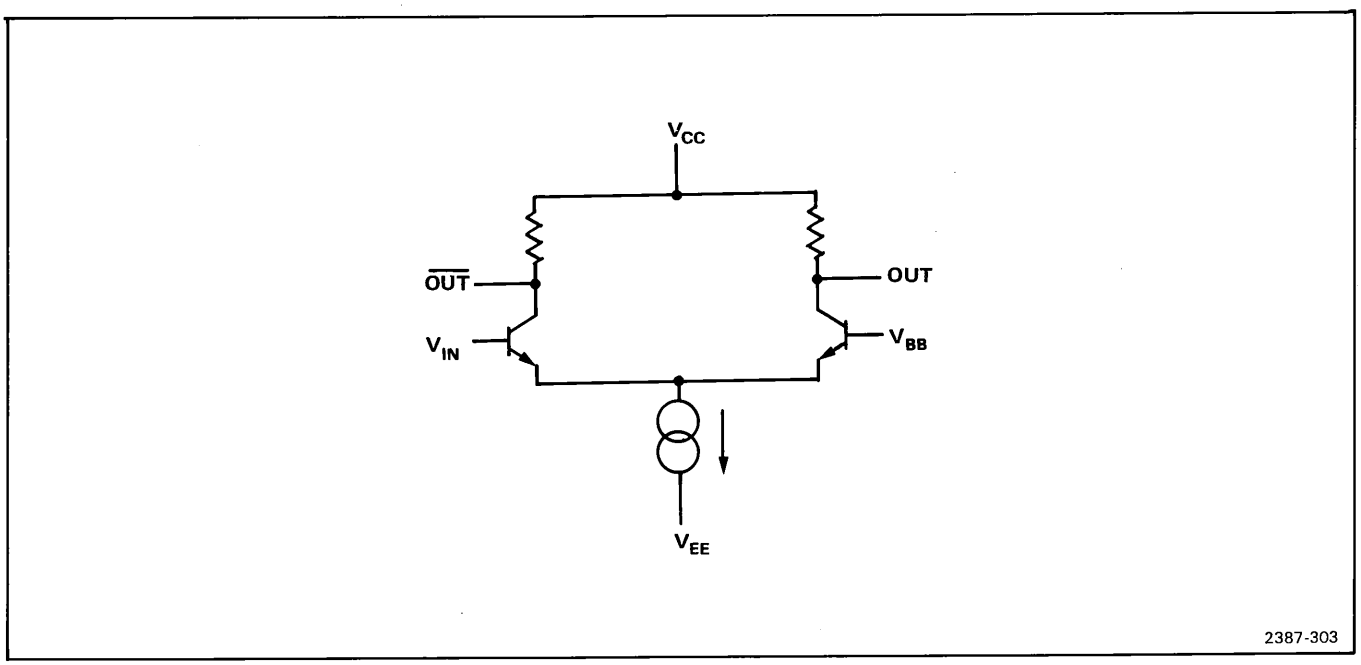


Figure 3-3. A basic ECL switch.

Improving the Basic ECL Switch

The output voltages of the basic switch are not compatible with the inputs of another similar switch. An emitter-follower output stage added to each output provides compatible output levels, isolates the outputs from the basic switch, and provides current gain (see Fig. 3-4). The emitter-followed outputs are left open (without internal pull-down resistor) to permit the use of wired-OR connections.

When returned to a −2 V supply through 50 ohms, the output of this "improved" ECL gate is about −0.7 V in the high state and about −1.6 V in the low state. The low output impedance of the emitter follower makes the gate suitable for driving transmission lines like coaxial cables or circuit-board runs with a characteristic impedance of 50 Ω or less.

Implementing Common Logic Functions in ECL

Because complementary outputs are available from each gate, the basic switch can form a simple buffer or act as an inverting buffer. By adding parallel transistors to one side of the differential pair, a simple OR/NOR function can be implemented (see Fig. 3-5). The base of the opposite transistor is usually connected to a reference voltage (V_{BB}) that sets the switching threshold of the gate. In a similar fashion, differential transistor pairs may be added in series to form AND/NAND gates (Fig. 3-6).

ECL in the 7612D

Most of the ECL parts used in the 7612D Time Base and Data Memory Boards are from the standard 10K (10XXX type numbers) and 100K (100XXX type numbers) ECL families. Typical propagation delay through a 10K-family gate is about 2 ns, and typical delay through a 100K-family gate is about 0.5 ns.

The ECL logic in the 7612D is powered by two supplies: the −2 V supply and the −5.2 V supply. Gate outputs are pulled down to the −2 V supply, typically through about 68 Ω. The −5.2 V supply is the V_{EE} supply for the ECL gates.

A WORD ABOUT SIGNAL NAMES

The 7612D contains two complete acquisition channels. Because each instrument has two identical Time-Base Boards and four identical Memory Boards (two per channel), some schematics represent more than one board. Many of the signal names used have A: or B: prefixes, indicating that there are two signals of the same name—one for the Channel A circuitry and one for the equivalent Channel B circuitry. On schematics that describe an identical board used in both channels, the A: or B: is not shown, because the prefix depends on the channel where the board is used. For example, two SEL (SELect) lines come from the Translator Board on diagram 5, A:SEL and B:SEL. The signal appears as SEL on the Data Memory Board (diagram 7) because the signal will be A:SEL if the Data Storage Board is plugged into channel A or B:SEL if the board is plugged into channel B.

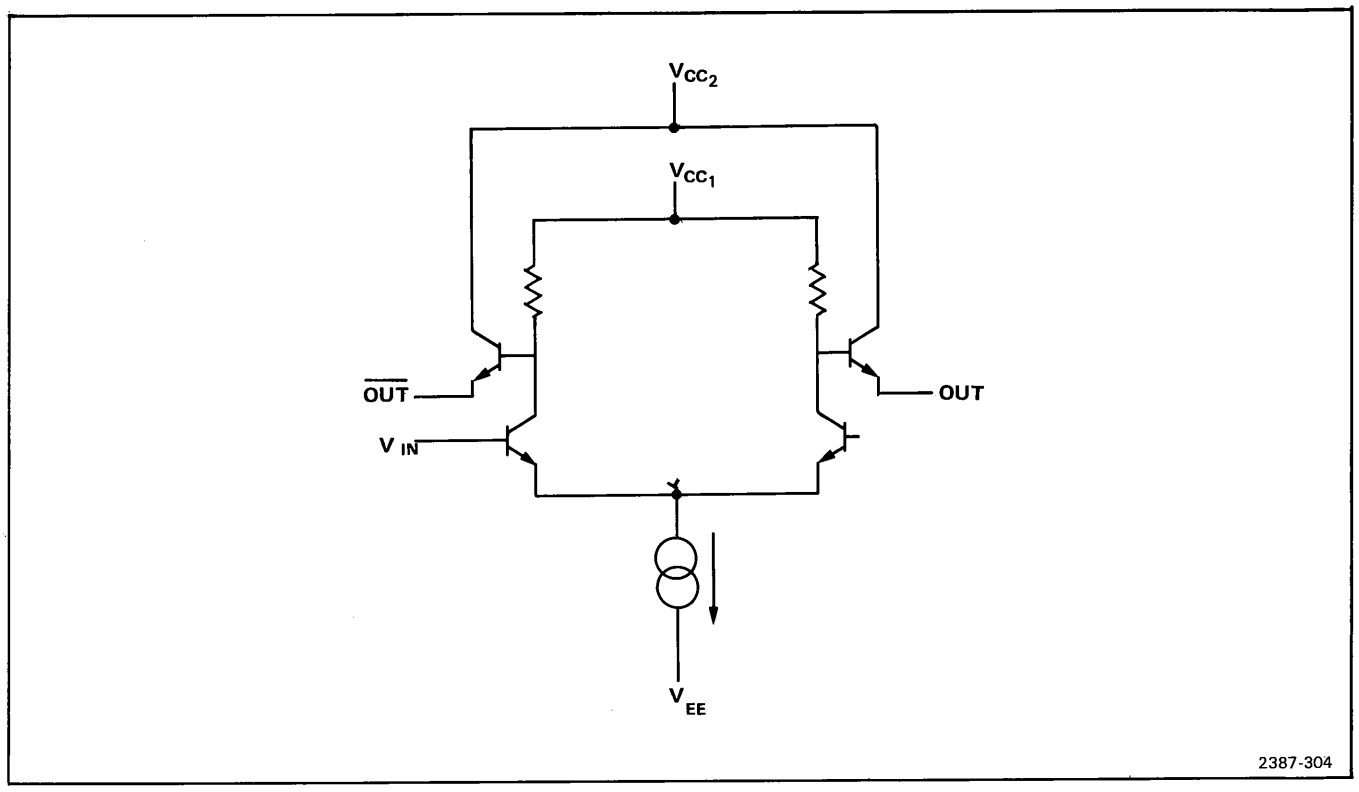


Figure 3-4. An ECL switch with emitter-follower buffers for level-shifting and current gain.

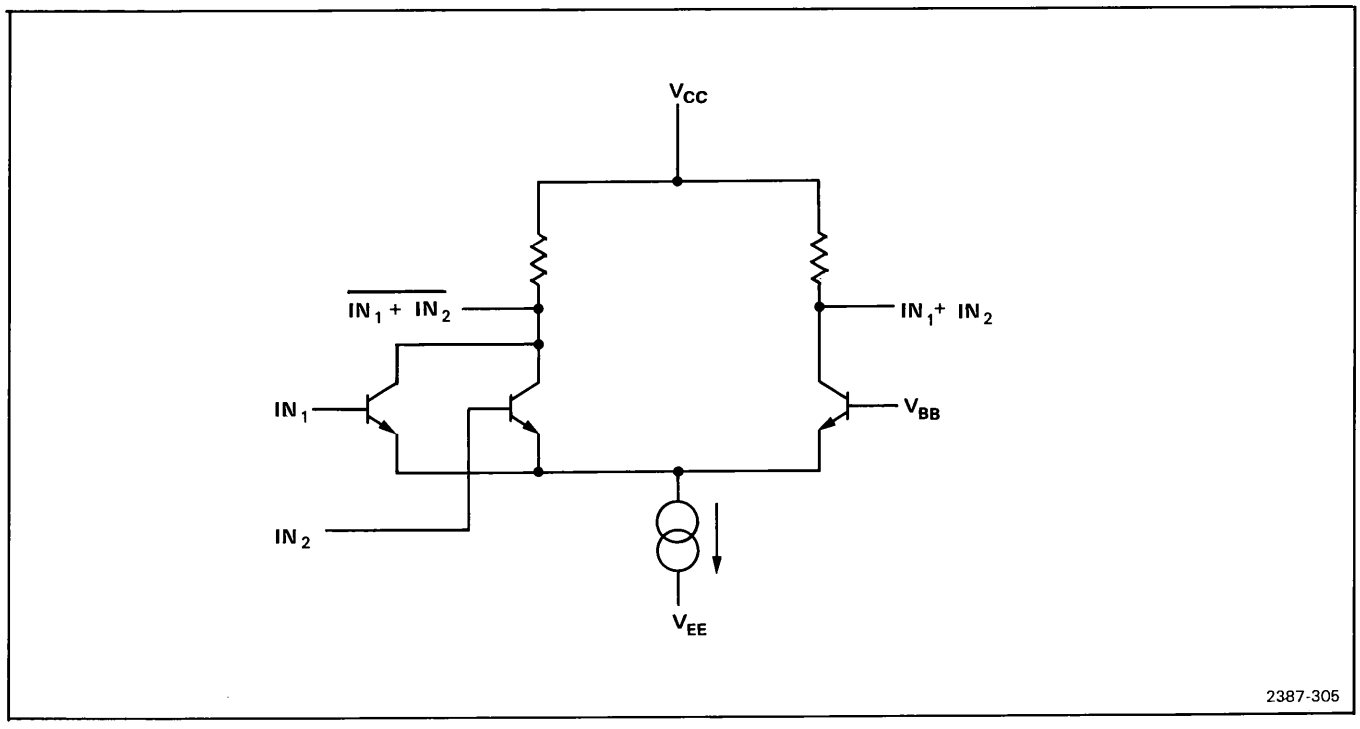


Figure 3-5. A simple ECL OR/NOR gate without output buffers.

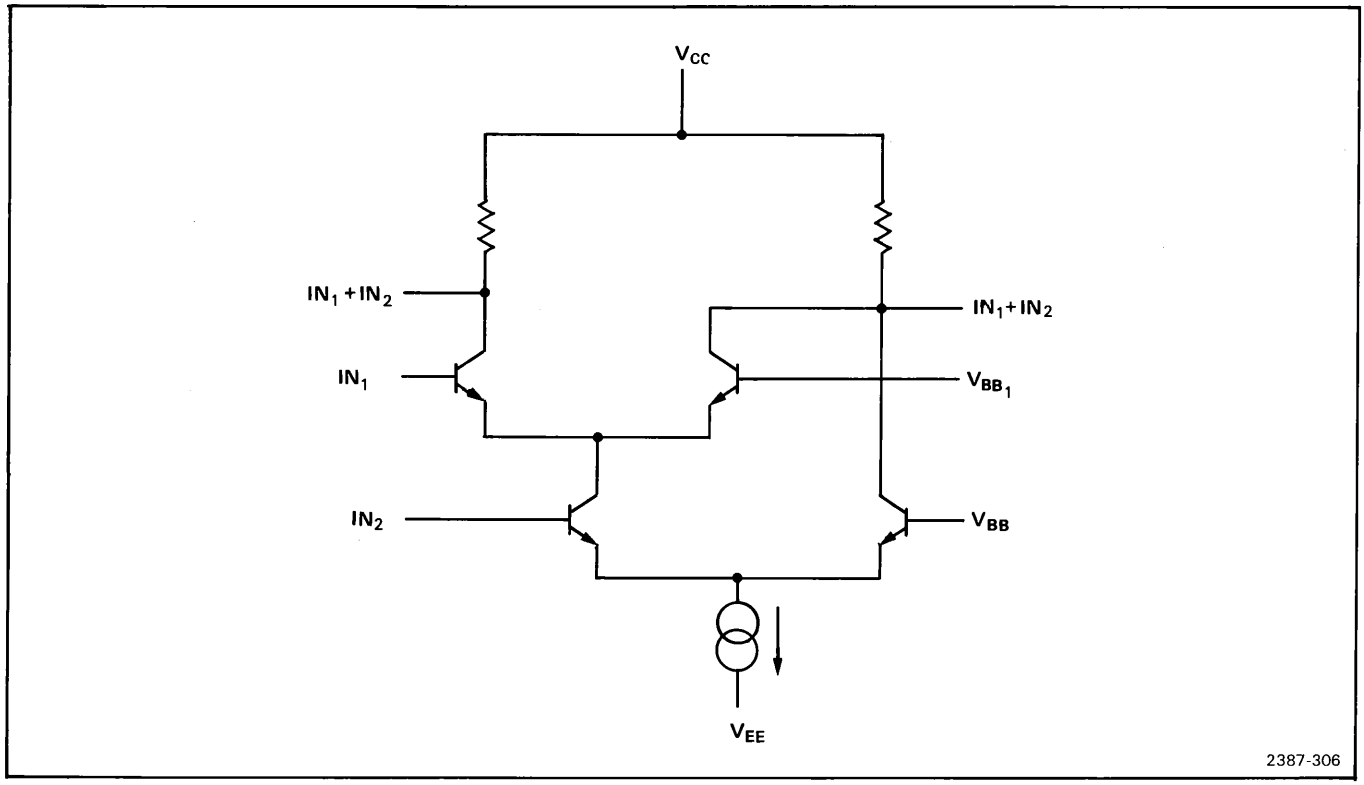


Figure 3-6. A simple ECL AND/NAND gate without output buffers.

In the case of the Data Storage Boards, the data input and output signal names shown on the schematic also depend on whether the board is plugged into an MSB (Most Significant Bits—bits 4-7) or an LSB (Least Significant Bits—bits 0-3) position. These cases are labeled on the schematics with a slash between the LSB and MSB signal names.

DETAILED CIRCUIT OPERATION

This part of the Theory of Operation section provides a detailed description of the electrical operation, and relationship of the circuits in the 7612D. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits commonly used in the electronics industry are not described in detail.

Complete schematic diagrams are provided in Section 8, Diagrams and Circuit Board Illustrations. The number inside the diamond preceding a heading in the following discussions refers to the schematic diagram for that circuit. The schematic digrams contain shaded borders around the major stages of the circuits to conveniently locate the components mentioned in the following discussions. The name of each stage is given in a shaded box on the diagram, and as a sub-heading in the discussion of the schematic diagram.

◇1 FRONT-PANEL DISPLAY

The MPU system drives the front-panel LEDs and lights and reads the front-panel switches. The front-panel circuitry is shown on diagrams 1 and 2.

The front-panel refresh and scan routines are interrupt driven. That is, the MPU (U222 on diagram 17) executes the refresh and scan routines when a front-panel interrupt (FPI) occurs. This interrupt is generated by the 555 timer, U858, and the associated components shown in the bottom left of diagram 1.

Timer U858 generates a five μs negative pulse about every three ms. The low on the output of U858 sets R-S flip-flop U756D and U756C, which asserts FPI (Front Panel Interrupt). The interrupt signals the MPU that it is time to refresh the front-panel LEDs and read the switches. If the interrupt is masked, such as when processing a message from the IEEE 488 bus, the MPU will ignore the FPI. Otherwise, it will store its current status and read the interrupt-occurred registers to find the source of the interrupt. When it finds FPI set, it will pass control to a firmware routine that resets interrupt FF U756C-D, refreshes the front-panel LEDs, and reads the front-panel switches.

REFRESHING THE FRONT-PANEL LEDs

There are six banks of front-panel LEDs, designated C,D,E,F,G, and H. On each front-panel interrupt, the MPU refreshes one bank of LEDs, so that all the LEDs are refreshed once for every six front-panel interrupts. Individual LEDs are selected by writing to a particular range of addresses. U848 decodes these addresses and selects the corresponding bank. Individual LEDs within a bank receive refresh data through the latches shown at the center of the diagram.

Table 3-1 shows the sequence in which LED banks are refreshed. On each interrupt, the low on pin 15 of multiplexer U848 will cause all its outputs to go low, turning all LEDs off. Then, data will be written sequentially into latches U338, U210, U424, and U724 at the addresses shown in the table. These addresses have common bit patterns in bits 2, 3, and 4. For example, if bits 2, 3, and 4 are 101, multiplexer U848 will decode bits 2, 3, and 4 and when the MPU enables U848 by asserting $\overline{\text{0D00 WRITE}}$, U848 will assert its pin 6 output, enabling $\overline{\text{LED}}$ bank C (DS102, DS402, DS606, and DS526). The data in the latches will activate the appropriate segments of each LED. When $\overline{\text{0D00 WRITE}}$ goes high, U848 will go to "memory mode," and hold its pin 6 output high. This output will stay high and the selected bank of LEDs will stay on until the next front-panel interrupt (FPI).

TABLE 3-1
Front-Panel LED Refresh Sequence

Write Latch		Latch Address During FPI Cycle					
		1	2	3	4	5	6
U338	1st	0D17	0D13	0D0F	0D0B	0D07	0D03
U210	2nd	0D16	0D12	0D0E	0D0A	0D06	0D02
U424	3rd	0D15	0D11	0D0D	0D09	0D05	0D01
U724	4th	0D14	0D10	0D0C	0D08	0D04	0D00

On the next front-panel interrupt the MPU will write data into the same latches, but at the addresses shown in column 2 of the table. This will cause U848 to select LED bank D (DS006, DS204, DS508, and DS620). The data written in the latches will refresh these LEDs. On the third interrupt, bank E will be selected; on the fourth, bank F, and so on until the seventh interrupt repeats the cycle. Figure 3-7 shows the timing for the refresh pulses.

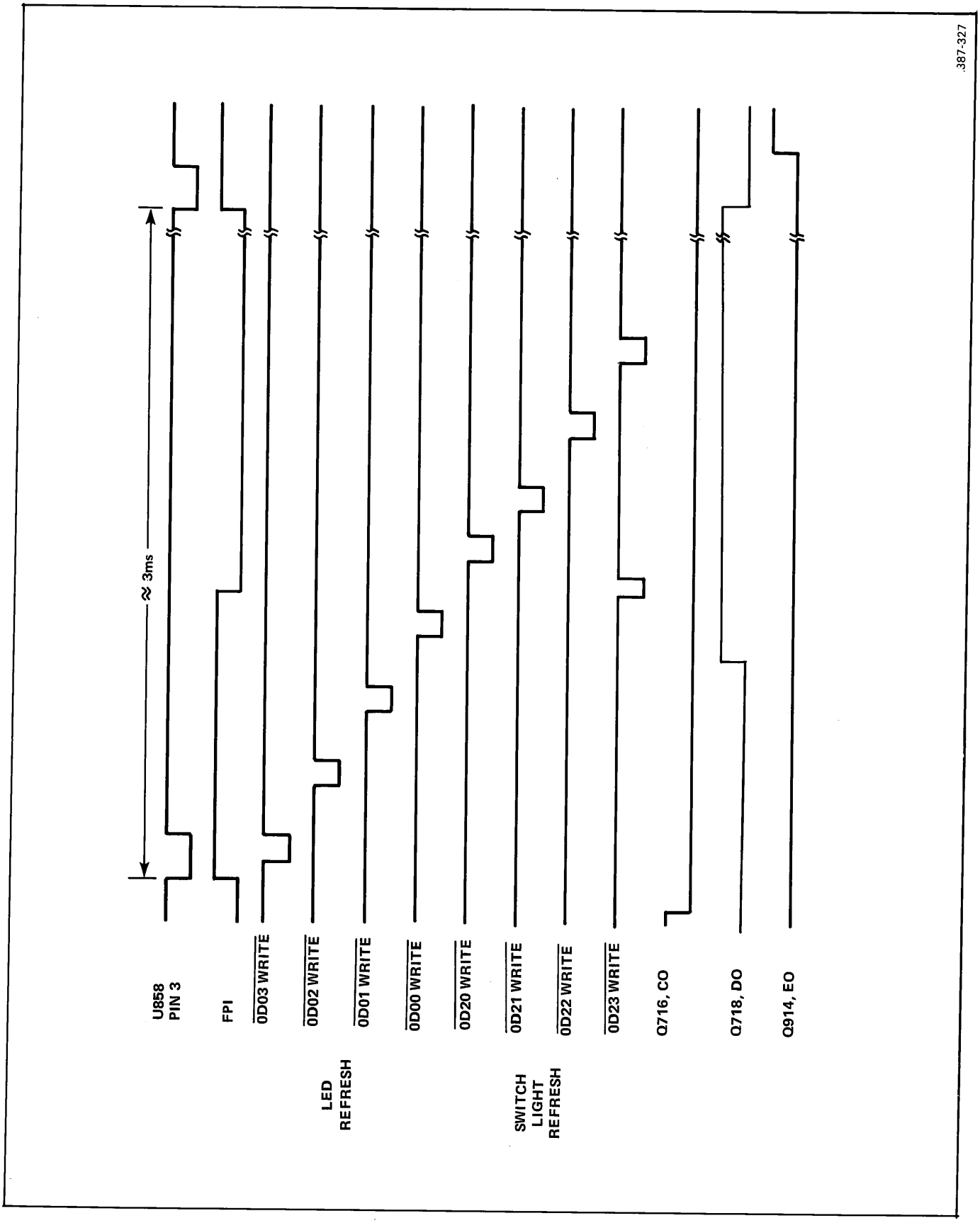


Figure 3-7. Timing of refresh pulses for front-panel indicators.

2 FRONT-PANEL SWITCHES

REFRESHING THE SWITCH LIGHTS

The lights that illuminate the front-panel switches are refreshed by the MPU. All lights are refreshed on each interrupt cycle. Data for the switch lights is latched by U124, U144, U154, and U638, shown at the left of diagram 2. The MPU directly turns any individual light on by setting the corresponding bit in the latch. For example, to turn the RECORD LENGTH light on, the MPU writes a data byte, with bit 3 set, into U124. The set bit causes the output of lamp driver U226D to go low, turning the lamp on.

SCANNING THE FRONT-PANEL SWITCHES

All the front-panel switches except ON-OFF are connected in a five-by-eight matrix as shown in Figure 3-8. The MPU checks for pressed buttons by asserting each of the select lines, $\overline{SD3}$-$\overline{SD7}$, one at a time, and reading the data bus through bidirectional bus drivers U358 and U452 at the left-center of diagram 1. Decoder U736 (bottom-left of diagram 2) decodes bits 2, 3, and 4 of the MPU address bus to generate the select lines. The scanning begins by reading data from address 0D00. U736 decodes the address and asserts SD7. If any button tied to the SD7 line is pressed, the corresponding data line(s) will go low. All other data lines are pulled high by R436B through J, shown on diagram 1.

For example, if the TRIGGER LEVEL button is pressed, the MPU will detect the pressed button on the next front-panel interrupt. The MPU reads data from 0D00, causing SD7 to go low. Because the TRIGGER LEVEL button is pressed, the low on SD7 causes $\overline{D00}$ to go low also. Because the MPU is reading data via the bidirectional bus drivers, U358 and U452 will be enabled to send data from the front-panel to the MPU bus. The MPU will detect the low on $\overline{D05}$, but to reduce the possibility of random noise simulating a pressed

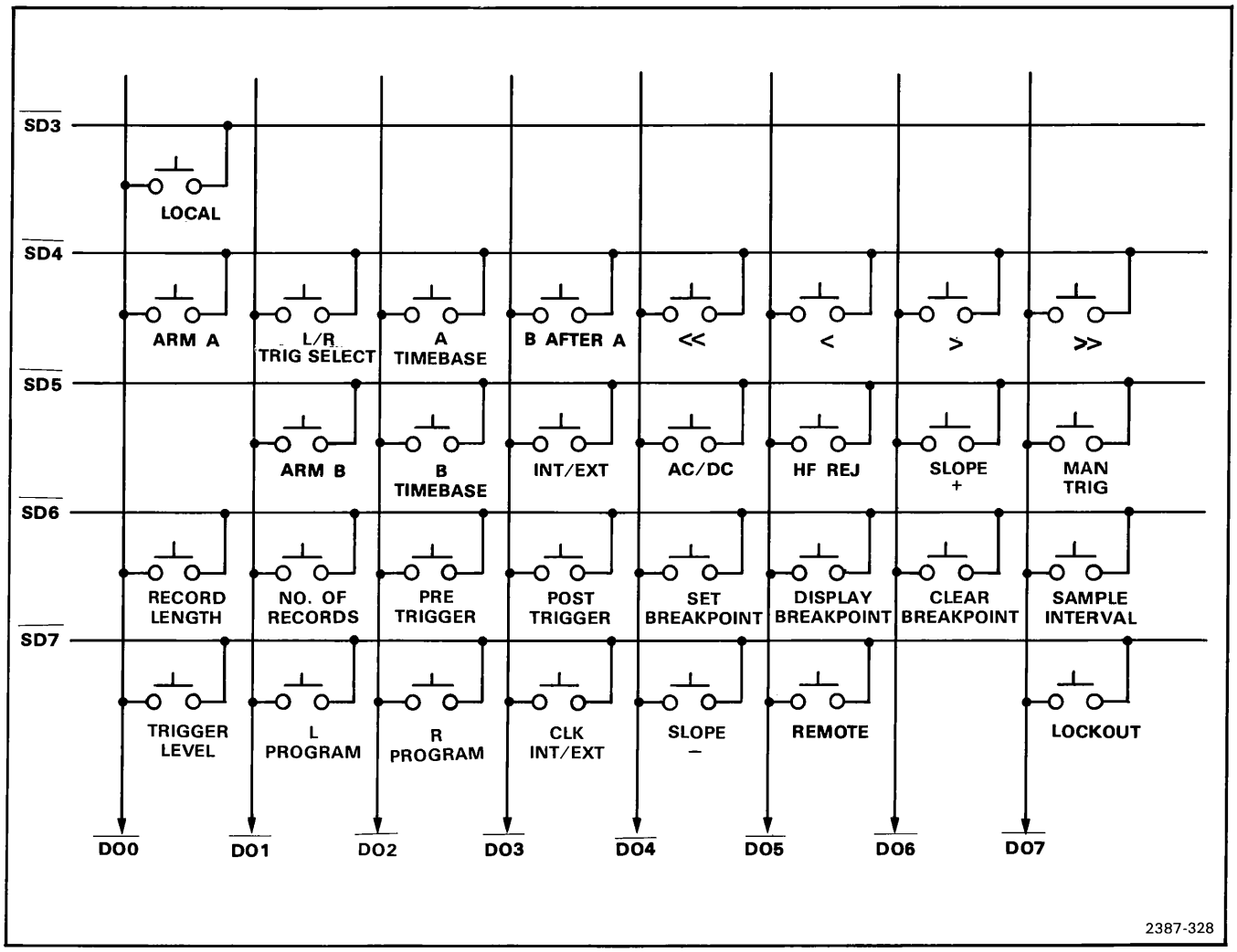


Figure 3-8. Five-by-eight matrix of front-panel switches.

button, no action will be taken until the next front-panel interrupt. If the button is still low on the next interrupt, about three ms later, it is assumed to be a valid front-panel input. The three-ms-scan period is fast enough that any normal front-panel input will be detected properly while random front-panel noise will be rejected.

The scanning process will continue through each of the select lines until all the front-panel switch data is read.

3 CLOCK BUFFER

The Clock Buffer produces four signals for the two Time Bases and two Headers, and a signal for external use. The signals are A:CLK and A:STB for Time Base A, B:CLK and B:STB for Time Base B, and CLK OUT for external use.

An internal oscillator or an external signal can serve as the source of the output signals.

Crystal Y200 is an oscillator which produces a 200 MHz output signal. Transistors Q114, Q122, Q214, and Q222 buffer the 200 MHz signal.

The level on the ECKSL line controls the signal-select gating. When ECKSL is low it enables U320B and inhibits U410A via U320A. Gate U320B will then respond to the oscillator signal, and U410A will ignore any Ext Clk In signal. When the ECKSL line is high U410A will respond to Ext Clk In signals and U320B will ignore the oscillator signal.

The output of U410A or U320B goes via inverters U410B, U410E, and U320E to gates that produce the individual output signals.

Strap P510, in the lower-right of diagram 3, can disable the signals that drive the hybrid comparators. When P510 is set to the Cal position, it grounds the pin 17 inputs of U320C and U410C, disabling their outputs and inhibiting the strobe drivers.

4 HEADER

There are two Header Boards. Each board attaches to one of the EBS tubes. The Header Board senses the output of the EBS tube and activates eight serial data lines to represent that output. The eight data lines connect to the Memory Boards.

HYBRID SUPPLY

The Hybrid comparators require regulated −6.5 V for target bias and comparator reference, and −12 V to operate the comparators. The circuit at the top of diagram 4 generates these voltages.

The −15 V power supply connects to pin 2 of chassis-mounted 12 V regulator, U5559, in the top-left corner of diagram 4. This regulator generates the −12 V for the Hybrid Comparators. The output from pin 3 of the regulator also goes to the input of a −5 V regulator, U314. The reference pin of U314 (pin 1) is tied to the junction of voltage divider R320 and R322. The voltage at this divider lowers the regulator's reference pin to −1.25 V, setting the output of the regulator to −6.5 V.

TARGET AND COMPARATORS

The EBS target consists of 10 diodes (eight for data and two for setting and checking beam alignment) shown near the center of diagram 4. Figure 3-9 shows a simplified schematic of one target diode and its comparator. The diodes are reverse-biased with 11.5 V from the +5 V and −6.5V supplies. When the 10 kV electron beam strikes an exposed portion of a diode stripe, it creates a number of electron-hole pairs in the target diode, which produces an output current corresponding to a target gain of about 2000. This current causes the target input of the comparator to rise about 200 mV from its quiescent −6.5 V level. The comparator senses this change and when the STB lines are asserted, the comparator latches, asserting its differential outputs.

The other input of each comparator is connected to a reference voltage divider that is adjustable to match the comparator thresholds and thus, the relative size and symmetry of each bit.

Diagram 4 shows only the complete Header assembly for channel B. The channel A Header assembly is identical.

5 TIME-BASE CONTROL

The Time-Base Control circuitry produces control signals for the A and B Time Bases. The Address Decoder, on the left part of the diagram, produces "setup" signals for the time bases. The circuitry on the right side of the diagram is the Data Transmitter, which tells the MPU where to find data and how much of it to transmit.

ADDRESS DECODER

The Address Decoder receives address data and control signals from the MPU and produces one setup signal for the Time Base for each read or write operation at the selected address. The Address Decoder also produces the A:PGM and B:PGM signals, which select the A or B Time Base for operation.

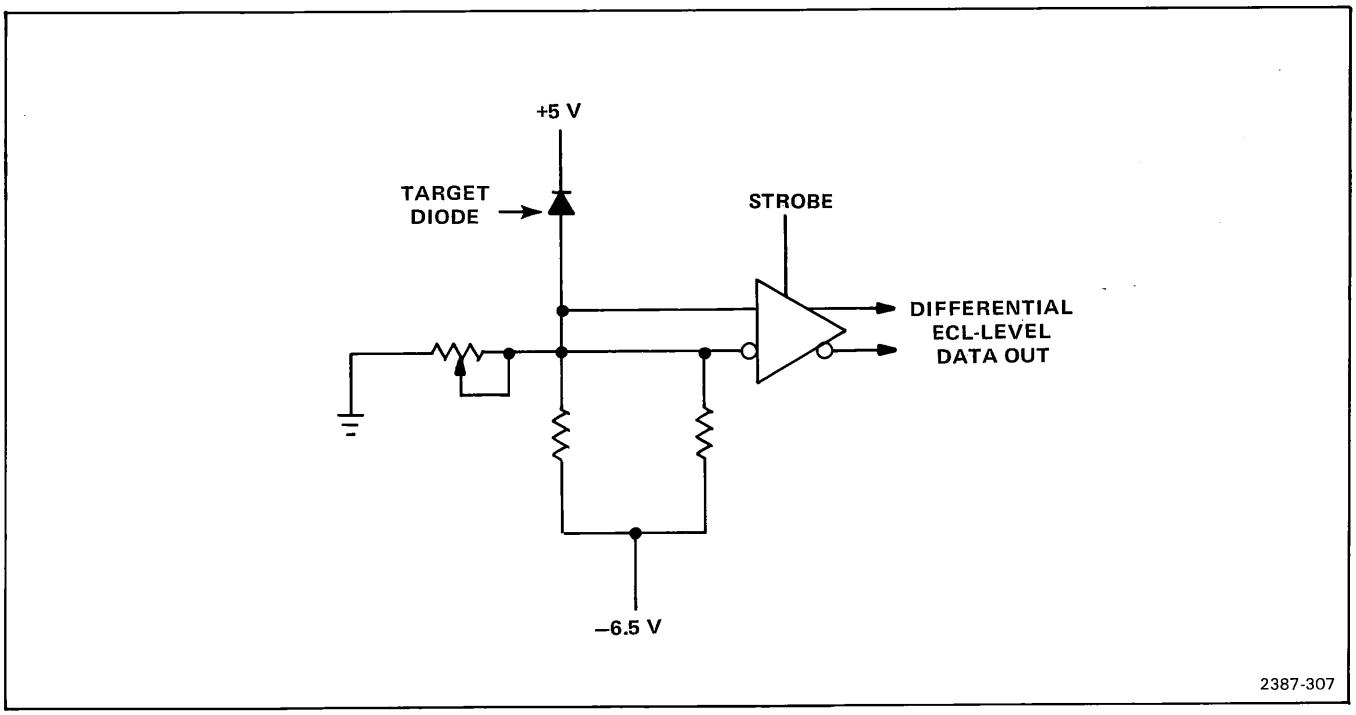


Figure 3-9. A simplified schematic diagram of one target diode and comparator.

The Address Decoder receives six address bits (BADR0-BADR5) and four control signals from the MPU.

A low level on $\overline{\text{TLTRSEL}}$ will enable U600A and U600B. Then a high level on BADR5 will activate U600A, which will enable decoder U210. Similarly, BADR4 will activate U600B, which will enable decoder U710.

A low level on BR/$\overline{\text{W}}$ will enable U600C, and $\overline{\text{Strobe}}$ pulses will then activate U930E. The low output of U930E will then activate the enabled decoder, U210 or U710, which will assert a low level on one of its output lines for the duration of $\overline{\text{Strobe}}$ (about 100 ns). If the BR/$\overline{\text{W}}$ line is high, the output of U930E will be low, and the selected decoder output will be low for the entire time the address is selected (about 500 ns).

Level shifters U010, U100, U110, and U200 change the decoder outputs to ECL logic levels, and invert their inputs, in some cases. Whenever U710 asserts a low level on its 0DA0 line it will clock latch U500, which will store the levels on the BD2 and BD3 lines. Level shifter U400 will pass the outputs of U500, and the HASD level, to its output as ECL-level signals A:PGM (BD3), B:PGM (BD2), A:SEL (HASD), and B:SEL ($\overline{\text{HASD}}$), respectively.

The MPUCLK signal clocks the $\overline{\text{HRD}}$ level into FF U900A, and level shifter U300 changes U900A's output to the $\overline{\text{A:RD}}$ and $\overline{\text{B:RD}}$ signals.

DATA TRANSMITTER

The Data Transmitter produces six control signals ($\overline{\text{L Send}}$, HRD, XMTI, A:AQI, B:AQI, and MPUCLK) for other parts of the 7612D. The Data Transmitter has three groups of circuitry, the Clock Generator, the Counter, and the Logic circuits.

MPU CLOCK GENERATOR

Oscillator U130 and related components produce the 10 MHz clock signal. Level-shifter U230 changes the clock signal to the TTL-level MPUCLK signal.

COUNTER

Three presettable up/down counters, U810, U820, and U830 function as the Counter.

In a two-step operation, the counter will receive data from the MPU via the BD bus. First, the $\overline{\text{CNTR}}$ signal will load the BD0-BD7 data word into U830 and U820. Next, the $\overline{\text{CTRL}}$ signal will load the less-significant four bits (BD0-BD3) of the subsequent data word into U810.

Pulses from U1020A will then decrement U830. When the numerical count in U830 reaches zero, its TC line will go high. The high from U830's TC output will enable U820 via U930F. Subsequent pulses from U1020A will decrement U820 until it reaches a zero count and asserts a high on its

TC output. At that point the two high levels, from the TC outputs of U830 and U820, will activate U920A. Gate U920A will then apply a low to U810's enable input. Pulses from FF U1020A will decrement U810 until it reaches a count of zero, when, via U910B, the output of the counter will stop the Data Transmitter.

LOGIC

The Logic circuit generates six control signals for other parts of the 7612D. The circuit has two modes of operation, transmit mode and skip mode.

Transmit Mode

In skip mode, the Logic circuit immediately produces $\overline{HRD}$, which goes to the Time Base circuitry as $\overline{A:RD}$ or $\overline{B:RD}$ via U900A and U300. These signals cause the Time Base to skip a predetermined amount of data. In transmit mode, FF U1020A will follow the Y Sent signal, and U1020A's output will activate U600D to produce $\overline{L\ Send}$ and $\overline{HRD}$ signals.

An operation to transmit three words will be described here. Figure 3-10 shows the timing of the transmit operation. Before the operation starts, a low on $\overline{RST}$ will reset FFs U1020A and U1020B. A low level from U700 pin 15 will set the Logic circuit to transmit mode, and the Y Sent line will be at a low level.

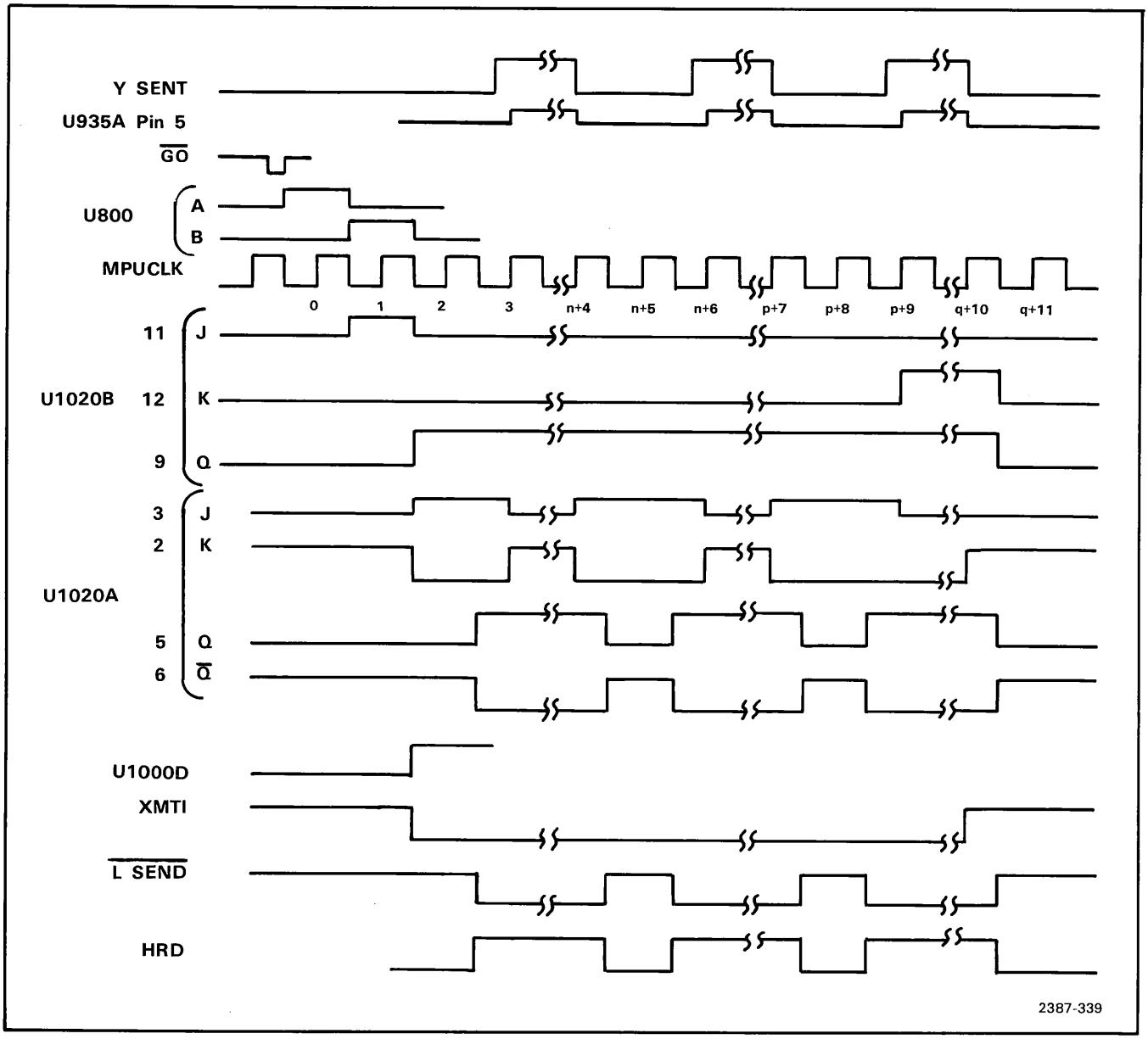


Figure 3-10. Timing of three-word transmit operation.

Action commences with a $\overline{Go}$ pulse. The trailing, positive transition of $\overline{Go}$ will clock U800A, which will assert a high level at the D input of U800B. The next MPUCLK (#0) will cause U800B to assert a high level, via U1030B and U930C, at the J input of U1020B.

The next MPUCLK (#1) will "set" U1020B, which will assert a high level on its pin 9 output. The high level from U1020B has the following effects:

a. It activates U1030D, whose low output will disable U1030C which will assert a high at U1020A's J input.

b. It activates U910A, which will assert a low at U1020A's K input.

The low from U1020B pin 7 will disable U1000D, which, via U730C, will produce a low on the XMTI line.

The second MPUCLK pulse will "set" U1020A, which will assert a high on its pin 5 output. The high from U1020A pin 5 will activate U1000B, which, via U730D, will assert a high on the HRD line. At the same time, the low from U1020A pin 6 will activate U600D, which will assert a low level on the $\overline{L\ Send}$ line.

The third MPUCLK will not cause FF's U1020A and U1020B to change states. In this example the Y Sent line will be high before MPUCLK #3 occurs. The positive transition of MPUCLK #3 will latch the high Y Sent level into U935A, which will assert a high on its Q output. This high will disable U1030D via U930C, and U1030D's high output will activate U1030C. When active, U1030C will apply a low to U1020A's J input. The high from U935A will activate U920C, whose low output will disable U910A. When disabled, U910A will apply a high to U1020A's K input.

Because the duration of the Y Sent pulses depends on the device(s) receiving the data, we cannot predict how many MPUCLK pulses will occur in that time. Instead, we call that number n after the first Y Sent pulse, p after the second Y Sent pulse, and q after the third Y Sent pulse (See Figure 3-10.)

The fourth MPUCLK will cause U1020A to reset because its J,K inputs are at 0,1 levels. Also, because U935A no longer is applying a high to U930C and U920C, U1020A's J and K inputs will be at 1,0 levels. When U1020A is reset, the HRD and L Send pulses will end.

The fifth MPUCLK will set U1020A just as MPUCLK #2 did. This will initiate the second HRD and [not]L Send] pulses.

The sixth MPUCLK will be a repeat of MPUCLK #3. It will clock Y Sent into U935A, which will cause U1020A's J and K inputs to be 0,1.

The seventh MPUCLK will reset U1020A, ending the second HRD and L Send pulses.

The eighth MPUCLK will set U1020A, which will initiate the third HRD and $\overline{L\ Send}$ pulses. The third HRD pulse will clock the low level from U910B into FF U900B (U910B sensed that the counter was at zero just after the second HRD pulse). Flip-flop U900B will assert a high on its pin 8 output, which will enable U1010C.

The ninth MPUCLK will cause two changes, as follows: 1) It will latch the third Y Sent level into U935A, which will assert a high on its output. This high will activate U1010C, whose low output will disable U920D. When disabled, U920D will apply a high to U1020B's K input. 2) The high from U935A will, via U930C, disable U1030D, whose high output will activate U1030C. When active, U1030C will apply a low to U1020A's J input.

The tenth MPUCLK will reset U1020B because its J and K inputs are at 0,1 levels. The low from U1020B pin 9 will disable U910A which will apply a high to U1020A's K input.

The eleventh MPUCLK will reset U1020A, and the sequence will end. The Logic circuit will have produced three HRD and $\overline{L\ Send}$ pulses to cause the MPU to send three data words.

Skip Mode

In skip mode, the Logic circuit will produce a predetermined number of $\overline{HRD}$ pulses but no $\overline{L\ Send}$ pulses. This causes the MPU to shift its index point, or skip, to a new location.

In skip mode FF U1020A is toggled by MPUCLK pulses. The pin 5 output of U1020A will decrement the counter. A skip operation is faster than a transmit operation of equal length because the skip operation does not depend on a Y Sent response from the IEEE 488 Handshake or XYZ Display circuitry.

An operation to skip three words will be described here. Figure 3-11 shows the timing of the skip operation.

Skip mode starts with the following conditions:

- Flip-flops U1020A and U2020B will be reset,
- The pin 15 output of U700 will be high.
- The Y Sent line will be low.
- The TC outputs of counters U810, U820, and U830 will be at low levels.

The pin 6 output of U910B will be high because the content of the counter is not zero.

A positive transition on $\overline{Go}$ will trigger FF U800A, which will put a high level at the D input of U800B. The next MPUCLK (#1) will cause U800B to produce two outputs, as follows: 1) The high output from pin 9 will activate U1030B, and 2)

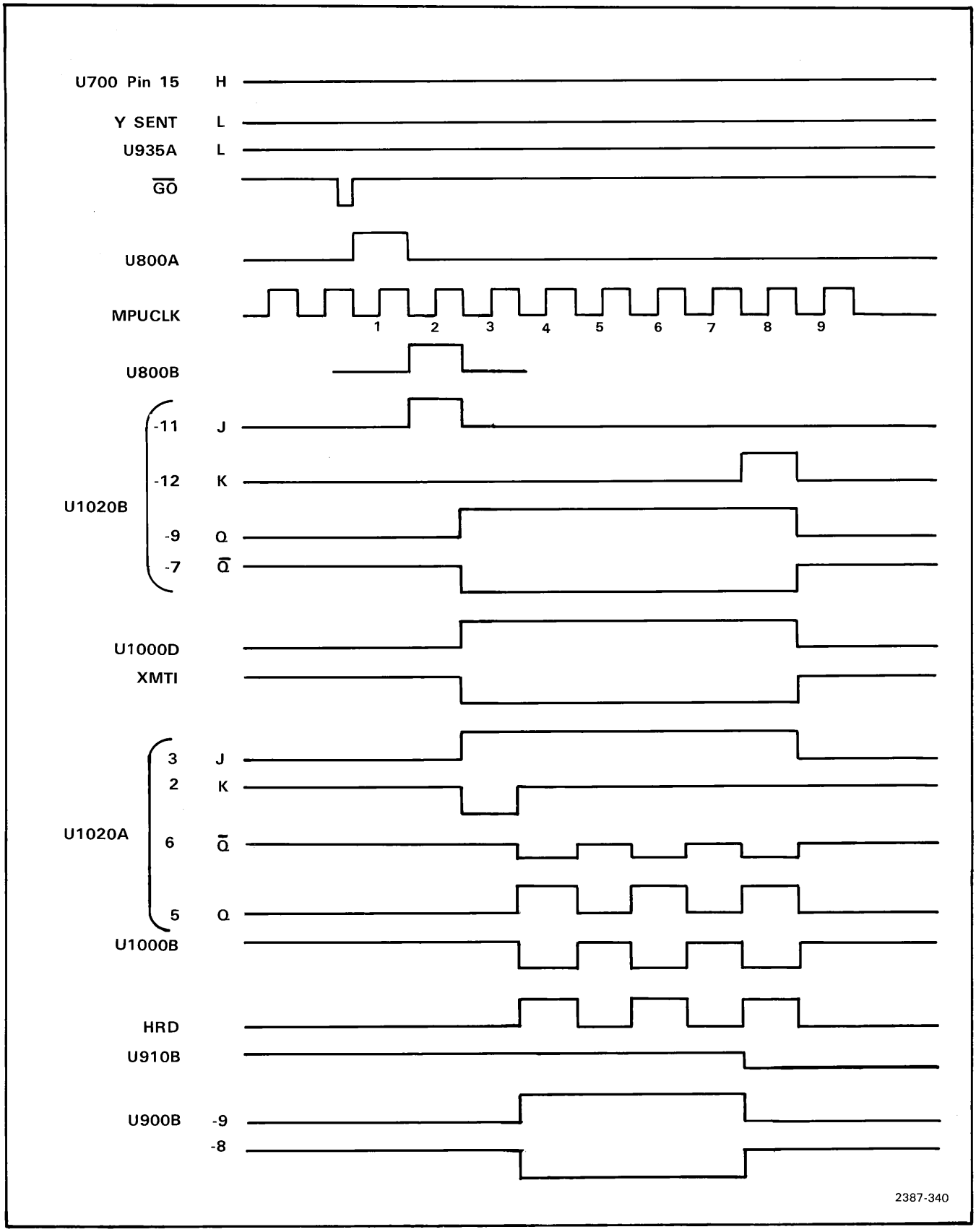


Figure 3-11. Timing of a three-word skip operation.

the low output from pin 8 will clear U800A. The output of U1030B will become a high at U1020B's J input. The K input of U1020B will be low because the low from U1020A pin 5 will disable U1010B and C, and their two high outputs will activate U920D.

The second MPUCLK will have three effects, as follows: 1) It will cause U1020B to set its Q output high, 2) it will remove the high from U1020B's J input by clocking the low input into U800B, and 3) the low from U1020B pin 7 will disable U1000D. Gate U1000D will then cause a low level on the XMTI line via U730C. Immediately after MPUCLK #2, the high on U1020B pin 9 will activate U1030A and D and U910A. When either U1030A or D is active, its low output will disable U1030C, which will then assert a high on U1020A's J input. When activated, U910A will apply a low level to U1020A's K input.

The third MPUCLK will have no effect on U1020B because its J and K inputs will be low. However, MPUCLK #3 will set U1020A (because its J and K inputs are 1,0), which will produce a high output on pin 5 that will clock the counter. The outputs from U1020A and U1020B will activate U1000B, which will assert a high on HRD via U730D. This positive transition on HRD will clock the high level from U910B into U900B. The high from U900B will activate U920B, which will disable U910A and apply a high level to U1020A's K input.

The fourth MPUCLK will toggle U1020A, whose Q output will go low. The low from U1020A pin 5 will disable U1000B, which will cause a low level on HRD via U730D.

The fifth and sixth MPUCLKs will cause repeats of the action caused by the third and fourth MPUCLKs, except that U900B will not change states when MPUCLK #5 causes HRD to go positive.

In this example, the counter reaches zero when it receives the third pulse from U1020A pin 5, which occurs at MPUCLK #7. Counters U810, U820, and U830 will apply their high outputs to U910B, which will activate it. Gate U910B then will produce a low that HRD will clock into U900B. Flip-flop U900B will assert a high level on its pin 8 output, which will activate U1010B. The low from U1010B will disable U920D, which will apply a high level to the K input of U1020B.

The eighth MPUCLK will cause: 1) U1020A to toggle again (its Q output will then be a low that will disable U1010B), and 2) U1020B to reset. The low from U1020B pin 9 will disable U1030A and U1030D, whose high outputs will activate U1030C to apply a low to U1020A's J input. The low from U1020A pin 5 will disable U1010B and C; their high outputs will activate U920D. The activated U920D will apply a low to U1020B's K input. The low levels from U1020A and B will disable U1000B, which via U730D, will return the HRD line to a low. Because U930C is inverting the low Y Sent input and U1020B's pin 7 output is high, U1000D will be activated and cause a high on the XMTI line. The skip operation is now complete.

6 CODE CONVERTER/CHECK-SUM GENERATOR

As its name indicates, this diagram shows two circuits. The Code Converter consists of the seven gates and two level shifters at the left side of the diagram. The rest of the circuitry is the Check Sum Generator. Figure 3-12 is a block diagram of the Code Converter/Check-Sum Generator.

CODE CONVERTER

Exclusive-or gates U330 and U430 receive the gray-coded DO0-DO7 bits from the Data Memory, and convert the data to binary code. The binary-coded data is level-shifted by U320 and U420 and applied to the hardware data (HD) bus and to one input of adders U310 and U410.

CHECK-SUM GENERATOR

Check-Sum Generator accumulates a modulo-256 sum of the data bytes passed to the IEEE 488 interface for transmission. Eight-bit full adder, U310 and U410, sums the result of each addition with the next byte. U510 and U610 latch the result of the addition and feed the result back to the adder for summing with the data byte.

Because no carry is accumulated from U510, the sum "wraps around" to zero when it reaches 256. The result is called a modulo-256 sum of the data bytes.

When all bytes are transmitted, the MPU reads the checksum result from latches U520 and U620 by asserting CKSM.

Inverters U720 and U730 invert the BD data and send it to the Counter in the Time-Base Control circuit, and to the time bases through level shifters U020 and U120 for use in programming the time bases.

7 DATA MEMORY

One Data Memory Board stores half the data from the EBS tube target. Together, two Data Memory Boards store all the bits from one EBS tube.

Each memory board has eight RAMs. Each RAM will store up to 256 four-bit words, for a total of 2048 four-bit words. Each channel has two memory boards, and can store up to 2048 eight-bit words.

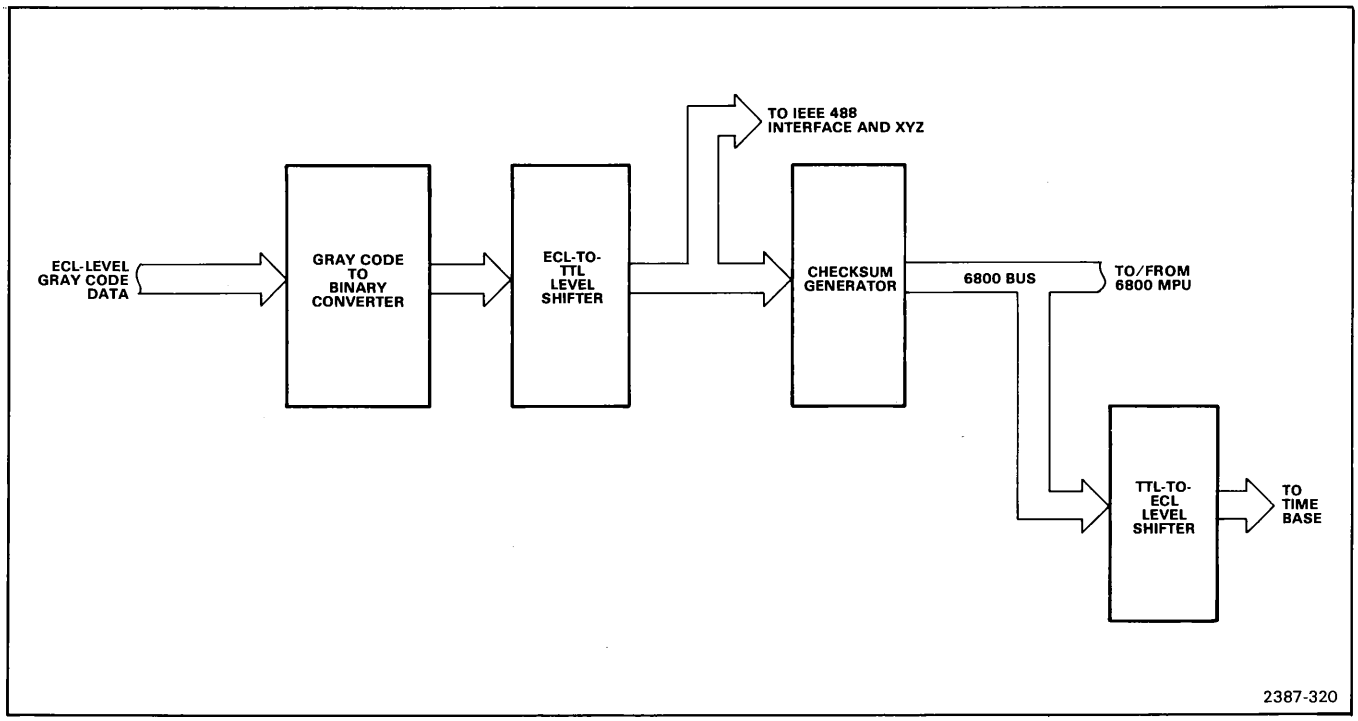


Figure 3-12. Block diagram of the code converter/checksum generator.

HIGH-SPEED SHIFT REGISTERS

Waveform data comes from the Hybrid Comparators at a constant five ns rate, but the memory chips used in the data memory cannot accept and store data at this rate. The high-speed shift registers accept data in a serial fashion, collect eight samples, and then transfer these eight samples in parallel to the memory. As a result, the data rate into the memory is reduced by a factor of eight. With five ns sampling, for example, data is written into the memory every 40 ns.

Differential data from the hybrid comparators is received and converted to single-ended by the four line receivers, U232A through D, shown at the left side of diagram 7. Resistors R138B through J terminate the differential lines. The single-ended data is fed into the serial inputs of shift registers U202, U212, U222, and U224. Data is clocked into the registers at the selected sampling interval by the BFTB and $\overline{\text{BFTB}}$ (Buffered Time Base) signals. Only the selected samples are clocked into the shift registers. If, for example, a 20 ns sampling interval is programmed for this segment, the output of U836B goes high every 20 ns, clocking every fourth sample into the shift registers. Each time a sample is shifted that sample appears on the first parallel output (pin 14) of the register, and all preceding samples are shifted toward the last output (pin 5) by one bit.

WRITING TO THE MEMORY

When eight samples have been collected, $\overline{\text{BFTB/8}}$ is asserted and the parallel outputs of the shift registers are latched by registers U302, U312, U322, and U324. Four sample intervals after the data is latched in these registers, WE goes low. The eight samples are written into the memory at the address supplied by the time base.

During the write process, the $\overline{\text{CS0}}$-$\overline{\text{CS7}}$ (Chip Select) lines are all asserted (except while writing the last group of eight samples). This enables all the memory chips to receive data. We discuss the special case of writing the last group of eight samples in the description of the Time Base under the "trigger locator circuit".

DATA STORAGE FORMAT

Each of the high-speed shift registers collects groups of eight samples from a single data bit. When the data is transferred to the memory chips, each chip stores four bits of a single sample from this group of eight samples (see Figure 3-13). For example, U416 stores four bits of the first sample taken in each group of eight samples. If the memory board is plugged into an MSB position, it stores the four most significant bits of these samples. If the board is plugged into an LSB position, the chip stores the four low-order bits. Figure 3-14 illustrates the format of data stored in the waveform memory.

The time base begins storing data in memory as soon as the ARM operation is complete. When the trigger occurs and when the acquisition is complete, the time base stores the memory address where each record is written. When the data is read, this address is used to recover the data from

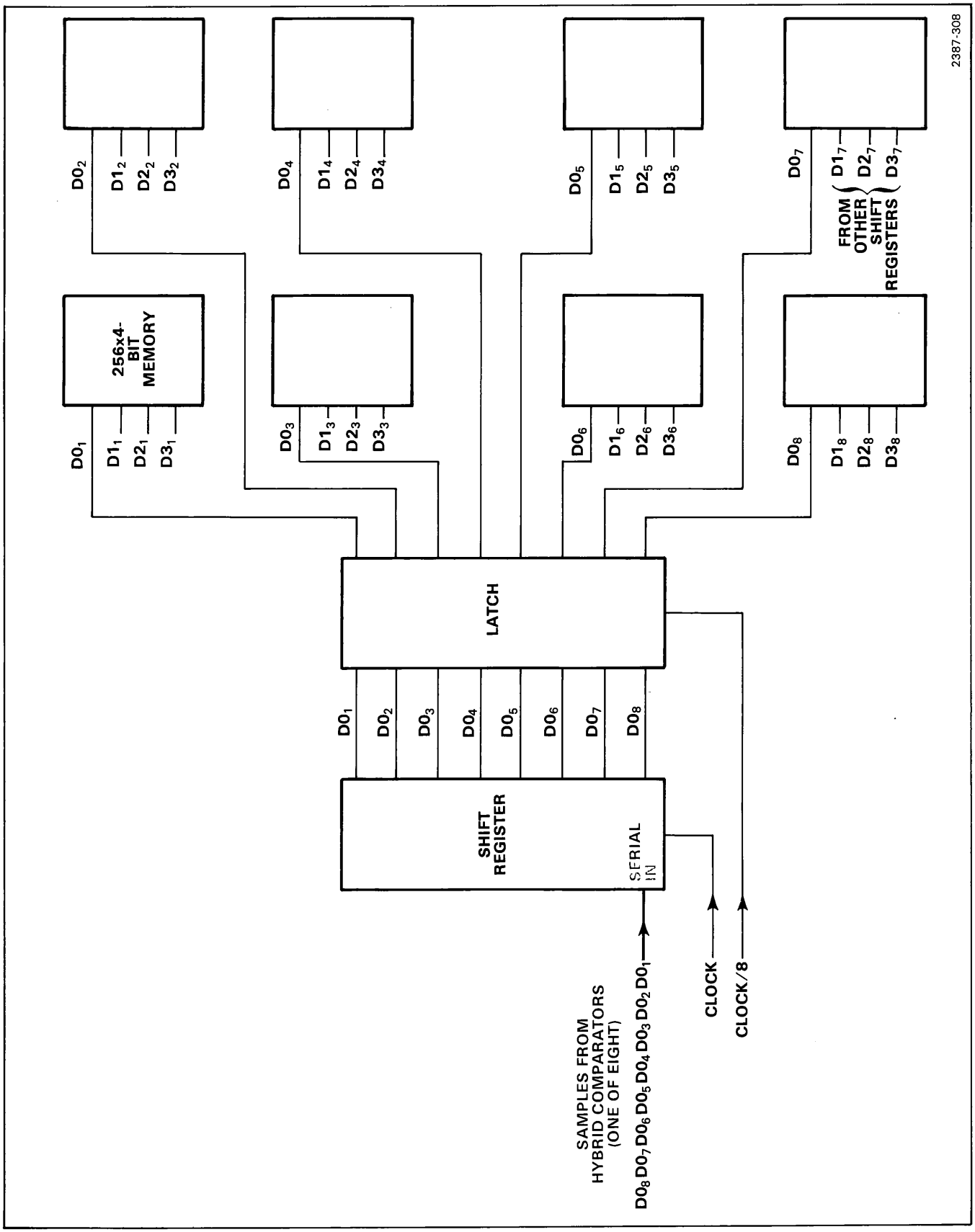


Figure 3-13. The shift register, latch, and data memory for eight samples of data bit Ø.

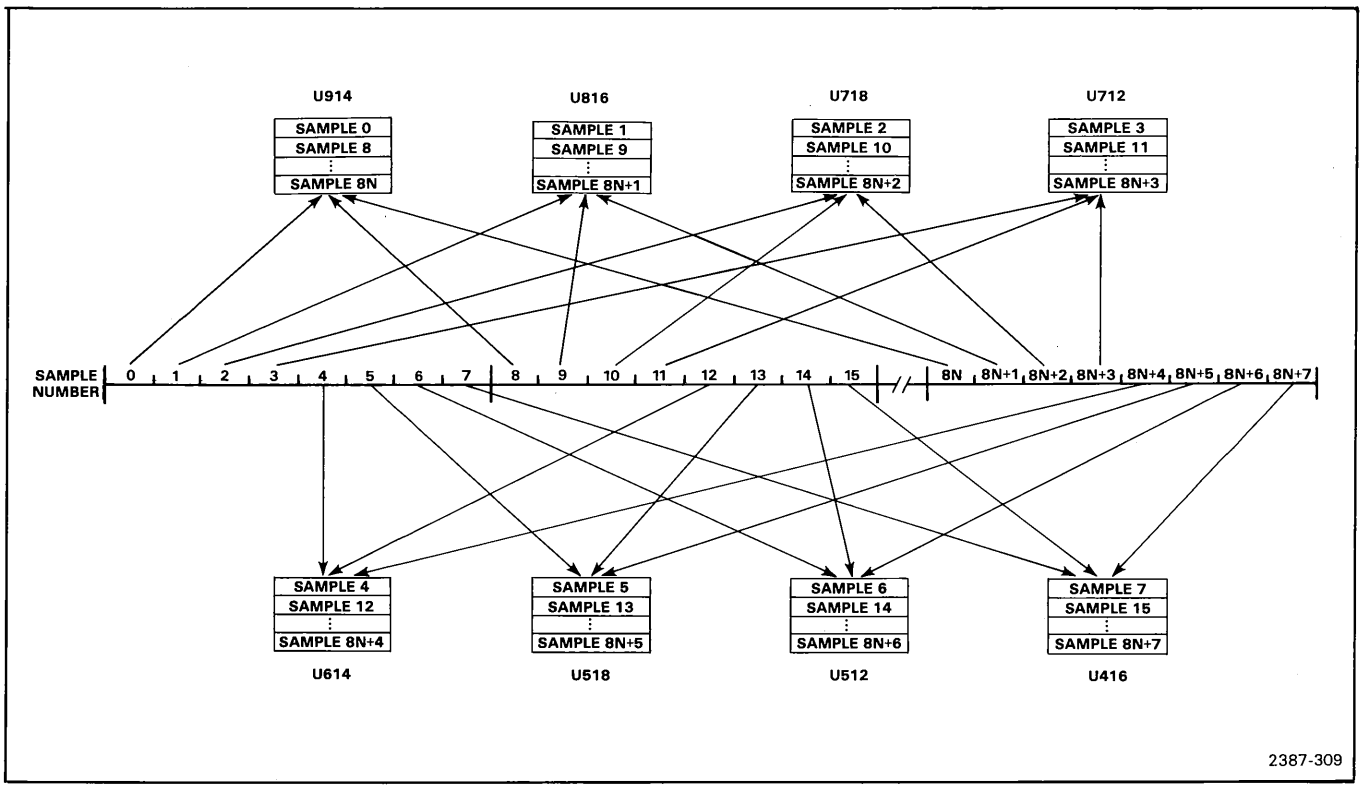


Figure 3-14. Data storage format for one Data Memory Board (four bits).

the memory. The time base also "unleaves" the data in memory from the format illustrated in Figure 3-14 by selecting corresponding chips on the MSB and LSB memory boards, one pair at a time, to reconstruct the original order in which the data was written.

Let's look at an example to clarify this data storage technique. Assume that time base A is set to acquire two 1024-point records with 256 samples of pre-trigger in each record. When the ARM A button is pressed or the ARM A command is received, the MPU checks the settings and loads them into the time-base hardware. As soon as the loading operation is complete, the time base begins acquiring pre-trigger data. Figure 3-15 shows data being written into the memory, illustrated as a circular buffer.

In pre-trigger mode, the time base ignores triggers until the circular buffer is completely filled. When the buffer is filled, triggers are accepted. The time base continues to acquire data, overwriting old data until a valid trigger is received and enough additional samples are taken to complete the record. In our example, 768 samples (1024-256) are acquired after the trigger. This leaves the memory with 256 samples stored before the trigger and 768 samples stored after the trigger as shown in Figure 3-15.

Figure 3-16 shows the sequence of events when storing data in B Triggers After A mode.

Figure 3-17 illustrates the storage of data in post-trigger mode. In this mode, triggers are accepted immediately after arming occurs. When a valid trigger is received, the time base begins counting samples. The acquisition is complete when the record length plus the number of post-trigger samples have been acquired. The first n samples (where n is the number of post-trigger samples) are overwritten with the end of the record. As a result, the start of the record is delayed by the number of post-trigger samples selected.

DATA AND ADDRESS BUFFERS

The data memory address bus (DADR0-7) is buffered by U532A-C, U436A-B, and U436D-F. These buffers are always enabled. The data bus (DO0-7) is buffered by U538A-D. These buffers are enabled only when the microprocessor selects the channel to be read by asserting A:SEL or B:SEL (shown as SEL on the schematic).

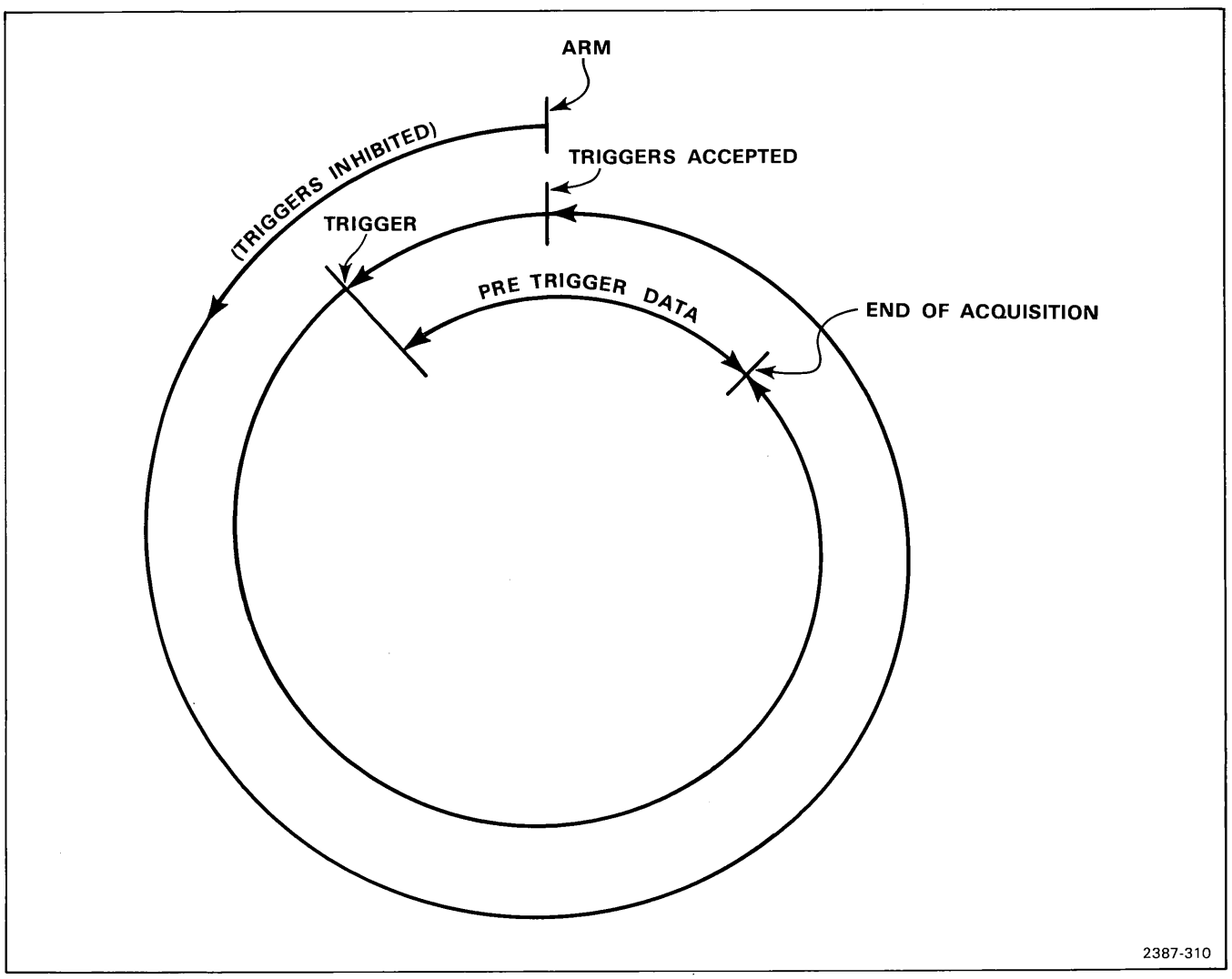


Figure 3-15. Data storage in pre-trigger mode.

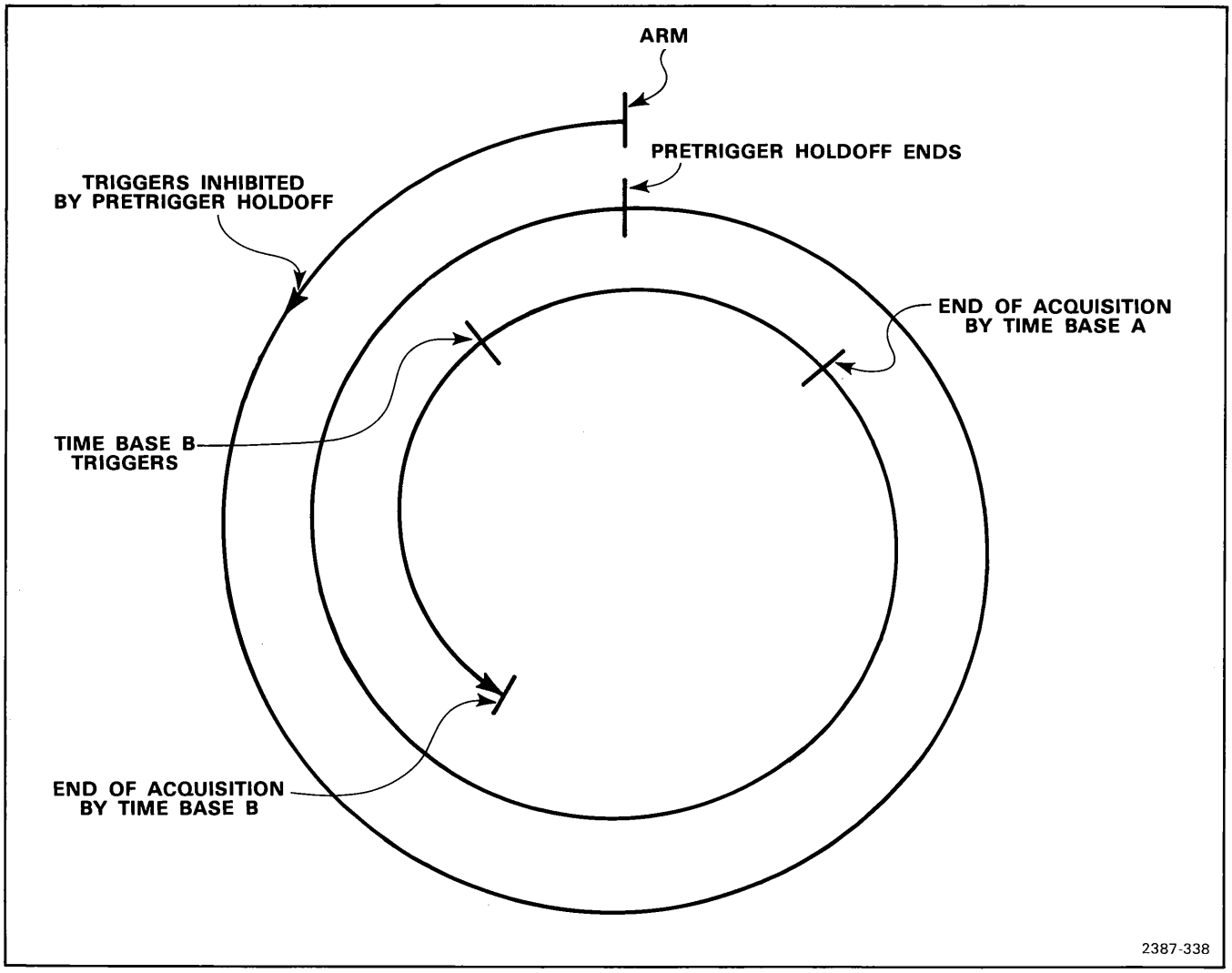


Figure 3-16. Data storage in B triggers after A mode.

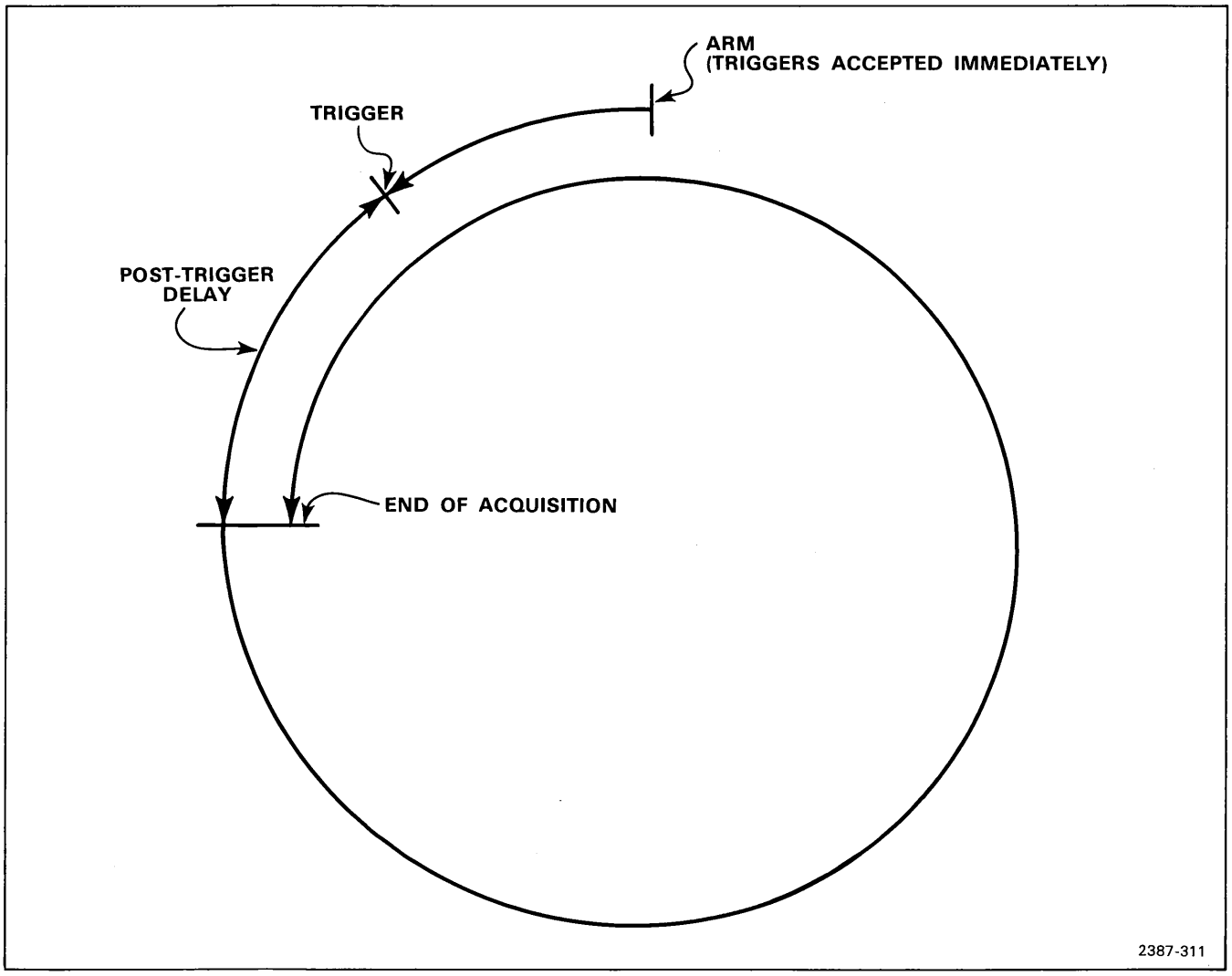


Figure 3-17. Data storage in post-trigger mode.

8 SEQUENCE CONTROL

The 7612D Time Base acts as the traffic controller for waveform data destined for the Data Memory. It generates memory addresses, clock signals, and chip-select signals that control the storage of data in the memories. Diagrams 8, 9, and 10 show the Time Base circuits. The Time Base has six principal parts, as follows:

1. The breakpoint locator, on diagram 8,
2. the clock generator, on diagram 9,
3. the sample interval generator, on diagram 9,
4. the memory address generator, on diagram 10,
5. the trigger control circuit, on diagram 10, and
6. the trigger locator, on diagram 10.

Figure 3-18 is a simplified block diagram of the time base. The 5 ns clock from the Clock Buffer is fed to the Clock Generator where it is gated with signals from the Sample Interval Generator and trigger locator circuits. The Clock Generator thus supplies two clock outputs, TB & TB/8. TB drives the high-speed shift registers on the Data Memory Board. TB/8 drives the memory latches on the Data Storage board, and the memory address generator on the Time Base Board.

Samples from the hybrid comparators are shifted into the high-speed shift registers by every TB clock. When eight samples are shifted in, the TB/8 clock is asserted, latching the eight samples and after a short delay, writes them into the data memory.

The Memory Address Generator supplies the address that controls where data is written in the memory. It also generates a signal that inhibits triggers until one complete record of pre-trigger data is acquired at the beginning of each record. When a complete record is acquired, the Memory Address Generator stores the ending memory address of the record so that any individual record can be retrieved in response to a "read" command.

The Breakpoint Locator counts the samples taken in the current segment. When the programmed number of samples has been taken, a segment counter is incremented and the sampling interval for the next segment is retrieved from a RAM (U406, U400) in the Sample Interval Generator. The new sampling interval is latched into the Sample Interval Generator and used to divide the master clock down to the programmed sampling interval. The output of the Sample Interval Generator is the gate signal that the Clock Generator uses to select samples from the 200 MHz master clock to become the TB clock pulse.

When the programmed number of segments has been acquired, the Breakpoint Locator asserts a control signal (ERE) that tells the time base to start a new record. This resets the segment counters in the Breakpoint Locator and prepares the time base to begin acquiring the first segment of the next record when a trigger is accepted.

The Trigger Control circuit accepts inputs from the other channel's time base, the MPU, and the Memory Address Generator. The output of this circuit is a start (STRT) pulse that tells the Trigger Locator to remember the position of the trigger within the group of eight samples collected by the high-speed shift registers. This information is used to ensure that the correct number of samples from the last group are written into the memory at the end of the record. For example, if the trigger occurs on the fifth sample shifted into the shift registers, when the last group of samples is acquired, only the first five samples will be written, because this group of samples will be written at the same memory address as the first group. This preserves the five samples stored at this address that represent the first five samples of the record.

The MPU programs the time base with the number and length of records, breakpoints, sample intervals, and trigger mode parameters. Acquisitions and waveform data output are also initiated by the MPU. The Translator Board serves as an interface between the time base and the MPU bus.

The time base also acts as a memory controller when data is being sent to the IEEE 488 bus or the XYZ monitor. The MPU sets the time base to read mode, sets the Memory Address Generator to the address of the record to be transmitted, and prepares the IEEE 488 interface to accept data directly from the time base.

BREAKPOINT LOCATOR

The breakpoint locator stores the location of the programmed breakpoints and provides the memory address for the sampling interval and breakpoint RAMs. The circuit also counts samples and compares this count to the stored breakpoint. When a breakpoint is reached, the segment counter is incremented and the sampling interval for the new segment is loaded into the sample interval generator. Figure 3-19 shows a block diagram of the breakpoint locator.

The segment counter contains the address number of the current segment. This counter provides the memory address for the sampling interval RAMs (diagram 9) and breakpoint RAMs. When the time base is armed, the MPU loads the breakpoint RAMs with the location of each breakpoint. The sample counters keep track of the number of samples acquired and the sample-number comparators compare the location of the next breakpoint to the number of samples acquired.

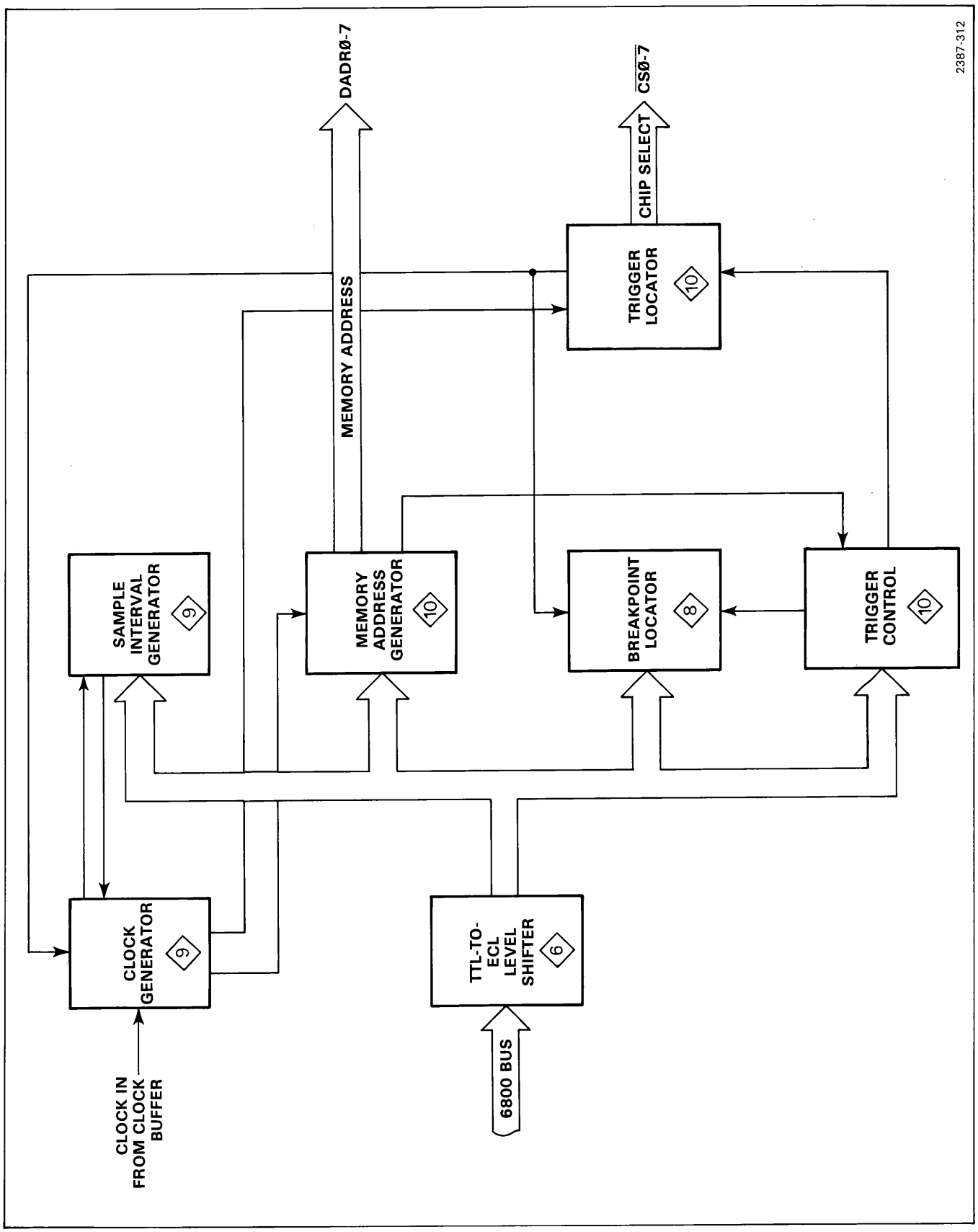


Figure 3-18. Simplified block diagram of the 7612D time base.

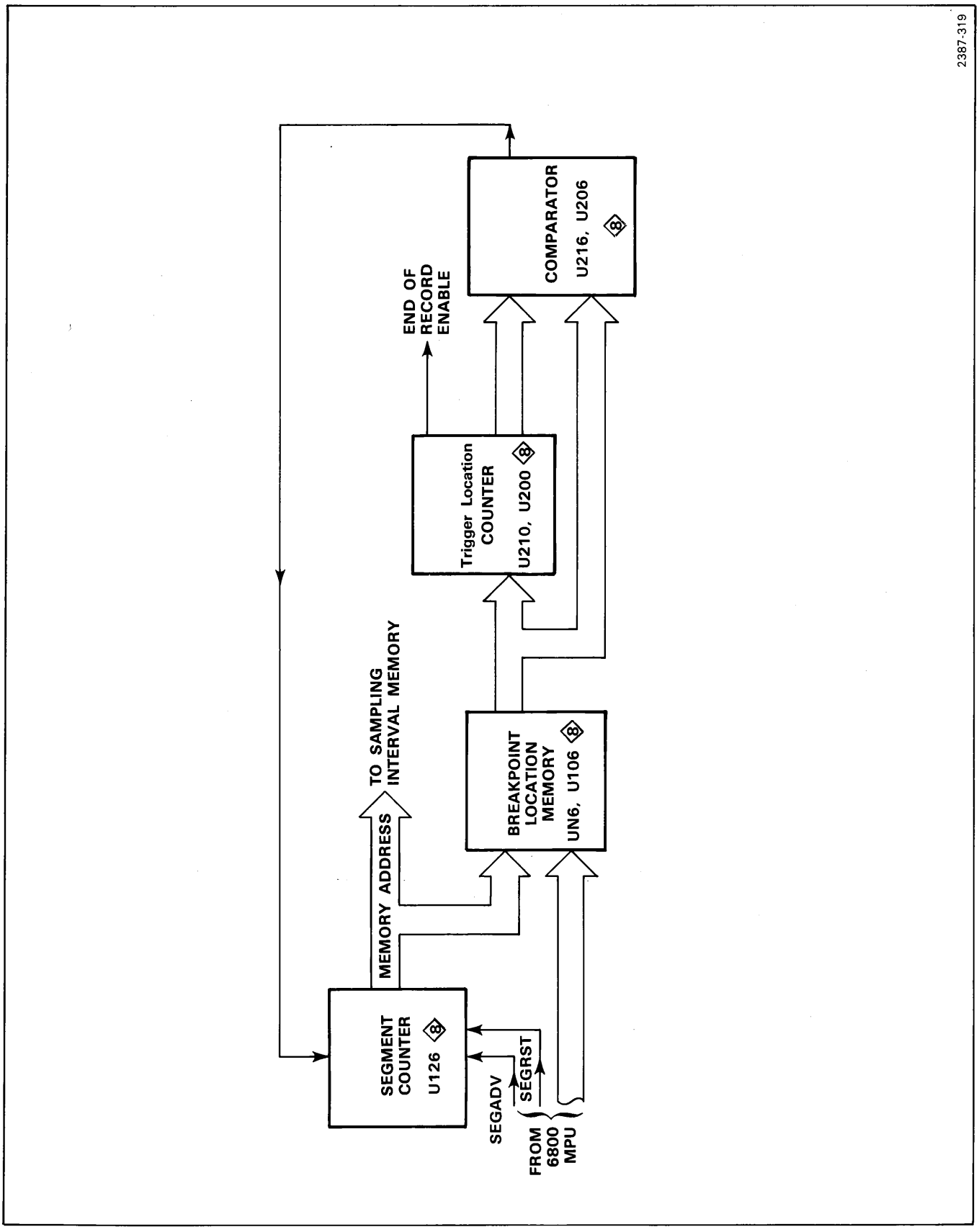


Figure 3-19. Block diagram of the breakpoint locator.

Operation In Pre-Trigger Mode

Recall from our discussion of programming the time base, that the first location in the breakpoint RAMs is loaded with the pre-trigger value. This value is the record length minus the number of pre-trigger samples. When the MPU completes the programming process, the last SEGRST pulse loads this pre-trigger value into the trigger location (TL) counter, U200 and U210.

The outputs of the breakpoint RAMs go to one input of exclusive-OR gates U216 and U206; the outputs of the TL counter go to the other inputs. Thus gates U216 and U206 compare the outputs of the breakpoint RAM and the TL counter. When all eight trigger location lines match the eight breakpoint RAM lines, both U216 and U206 will produce a low output, which is connected to the D input of U140C. The low on U140C's D input permits the next TL pulse to clock segment counter U126 via U140C.

The TL counter advances only after a trigger has occurred. Gates U306A-U306B produce pulses that clock the TL counter. During a store operation the low on EOP will disable U306A and the high on $\overline{EOP}$ will enable U306B. When U306B is enabled, TRIG LOC pulses can activate it and its output will clock the TL counter. TRIG LOC will be asserted only after pretrigger holdoff is satisfied, which will take place on the first trigger after pretrigger holdoff and on every eighth clock cycle afterwards. The TRIG LOC frequency equals TB/8.

While $\overline{EOP}$ is high (7612D in store mode), TRIG LOC pulses will increment the TL counter once after each eight samples. When its count matches the count in the breakpoint RAM, U216 and U206 will produce a low output. The output of U216 and U206 is connected to the D input of U140C. The next TL pulse will clock U140C, causing its $\overline{Q}$ output to go high and its Q output to go low. The low Q output of U140C will disable U100C because SEGADV is low, and U100C's high out will set U140C. The outputs of U140C will now be: Q high, activating U100C and ending the set input to U140C; and $\overline{Q}$ low. This sequence of events will generate one clock pulse for segment counter U126.

When it is advanced, the segment counter does two things:

1. It selects a new sample interval by sending a new address to the sample interval memory (diagram 9), and

2. It selects a new breakpoint from the breakpoint RAMs.

When the TL counter reaches terminal count (pins 4 of U200 and U210 low), U100A will be activated, and will assert a high ERE.

Via FFs U120B and U130B, ERE will cause a high at the pin 15 input of FF U140A. The next TB/8 will cause U140A to assert HOFST and $\overline{HOFST}$. The high on HOFST will:

- put shift register U440 (diagram 10) in hold mode (because HOFST sets U440's S0 and S1 inputs high via FF U346C and U146B, respectively),

- enable the eight chip-select gates via U316B. The high outputs of U440 will deselect memory chips that should not be written.

- reset segment counter U126 to zero via U130A and U100D.

- put trigger-location counter U200-U210 in load mode.

The low on $\overline{HOFST}$ will:

- enable U536B (diagram 8) so that TB 3 will activate it to produce an $\overline{ER}$ pulse. The $\overline{ER}$ pulse stores the memory address in U236 and U320 (diagram 10), and stores the chip-select data in U426.

- enable FF U110A (diagram 8) to produce EOP when the next TB/8 pulse occurs.

The EOP pulse will:

- allow $\overline{TB/8}$ instead of Trig Loc to clock the TL counter via U306A and B,

- reset pretrigger hold-off FF U516A (diagram 10), and

- enable U120A (diagram 8) to generate RSTA on the next TB/8 pulse (RSTA will set FF U526B, which will assert a low on STRT).

- Via U316C, EOP will also reset memory address counters U230 and U226 (on diagram 10).

- advance partition counter U220.

The time base is now ready to acquire another record, which it will do unless record number counter U220 is at terminal count. If U220 is at terminal count, its $\overline{DNE}$ output and $\overline{RSTA}$ will activate U316D, whose output will reset write FF U516B. The low on Write will then activate U410B which will assert a low on $\overline{DN}$, causing an interrupt to the MPU to tell it that the acquisition is complete.

When the Write and PGM lines are low the time base is in the read mode.

Operation In Post-Trigger Mode

In the post-trigger (special-delay) mode the TL counter counts the delay and the record length after the delay. Because of this the TL counter can reach terminal count before the end of a record. To prevent this terminal count from generating an ERE pulse, U006A is activated by highs on SDM and the $\overline{TC}$ output of segment counter U126. The segment counter is programmed to reach terminal count after the early $\overline{TC}$ from the trigger level (TL) counter has ended. Gate U006A will be disabled by the $\overline{TC}$ output of U126. The two desired $\overline{TC}$ signals from TL counter U210 and U200 thus activate U100A and produce the ERE signal.

PROGRAMMING THE TIME BASE

Time Base Control Signals

The MPU system accepts input from the front panel or from the IEEE 488 bus. Input that affects the time-base settings is not implemented immediately; it is stored in an intermediate program buffer by the MPU system. When the time base is armed, the MPU verifies the validity of settings, reports any errors found, and, if necessary, modifies the settings to resolve conflicts. Then the MPU puts the time base in program mode and loads the record length, trigger mode, breakpoint locations, sampling intervals, and number of records parameters. When the MPU takes the time base out of program mode, the acquisition starts.

The Time-Base-Control logic, shown on diagram 5, interfaces the time base and the MPU. Data from the MPU reaches the time base through a TTL-to-ECL level shifter on the Translator Board. The MPU programs time-base functions through this extended data bus and a set of control lines decoded from the MPU address bus. Table 3-2 shows the control lines, their MPU addresses, and a summary of their functions.

TABLE 3-2
Time Base Control Signals

Name	Address	Function
A:SEGRST	0D90	Reset time base A segment counter.
A:SEGADV	0D91	Advance time base A segment counter.
A:SEGLNG	0D92	Write A segment length into breakpoint address memory.
A:SI	0D93	Write A sample interval into sample interval memory.
A:NPTN	0D94	Write A record length into record length memory.
A:PTNRST	0D95	Reset time base A partition counter.
A:PTNADV	0D96	Advance time base A partition counter.
A:DTM	0D97	Write trigger mode into A trigger mode latches.
B:SEGRST	0D98	Reset time base B segment counter.
B:SEGADV	0D99	Advance time base B segment counter.
B:SEGLNG	0D9A	Write B segment length into breakpoint address memory.
B:SI	0D9B	Write B sample interval into sample interval memory.
B:NPTN	0D9C	Write B record length into record length memory.
B:PTNRST	0D9D	Reset time base B partition counter.
B:PTNADV	0D9E	Advance time base B partition counter.
B:DTM	0D9F	Write trigger mode into B trigger mode latches.

Setting the Time Base to Program Mode

The MPU programs the time base in two steps. The first of these steps is performed only when the time base settings have been modified since the last ARM; it loads data to establish: a.) record length, b.) trigger source (Channel A or Channel B), c.) breakpoints and sample intervals. The second step is performed each time the instrument is armed, even if no settings are changed. This step specifies the number of records and the trigger mode (pre- or post-trigger). Figure 3-20 shows a simplified flow chart of the time base programming process.

The MPU begins the programming process by asserting PGM (A:PGM for channel A, B:PGM for channel B) to put the time base(s) into the program mode. The PGM signals from U500 (diagram 5) are converted to ECL-level signals by U400 and fed to their respective time bases via the Main Interconnect Board. The PGM signal comes onto the time base board in the lower-right of diagram 8. U530D buffers and inverts the signal to produce PGM. These signals are distributed throughout the time base to set it up for programming. We'll discuss the individual effects of the signals in the descriptions for the circuits involved.

Step 1

Setting the Record Length. If the time-base settings have changed since the last arm, the MPU will program the record length by placing a code for the selected record length on the four low-order bits of the data bus and asserting PTNL (ParTitioN Length). The record length is stored in a four-bit latch, U310, shown in the lower-right of diagram 10. The four low-order bits of the MPU data bus, translated to ECL levels, are fed to the latch inputs (ED0-3). The rising edge of PTNL clocks the data into the register. Table 3-3 shows the code for each record length and for the Post-Trigger mode.

TABLE 3-3
Programming Codes for the Record Length Latch

Record Length	Code				
	ED3 Mode				
	SDM*	PRE	ED2	ED1	ED0
2048	1	0	0	0	0
1024	1	0	1	0	0
512	1	0	1	1	0
256	1	0	1	1	1

***Special Delay Mode (Post-Trigger Mode)**

The outputs of the record-length latch are used to detect the completion of the pre-trigger hold-off and to generate the three high-order bits of the data memory address.

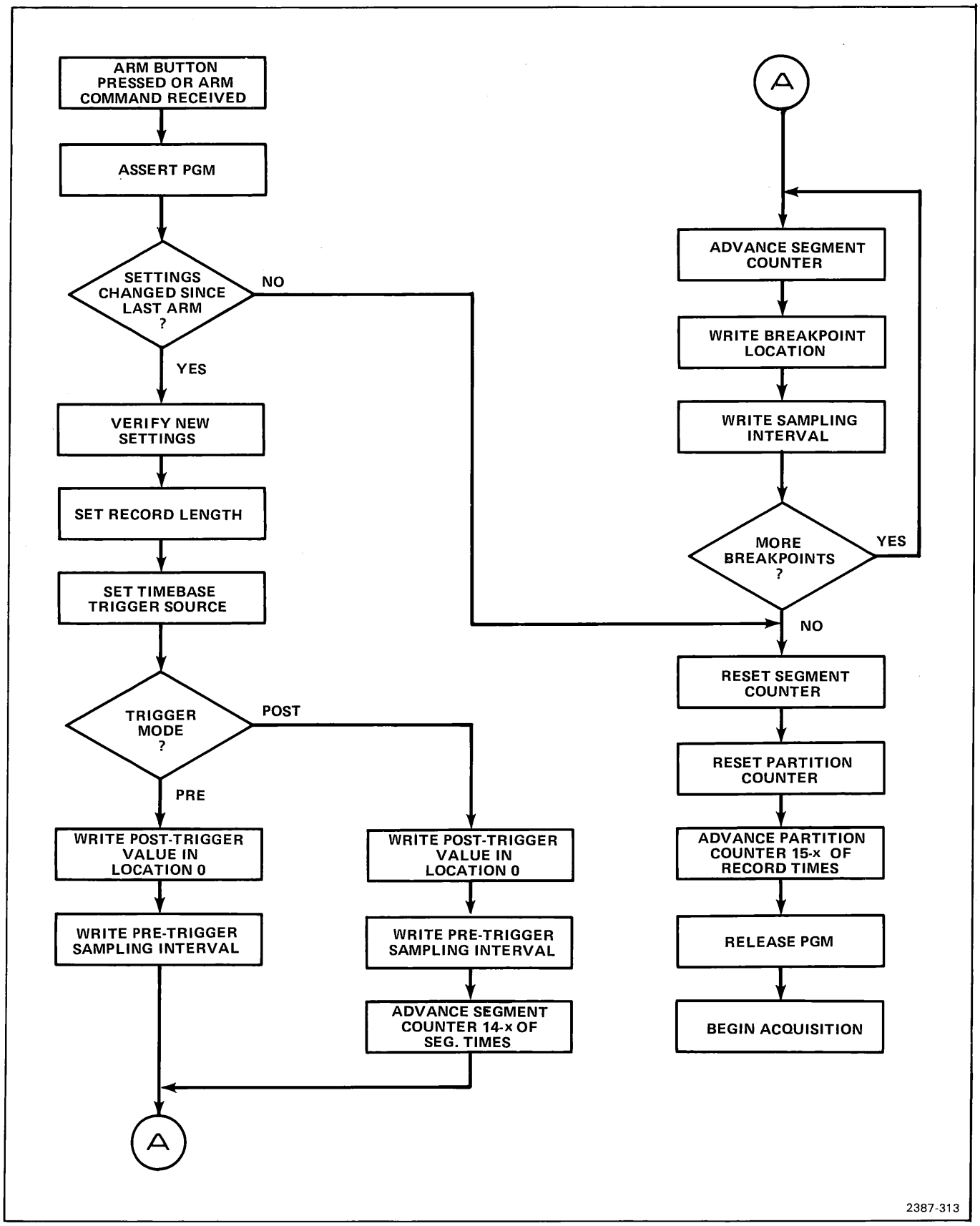


Figure 3-20. Simplified flow chart of the time base program.

Selecting the Trigger Source. Next, the MPU selects the trigger source for the time base. The trigger for time-base A can come from either the right or left trigger channel. The B time base trigger can also come from either of these sources, and can be inhibited until channel A has acquired its first complete record (B after A mode). The MPU programs the trigger source by placing a code on ED0 and ED1 and asserting DTM. Table 3-4 shows the codes required to set the trigger source for each time base.

TABLE 3-4
Programming Codes for the Time Base Trigger Source

Time Base	Trigger Source	Code	
		ED1	ED0
CHANNEL A	Left	0	0
CHANNEL A	Right	0	1
CHANNEL B	Right	0	0
CHANNEL B	Left	0	1
CHANNEL B	B after A (R source)	1	0
CHANNEL B	B after A (L source)	1	1

Analog trigger signals from the plug-in units or EXT TRIG IN connectors are received and processed by the right and left trigger generators. The output of each trigger generator is an ECL-level Gate signal that goes to the corresponding time base via a loop-through of the opposite time base. The trigger signal comes on to the Time Base Board in the upper-left of diagram 10. The trigger signal from the other time base arrives on pin A1.

The trigger source circuit selects either the trigger coming from the corresponding trigger channel, or the trigger signal looped through from the other time base. The positive transition of DTM clocks the data on the two low-order bits of the MPU data bus (ED0 and ED1) into U526A and U510A, respectively. If ED0 is high when DTM goes high, the Q output of U526A will go high, enabling U530A. This selects the trigger signal coming directly from the trigger board as the trigger source. If ED0 is low when DTM goes high, the Q output of U526A will go low, enabling U530C and selecting the trigger signal from the other time base.

If the time base is plugged into the channel B slot, an additional option is available. The trigger can be inhibited until time base A acquires one complete record. This is accomplished by setting ED1 high and asserting DTM. The high on ED1 causes the Q output of U510A to go low, enabling flip-flop U510B. When the programming process is complete, PGM goes low, leaving the Q output of U510B high. The high on this output inhibits the positive transition required to clock U526B and start the B acquisition. When channel A finishes acquiring one complete record, the B EOP (Buffered End of Partition) line goes high, clocking U510B. The Q output goes low, so the next trigger will cause a positive transition on the clock input of U526B, asserting STRT and $\overline{\text{STRT}}$ (Start).

Setting Breakpoint and Sample Interval in Pre-Trigger Mode. If any of the time-base settings have changed since the last ARM operation, the MPU loads the breakpoint locations and sampling intervals in high-speed ECL RAM in the time base. The breakpoint locations are stored in two RAM chips, U106 and U116, shown at the top-center of diagram 8. The sampling interval for each segment is stored in another pair of RAM chips, U400 and U406, shown in the center of diagram 9.

To begin the storing process, the MPU resets the segment counter, U126 (top-left of diagram 8), by asserting SEGRST (Segment ReSeT). The outputs of this counter (SC0-SC3) provide the address inputs for the breakpoint location and sampling interval RAM. When the counter is reset, its outputs are set to zero, and the first location in the RAMs (location zero) is selected.

Then, the MPU places the pre-trigger value on the data bus (ED0-7) and asserts SEGLNG (Segment Length) to write the data into U106 and U116. The sampling interval for the pre-trigger samples (which is the same as for the first segment) is placed on the bus next and $\overline{\text{SI}}$ (bottom-center of diagram 9) is asserted to write the data into RAMs U400 and U406.

Next, the MPU asserts SEGADV (SEGment ADVance) to advance the segment counter and point to the next RAM location. The first breakpoint and its corresponding sampling interval are written into the RAM at this location. This process is repeated until all the breakpoints are loaded into the time base.

Finally, SEGRST is asserted to reset the segment counter in preparation for the start of acquisition. This SEGRST pulse also loads the first breakpoint location into trigger-location counters U200 and U210. The high on SEGRST causes the inverted output (pin 15) of U100D to go low, enabling the parallel inputs of the sample counters. However, the counters require a clock pulse on their CP inputs to load the data from the parallel inputs. The SEGRST pulse, differentiated by C546, R546, and R640 (upper-left of diagram 9), generates this clock pulse. The positive transition from the differentiator network causes the output of U536D and U146E to go low and cause a brief low on Trig Loc.

Trig Loc is connected to the input of U306B at the left-center of diagram 8. Because $\overline{\text{EOP}}$ is high, the low on Trig Loc will disable U306B, and U306B will go low briefly.

At the end of the Trig Loc pulse, the clock inputs of U200 and U210 will return a positive transition and will load the first value from the breakpoint RAMs.

Setting Breakpoints and Sample Intervals in Post Trigger Mode. The process for loading breakpoints in post-trigger mode is similar to the pre-trigger operation except that the first location of the breakpoint RAM stores the post-trigger value and sampling interval instead of the pretrigger values. The post-trigger value is set so that the trigger-location counters will reach terminal count (15) when

the number of post-trigger samples plus the number of samples in the record have been taken.

Breakpoints are loaded in post-trigger mode the same way as in pretrigger mode, except that the breakpoints are moved to the end of the breakpoint memory, so that the last breakpoint is always written in location 14 of the memory (see Fig. 3-21). After the post-trigger value is loaded in location zero, the 6800 pulses SEGADV 14 minus the number of segments times. If, for example, three breakpoints (four segments) are set, the 6800 pulses SEGADV 10 times. The first breakpoint is written in memory location 12, the second is written in location 13, and the last breakpoint is written in location 14.

Step 2

Setting the Number of Records. The MPU sets the time-base hardware to acquire the selected number of records at each ARMing, even if the settings haven't changed. First, the MPU asserts PTNRST (Partition Reset) to reset partition counter U220 (bottom-right of diagram 8). Then it pulses PTNADV (Partition Advance) 15 minus the number of records times. If four records are selected, PTNADV will be pulsed eleven times. This presets the counter so that it will reach terminal count (15) after four records have been acquired.

Beginning the Acquisition. When all the time base programming is complete, the MPU enables the "done" interrupt generated by the terminal count ($\overline{TC}$) output of the partition counter, U220. This interrupt signals the MPU when the acquisition is complete. Finally, the MPU releases PGM and the time base begins taking samples.

9 SAMPLE INTERVAL GENERATOR

The Sample Interval Generator consists of two programmable divider circuits that produce gate signals for the clock generator. Figure 3-22 shows a block diagram of the Sample Interval Generator.

Two RAMs store the codes that set the sample interval generator to the desired divide ratio for each segment. The section on Programming the Time Base describes how the microprocessor loads these RAMs. During the acquisition, the segment counter provides an address that points to the RAM location that contains the sampling interval for the current segment. The data outputs of the RAMs are loaded into the programmable dividers by a Rate Latch Clock pulse (RLCLK) from the clock generator.

The pre-scaler divider network divides the master clock by an integer value from one to ten. The other network divides the output of the pre-scaler by decade values from one to 1 $\times$ 10 to the seventh power. To generate a five ms sampling interval, for example, the pre-scaler is set to divide by 5. The decade divider is set to divide the output of the pre-scaler by 100. The result is a 5 ms gate pulse for the clock generator.

Diagram 9 shows the sample interval generator. The sample interval RAMs, U406 and U400, are shown at the top- and bottom-center of diagram 9. RAM U400 stores the pre-scaler value, and U406 stores the decade divider value. Table 3-5 shows the code stored in each RAM for all valid sampling intervals. Bits 4-7 program the pre-scaler network; bit 3 is cleared (low) only when the 5 ns sampling interval is used. Bits 0-2 program the decade divider.

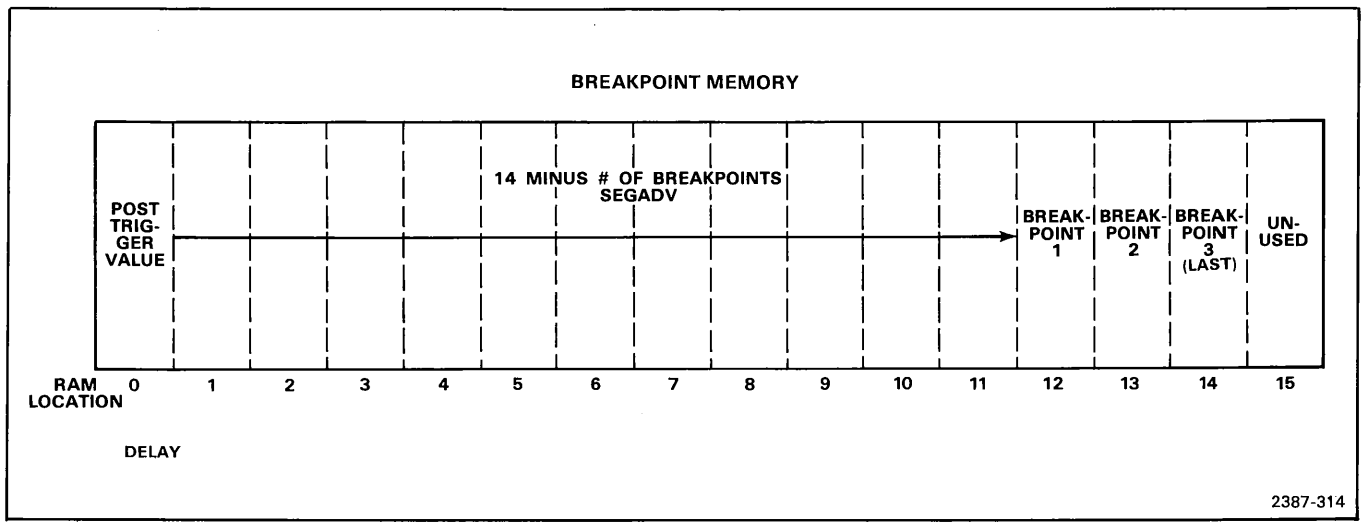


Figure 3-21. Loading breakpoints in post-trigger mode.

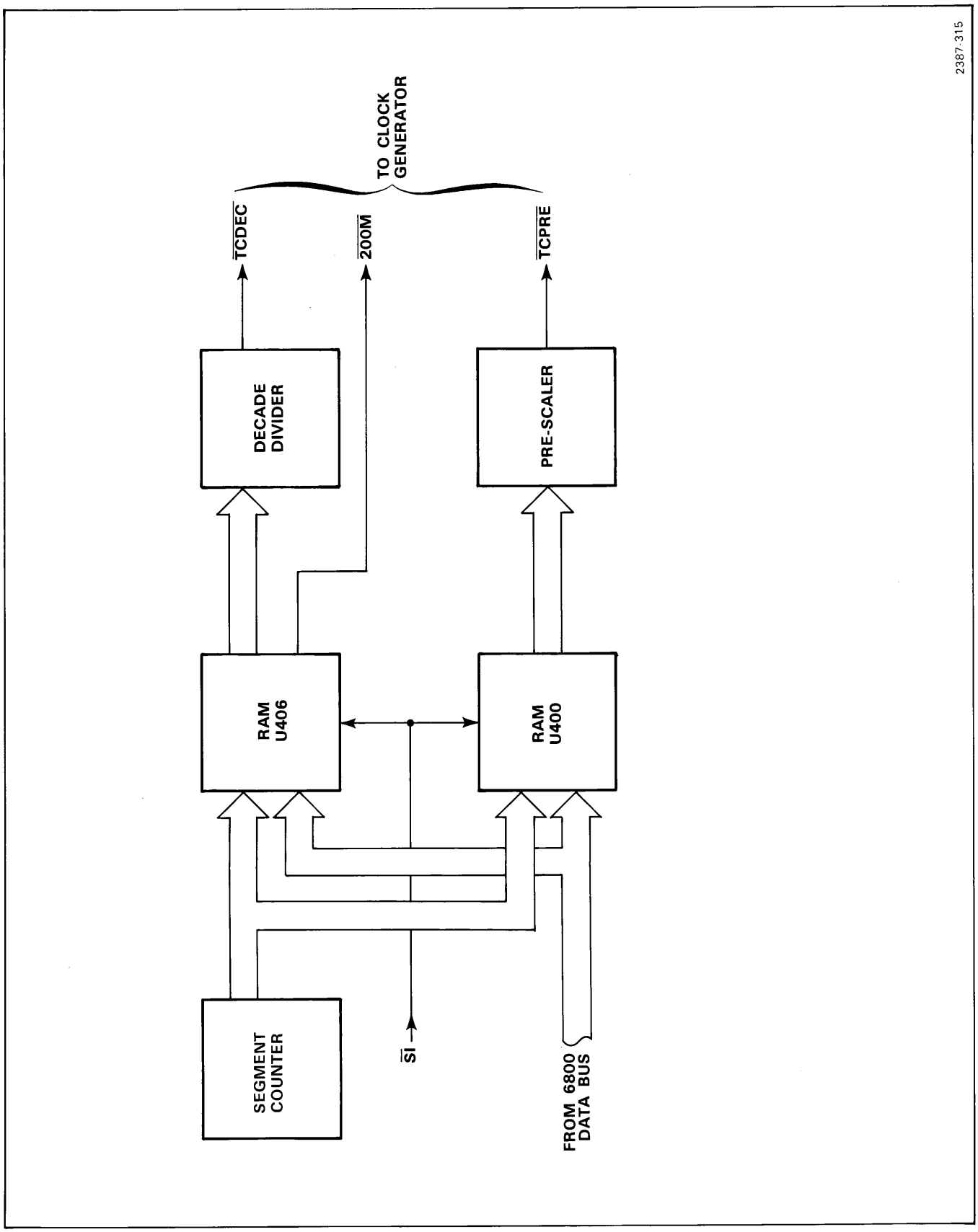


Figure 3-22. Block diagram of sample interval generator.

TABLE 3-5
Sample Period Word

Sample Period	Data Bus			Hex	Divide Ratio
	7 6 5 4	3	2 1 0		
5 ns	1 0 0 1	0	1 1 1	97	1
10 ns	1 0 0 1	1	1 1 1	9F	2
20	1 0 0 0	1	1 1 1	8F	4
30	0 1 1 1	1	1 1 1	7F	6
40	0 1 1 0	1	1 1 1	6F	8
50	0 1 0 1	1	1 1 1	5F	10
60	0 1 0 0	1	1 1 1	4F	12
70	0 0 1 1	1	1 1 1	3F	14
80	0 0 1 0	1	1 1 1	2F	16
90	0 0 0 1	1	1 1 1	1F	18
100	0 0 0 0	1	1 1 1	ØF	20
200	1 0 0 0	1	1 1 0	8E	40
300	0 1 1 1	1	1 1 0	7E	60
400	0 1 1 0	1	1 1 0	6E	80
500	0 1 0 1	1	1 1 0	5E	100
600	0 1 0 0	1	1 1 0	4E	120
700	0 0 1 1	1	1 1 0	3E	140
800	0 0 1 0	1	1 1 0	2E	160
900 ns	0 0 0 1	1	1 1 0	1E	180
1 μs	0 0 0 0	1	1 1 0	ØE	200
2 μs	1 0 0 0	1	1 0 1	8D	400
3	0 1 1 1	1	1 0 1	7D	600
4	0 1 1 0	1	1 0 1	6D	800
5	0 1 0 1	1	1 0 1	5D	1000
6	0 1 0 0	1	1 0 1	4D	1200
7	0 0 1 1	1	1 0 1	3D	1400
8	0 0 1 0	1	1 0 1	2D	1600
9	0 0 0 1	1	1 0 1	1D	1800
10	0 0 0 0	1	1 0 1	ØD	2000
20 μs	1 0 0 0	1	1 0 0	8C	4E3
30	0 1 1 1	1	1 0 0	7C	6E3
40	0 1 1 0	1	1 0 0	6C	8E3
50	0 1 0 1	1	1 0 0	5C	10E3
60	0 1 0 0	1	1 0 0	4C	12E3
70	0 0 1 1	1	1 0 0	3C	14E3
80	0 0 1 0	1	1 0 0	2C	16E3
90	0 0 0 1	1	1 0 0	1C	18E3
100 μs	0 0 0 0	1	1 0 0	ØC	20E3
200 μs	1 0 0 0	1	0 1 1	8B	4E4
300	0 1 1 1	1	0 1 1	7B	6E4
400	0 1 1 0	1	0 1 1	6B	8E4
500	0 1 0 1	1	0 1 1	5B	10E4
600	0 1 0 0	1	0 1 1	4B	12E4
700	0 0 1 1	1	0 1 1	3B	14E4
800	0 0 1 0	1	0 1 1	2B	16E4
900 μs	0 0 0 1	1	0 1 1	1B	18E4
1 ms	0 0 0 0	1	0 1 1	ØB	20E4

TABLE 3-5 (cont)
Sample Period Word

Sample Period	Data Bus 7 6 5 4	Data Bus 3	Data Bus 2 1 0	Hex	Divide Ratio
2 ms	1 0 0 0	1	0 1 0	8A	4E5
3	0 1 1 1	1	0 1 0	7A	6E5
4	0 1 1 0	1	0 1 0	6A	8E5
5	0 1 0 1	1	0 1 0	5A	10E5
6	0 1 0 0	1	0 1 0	4A	12E5
7	0 0 1 1	1	0 1 0	3A	14E5
8	0 0 1 0	1	0 1 0	2A	16E5
9	0 0 0 1	1	0 1 0	1A	18E5
10 ms	0 0 0 0	1	0 1 0	ØA	20E5
20 ms	0 0 0 0	1	0 0 1	89	4E6
30	0 1 1 1	1	0 0 1	79	6E6
40	0 1 1 0	1	0 0 1	69	8E6
50	0 1 0 1	1	0 0 1	59	10E6
60	0 1 0 0	1	0 0 1	49	12E6
70	0 0 1 1	1	0 0 1	39	14E6
80	0 0 1 0	1	0 0 1	29	16E6
90	0 0 0 1	1	0 0 1	19	18E6
100	0 0 0 0	1	0 0 1	Ø9	20E6
200 ms	1 0 0 0	1	0 0 0	88	4E7
300	0 1 1 1	1	0 0 0	78	6E7
400	0 1 1 0	1	0 0 0	68	8E7
500	0 1 0 1	1	0 0 0	58	10E7
600	0 1 0 0	1	0 0 0	48	12E7
700	0 0 1 1	1	0 0 0	38	14E7
800	0 0 1 0	1	0 0 0	28	16E7
900 ms	0 0 0 1	1	0 0 0	18	18E7
1 sec	0 0 0 0	1	0 0 0	Ø8	20E7

PRE-SCALER DIVIDER

The pre-scaler divider divides the C100M clock (the 200 MHz clock was divided by two in the clock generator) by integer values from one to ten. The division is accomplished by presetting decade counter U636 (bottom-right of diagram 9) with a value that will cause it to reach terminal count (9) in the desired number of clocks. For example, to divide by four, the counter is preset to six (0110). After three clock pulses, the counter reaches nine, and the $\overline{TC}$ output will go low (see Fig. 3-23). The low on $\overline{TC}$ drives the $\overline{PE}$ (Parallel Enable) input low. On the next positive clock transistion (the fourth clock), the counter reloads the value on its parallel inputs and the process is repeated.

The parallel inputs of the counter receive data from latch U610. While the sampling interval remains unchanged the outputs of the latch will not change, and the pre-scaler counter will reload itself with the same value each time it reaches terminal count. Thus, the counter continuously divides the 100 MHz clock by the programmed value.

DECADE DIVIDER

The decade divider is similar to the pre-scaler divider. It consists of seven cascaded decade counters, with U700 (top-right of the diagram) as the most significant counter in the string. The terminal count output of the pre-scaler divider ($\overline{TCPRE}$) provides a gate signal for the decade counter. Each time the pre-scaler counter reaches terminal count, the $\overline{TCPRE}$ output goes low, and one 100 MHz clock pulse is allowed to pass through U536C, clocking the decade counter once. The positive transition of the $\overline{TCPRE}$ pulse also clocks pre-scaler U636, reloading it and causing $\overline{TCPRE}$ to go high.

The decade counter can use type 10010 or type 10016 integrated circuits. When type 10010 is used, each counter can be loaded with zero (0000) or nine (1001). (When type 10016 is used, each counter can be loaded with six (0110) or 15 (1111). If the counter is loaded with zero, it will require nine clock pulses to reach terminal count. Then, its terminal count output will go low, and the tenth clock pulse will reload the counter and clock the next counter in the chain. In

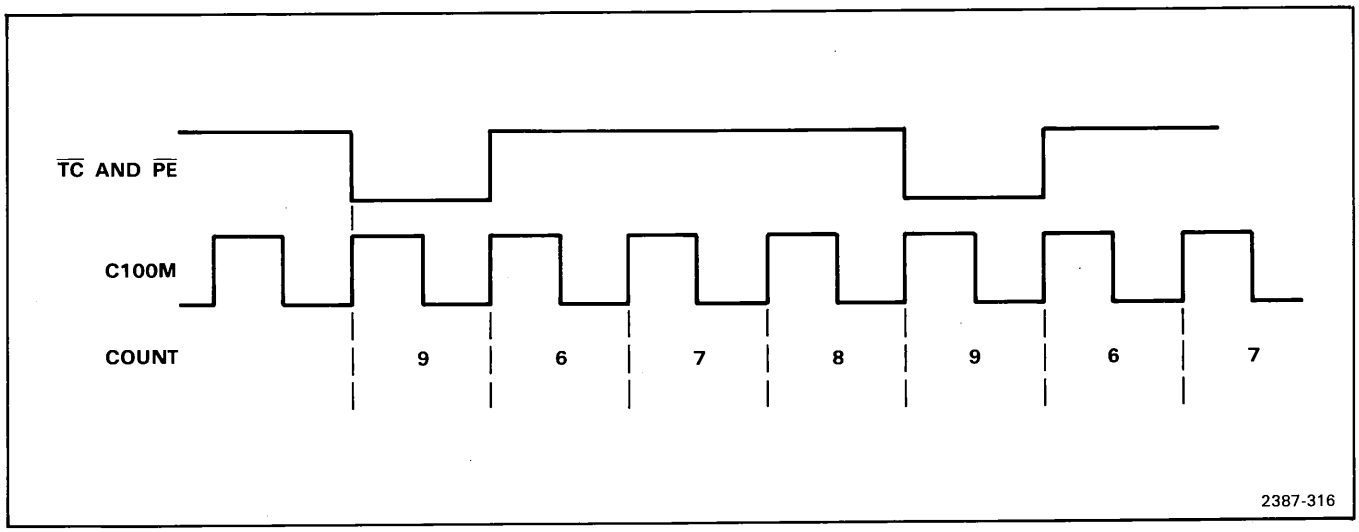


Figure 3-23. Timing for a divide-by-four operation in the pre-scaler.

this mode, the counter divides by ten. If the counter is preset to nine, the terminal count output is immediately asserted, and the next clock pulse clocks the next counter in the chain. In this mode, the counter effectively divides by one.

Each counter also has a count enable ($\overline{CE}$) input that must be low to enable the counter clock input. When the input is high, clocks are ignored. The count enable input of each counter (except U700) is gated so that it is asserted only when all the preceding counters have reached terminal count. For example, the third counter (U616) is clocked only when U700 and U606 have both reached terminal count. When they do, both inputs of U726A will go low, so its output goes low. This enables the parallel inputs of U606 to reload the counter and assert the U616 count enable input. The next clock pulse reloads U606 and clocks U616. Thus, U700 is clocked once for each $\overline{TCPRE}$ pulse, U606 is clocked once each 10 pulses, U616 is clocked once every 100 pulses, and so on.

The counters are programmed by three bits from RAM U406. The array of gates between the RAM output and latch U600 convert this three-bit binary code to a seven-bit code. Table 3-6 shows the three-bit binary code and the seven-bit output code. Notice that the seven-bit code contains a number of 1's equal to the value of the binary input value. When the input for a counter is a 1, the P0 and P3 inputs are held high and the counter is preset to nine. The counter's TC output goes low immediately, and the counter effectively divides by one. When the input to the counter is zero, its parallel inputs are all held low, presetting it to zero. In this mode, the counter divides by ten. Each counter that is set to divide by ten provides a decade of division (multiplies the interval by 10). When two counters are set to divide by ten, the net result is a division by 100. Three counters divide by 1000, and so on. If all seven counters are set to divide by ten, the decade divider will produce one $\overline{TCDEC}$ pulse for 10^7 $\overline{TCPRE}$ pulses.

TABLE 3-6
Decade Counter Programming Codes

Input Binary Value			Seven-bit Output Code							Division Ratio (Number of Zeros In This Row Under "Seven-Bit Output Code")
2	1	0	U700	U606	U616	U710	U720	U626	U730	
0	0	0	0	0	0	0	0	0	0	7
0	0	0	1	0	0	0	0	0	0	6
0	1	0	1	1	0	0	0	0	0	5
0	1	1	1	1	1	0	0	0	0	4
1	0	0	1	1	1	1	0	0	0	3
1	0	1	1	1	1	1	1	0	0	2
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

For example, if the decade counter is programmed with a decimal three (binary 011), U730, U626, U720, and U710 will divide by ten each, for a net division of 10,000 (10 to the fourth power).

GENERATING A SAMPLE INTERVAL CLOCK

Now let's walk through the complete division process for generating one sampling interval clock. For this example, assume that the sampling interval is set to five ms. Table 3-5 shows that the pre-scaler divider will have loaded a five (0101) to divide by five. This value will be latched by U610 and will appear at the parallel inputs of U636. The counter will begin counting up from five. Four clocks later it will reach terminal count (nine) and $\overline{\text{TCPRE}}$ will go low. The next clock pulse will reload the counter with the data that remains at its parallel inputs. This same clock pulse will pass through U536C while $\overline{\text{TCPRE}}$ is low, clocking counter U700 once for each five C100M pulses for an output period of 50 ns.

Table 3-5 shows that for a five ms sampling interval, the decade counter was also programmed with a five (0101). From Table 3-6, a 0101 on the decade divider inputs causes U626 and U730 to divide by ten, and the others to divide by one, for a net division of 100.

The decade counter will receive a C100M pulse each time the pre-scaler reaches terminal count (every 50 ns in this example). Multiplying the 50 ns output by the 100 from the decade counter yields a final output of 5000 ns, or five ms.

The output of the decade counter, $\overline{\text{TCDEC}}$ (Terminal Count Decade) is ANDed with the output of the pre-scaler counter to form the master time base clock TB.

CLOCK GENERATOR

The clock generator has three functions. First, it divides the master 200 MHz clock by two to drive the pre-scaler and decade dividers. Second, it takes the output of the pre-scaler and decade dividers and generates the master time base clock pulses, TB. Third, it generates the rate-latch pulse that controls the pre-scaler and decade-divider latches, U610 and U600.

DIVIDING THE MASTER CLOCK

The CLK signal from the Clock Buffer Board comes in at the left edge of diagram 9 as a differential signal. Buffer U740B converts it to single-ended. FF U540A divides the 200 MHz signal by two and applies the resulting 100 MHz clock (C100M) to the prescaler and decade dividers and to the time base (TB) generator circuit.

Generating the Time Base Clock (TB)

The time base generates the TB pulse, which controls the storage of samples coming from the hybrid comparators (on the Header Board). Gates U246A, U246C, and U336B (center of diagram 9) generate this clock pulse. The outputs of the three AND gates are wired-OR so that when any output goes high it will cause a high on the TB line.

When U336B is reading data from the data memory, U336B allows the MPU to generate TB clocks. In this mode, the WRITE line will be low and $\overline{\text{WRITE}}$ will be high, disabling U246A and U246C. The MPU asserts $\overline{\text{RD}}$ to generate TB clock pulses.

During an acquisition, the other two gates, U246A and U246C, generate the TB pulses. U246C produces the pulses when the time base is sampling at 5 ns, and U246A produces them at all other intervals.

When the time base is sampling slower than five ns, the 5NS line will be low and U246A will be enabled. Gate U246A will pass one C100M pulse from U540A each time the decade and pre-scaler dividers reach terminal count ($\overline{\text{TCPRE}}$ and $\overline{\text{TCDEC}}$ will go low).

When sampling at 5 ns, 5NS will be low, enabling U246C, and 5NS will be high, disabling U246A. Gate U246C will connect the 5 ns output pulses from U740B to the TB line.

DIVIDING THE TB CLOCK BY EIGHT

The data memory shift registers receive one sample on each TB pulse. After eight samples are collected, the group of samples will be written into the data memory. Shift register U640, in the lower-left of diagram 9, divides the TB clock by eight and provides several outputs at different phases with relation to the TB pulse. These outputs drive the data memory latches and other circuits in the time base.

Figure 3-24 shows the shift register timing. Assume that the shift register contains zeros at power-up, so the Q6 output and S0 input are low. With S0 low and S1 open-circuited (low), U640 will be set to load mode, so the next TB pulse will load the data P0-P7 inputs. P0-P6 are tied high and P7 is left open-circuited (low), so Q0-Q6 goes high and Q7 goes low. The highs on Q6 and S0 put the shift register in shift-left mode. The next clock pulse shifts each output from Q0 toward Q7. Q0 is loaded with a low, and the high in Q6 is shifted to Q7. The next clock (#1) pulse shifts the low from Q0 into Q1 and the subsequent pulse (#2) shifts the low into Q2. The low continues to move toward Q7 until it reaches Q6. Then the S0 input goes low again and the shift register switches to load mode. The next clock reloads the register and the process is repeated.

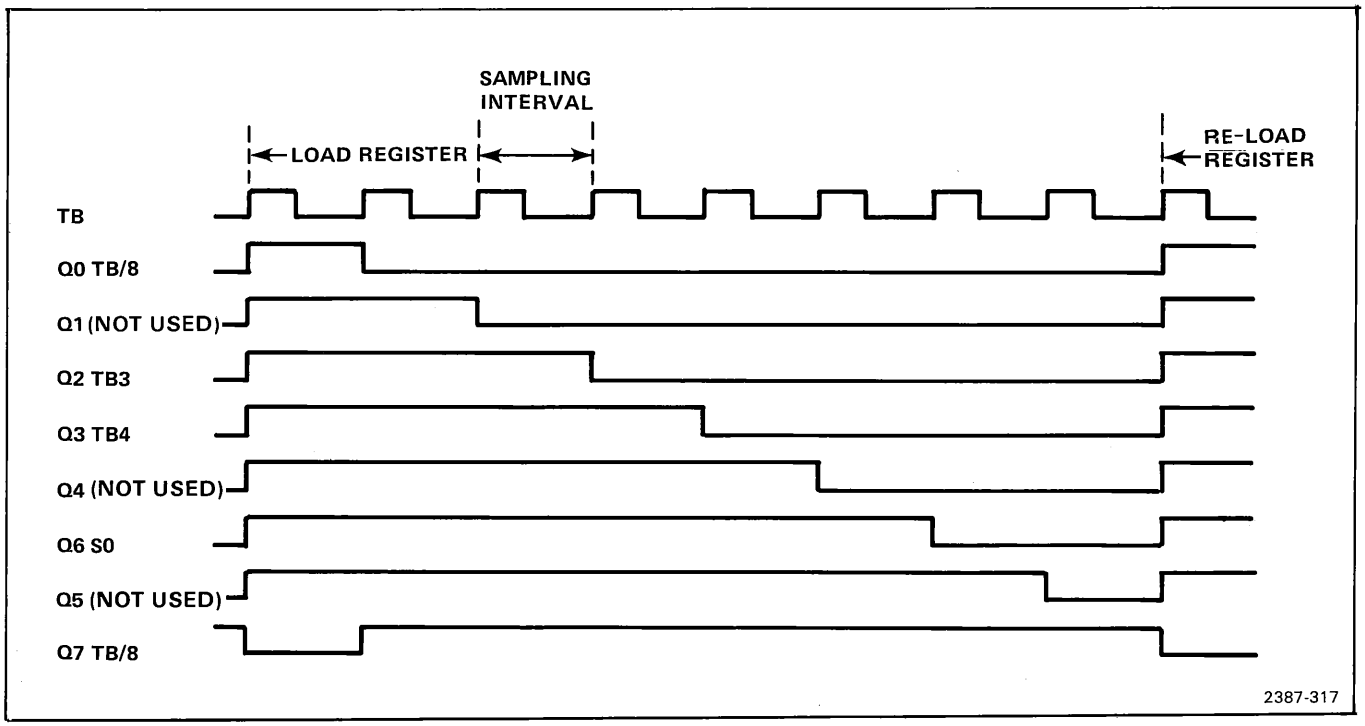


Figure 3-24. Timing of the TB/8 shift register, U640.

Generating The Rate Latch Clock (RLCLK)

The circuit in the upper-left of diagram 9 will produce a RLCLK pulse under five conditions:

1. at the end of the time-base programming sequence,
2. at the end of each record,
3. each time Trig Loc goes low while $\overline{\text{SLO}}$ and 5NS are low,
4. when TC DEC goes high while $\overline{\text{SLO}}$ is high and Trig Loc and 5NS are low, or
5. when TL 6 and 5 NS are low.

While the time base is being programmed, the microprocessor will assert PGM and $\overline{\text{PGM}}$. The high on PGM will cause the outputs of U620D and U620A to go high, which will set flip-flop U540C ($\overline{\text{Q}}$ output low). The high on PGM will also disable U146D, which will assert a low on the Trig Loc line.

At the end of time-base programming sequence, the MPU will assert SEGRST again. The SEGRST pulse is differentiated by C546, R546, and R640, resulting in a short positive-going pulse which will activate U536D briefly. The low output of U536D will disable U620B and cause a low on the RLCLK line. About 50 ns later, pin 13 of U536D returns to its low state and its output returns high. As a result, the RLCLK line makes a positive transition, latching the first sampling interval from the RAMs into divider latches U600 and U610.

At the end of each record, an RLCLK pulse will be generated, which will latch the first sampling interval into the frequency dividers in preparation for acquiring the first segment of the next record. When the time base finishes storing the current record, EOP (End Of Partition) will be asserted. The high on EOP will cause the output of U620B to go high, asserting RLCLK.

When Trig Loc goes low, RLCLK will be asserted. As long as the segment counter does not reach a breakpoint and advance, the dividers will be reloaded with the same sampling interval. When the breakpoint-locator circuit detects the end of a segment, the segment counters will be advanced, and the next RLCLK will latch the new sampling interval into rate latches U600 & U610. Depending on the sampling interval in use, one of three gates will produce the RLCLK pulse. For the 5 ns interval, U630B will generate the RLCLK pulse. For all intervals less than or equal to 100 ns but greater than 5 ns, U630A will generate the RLCLK pulse. For the remaining intervals (greater than 100 ns), flip-flop U540C will generate the RLCLK pulse.

First, consider the case of the slow sampling intervals (greater than 100 ns). In this case, $\overline{\text{SLO}}$ will be asserted and 5NS will be low, so U620C will be disabled and its output will be low. After the pre-trigger hold-off period and when not in program mode, the output of U620D will also be low, so the U540C set input (pin 3) will be low and it will accept clock pulses.

Figure 3-25 shows the timing relationships of the Trig Loc, TCDEC, TB and RLCLK signals. TB pulses are generated at the selected sampling interval; one is generated each time the pre-scaler and decade dividers reach terminal count. Each TB pulse shifts one sample into the data memory shift registers. After eight TB pulses, the group of eight samples collected in the shift registers will be written into the data memory. Because the trigger can occur at any point while collecting samples in the shift register, the time base must remember the location of the trigger within the group of eight samples. The Trig Loc pulse will go high at the sample where the trigger occurred in each group of eight samples. For example, if the trigger occurred on the third sample of the group, Trig Loc will go high on the third sample of each group for the rest of the acquisition.

Because breakpoints are always located at multiples of eight samples from the trigger location, a Trig Loc pulse will occur at each possible breakpoint location (every eighth sample after the trigger). When the decade divider reaches terminal count, TCDEC will go high. If Trig Loc is high at that time, TCDEC will clock the $\overline{Q}$ output of U540C low. The next time TCDEC goes high, TRIG LOC will be low, and the $\overline{Q}$ output of U540C will go high. This positive transition of RLCLK will latch the new sampling interval.

If the time base is sampling at 100 ns intervals or some faster rate, only the pre-scaler divider is used, and the RLCLK pulse does not need to be synchronized with TCDEC. For these intervals, $\overline{SLO}$ will not be asserted and 5NS will be low. Except during the pre-trigger hold-off or during programming, the output of U620D and pin 6 of U630A will be low (the high on $\overline{SLO}$ disables U630A) when Trig Loc is low. When Trig Loc goes high at the trigger location in the eight-sample group, the output of U620D will go high, asserting RLCLK and latching the sampling interval code from the RAMs.

When the time base is sampling at five ns intervals, U630B will generate the RLCLK pulse. In this case 5NS will be asserted and the output of U620D will be low as previously discussed. Because of the propagation delays involved in the interval switching logic, Trig Loc is not used to generate the pulse. Instead, TL6 is used because TL6 is asserted two TB pulses before the trigger (earlier than Trig Loc) to compensate for the propagation delay through the switching logic.

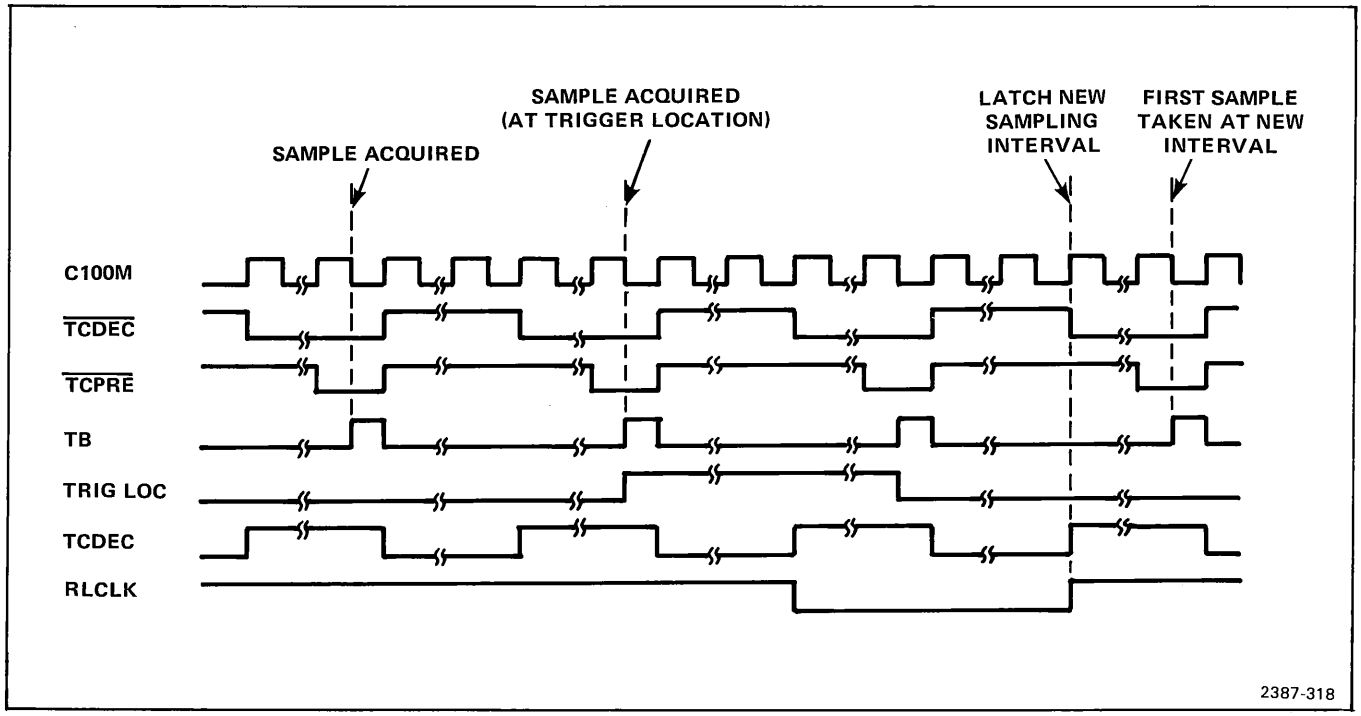


Figure 3-25. Timing of the RLCLK pulse.

10 DATA MEMORY CONTROL

The Data Memory Control diagram shows the trigger control, trigger locator, and memory-address generator circuits. The trigger control circuit selects valid trigger signals from the designated source, left or right. The trigger locator circuit "remembers" where a valid trigger occurs during a data acquisition. The memory-address generator produces addresses that direct the storage of data in memory.

TRIGGER CONTROL

The trigger control circuit is a logic circuit that permits a valid trigger signal to start a time-base operation, and determines which trigger signals are valid ones.

Gates U530A and C receive the trigger signals from the Left and Right Trigger circuits. Flip-flop U526A selects which trigger will be used. The outputs of U530A and C are wire-ORed with the Q outputs of FFs U510B and U516A, and will therefore be able to clock U526B only when U510B and U516A are cleared. Flip-flop U510B will be cleared in the normal trigger mode. In B triggers after A mode, U510B will be set until a B EOP pulse from Time Base A clears it. Flip-flop U516A will be cleared when:

a. the Time Base is in special-delay mode, or

b. a $\overline{\text{TB/8}}$ pulse ends while EPOPM and $\overline{\text{PTHOE}}$ are low.

After U510B and U516A are cleared the next trigger, from the selected trigger channel, will clock FF U526B, which will assert the STRT level. (STRT means "get ready to stop.") STRT indicates the time when the trigger occurred.

Pretrigger Holdoff Generator

The pretrigger holdoff generator produces the $\overline{\text{PTHOE}}$ (pretrigger holdoff end) signal, which is used in the trigger control circuit. The generator consists of inverters U410A and D and gates U326A, B, and C.

When the memory-address counter has counted one record length, the pretrigger holdoff generator will produce a $\overline{\text{PTHOE}}$ signal. One record length will have occurred when:

a. U230 reaches terminal count and produces a low on its pin 4 output, and

b. U226 has a high on its pin 3 output, and

c. U326B is activated by U226 or U310, and

d. U326C is activated by U226 or U310, and

e. U326A is activated by U226 or U310.

Figure 3-26 shows the devices that can assert $\overline{\text{PTHOE}}$.

MEMORY ADDRESS GENERATOR

At the start of a write operation:

1. The EPOPM pulse will reset U226 and U230. (PGM causes U316C to produce EPOPM.)

2. Lows on $\overline{\text{Write}}$ and HOFST disable U316B, making all CS lines low.

3. BFTB pulses will shift data from the target into the shift registers on the Data Memory (diagram 7).

4. A $\overline{\text{BFTB/8}}$ pulse will latch the content of the shift registers into latches U302, U312, U322, and U324 (diagram 7).

5. The Data Memory Control (diagram 10) will produce a write enable ($\overline{\text{WE}}$) signal as follows: $\overline{\text{Write}}$ enables U136D, and TB4 activates U136D to produce $\overline{\text{WE}}$, which stores data from the latches into the RAMs.

6. After the data is stored, the clock memory address counter (CMAC) signal from U006C will increment the MAC to select the next memory address. The low on $\overline{\text{TB/8}}$ disables U006C when $\overline{\text{BFTB/8}}$ enters data into the latches, and U006C's low CMAC output stops U230 and U226 from incrementing. When a high on $\overline{\text{TB/8}}$ activates U006C, CMAC will go high and clock the MAC, which then selects the next memory address.

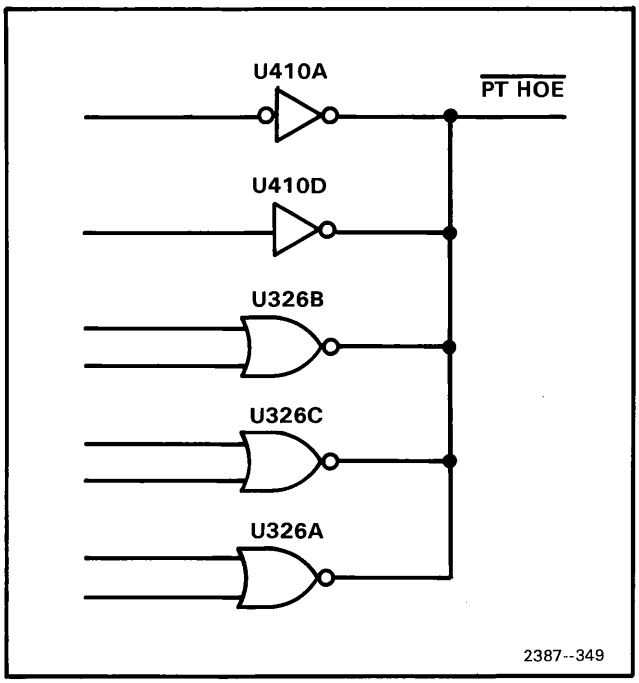


Figure 3-26. Devices that can assert $\overline{\text{PT HOE}}$.

The outputs of U230 and U226 become the memory address signals, DADR0-DADR7. The lower five lines, DADR0-DADR4, go directly to the memory. The other three lines reach the memory via the record-length gates.

Setting the Record Length

The record length is determined by the levels on the DADR7, DADR6, and DADR5 lines.

To select a 2048-word record, lows from record-length latch U310 will enable U336D, C, and A, and disable U330D, C, and A. In this condition the outputs of counter U226 will activate the U336 gates that drive the DADR7, DADR6, and DADR5 lines.

To select a 1024-word record, a high from U310 will disable U336D and enable U330D. Then the outputs of counter U226 will activate the DADR6 and DADR5 lines. The PC0 line from partition counter U220 (diagram 8) will then designate which 1024-word record will receive the data.

To select a 512-word record, highs from U310 will disable U336C and D, and enable U330C and D. In this situation the outputs of counter U226 will activate the DADR5 line. The PC0 and PC1 lines from partition counter U220 (diagram 8) will then designate which of the four 512-word records will receive the data.

Selecting a 256-word record is the same process as for a 1024- and 512-word records. Then U336D, C, and A will be disabled and U330D, C, and A will be enabled. Counter U226 then cannot activate the DADR7, DADR6, or DADR5 lines; instead the PC0, PC1, and PC2 lines from partition counter U220 on diagram 8 designate which of the eight 256-word records will receive the data.

7. The next $\overline{\text{BFTB/8}}$ pulse latches data from the shift registers into latches U302, U312, U322 and U324 (diagram 7).

8. A low on TB4 will activate U136D, whose $\overline{\text{WE}}$ output will store the data from the latches into the RAMs.

9. When $\overline{\text{TB/8}}$ goes high, U006C produces another CMAC pulse.

To display this stored record, a low on load memory address counter ($\overline{\text{LMAC}}$) will load the start-of-record address into U230 and U226. CMAC pulses then increment the MAC and the $\overline{\text{WE}}$ line stays high to read data from the memories.

TRIGGER LOCATOR

The Trigger Locator provides a means of referencing timebase operations to the occurrence of a valid trigger signal.

While the 7612D is storing data, lows on HOFST and $\overline{\text{Write}}$ will disable U316B, whose low output will cause all CS lines to be low. Eight words will be stored at one address in eight Data Memory RAMs. Then the memory address will be incremented by one and eight more words will be stored at the new address, and so forth until enough words have been stored. If the memory is being used, when memory address 255 is reached, eight times 256=2048 words will have been stored. If no trigger has occurred, the memory address counter (MAC) will reset to zero. Because the MAC was reset, new data will be written over previously stored data at address zero.

If a 2048-word record is selected, and if pre-trigger is set to 2032, there will be 16 words stored after the trigger occurs (2048-2032=16). Let's consider an example where the trigger occurs at chip select 1 of memory address 149. Figure 3-27 shows a representation of the memory and its address.

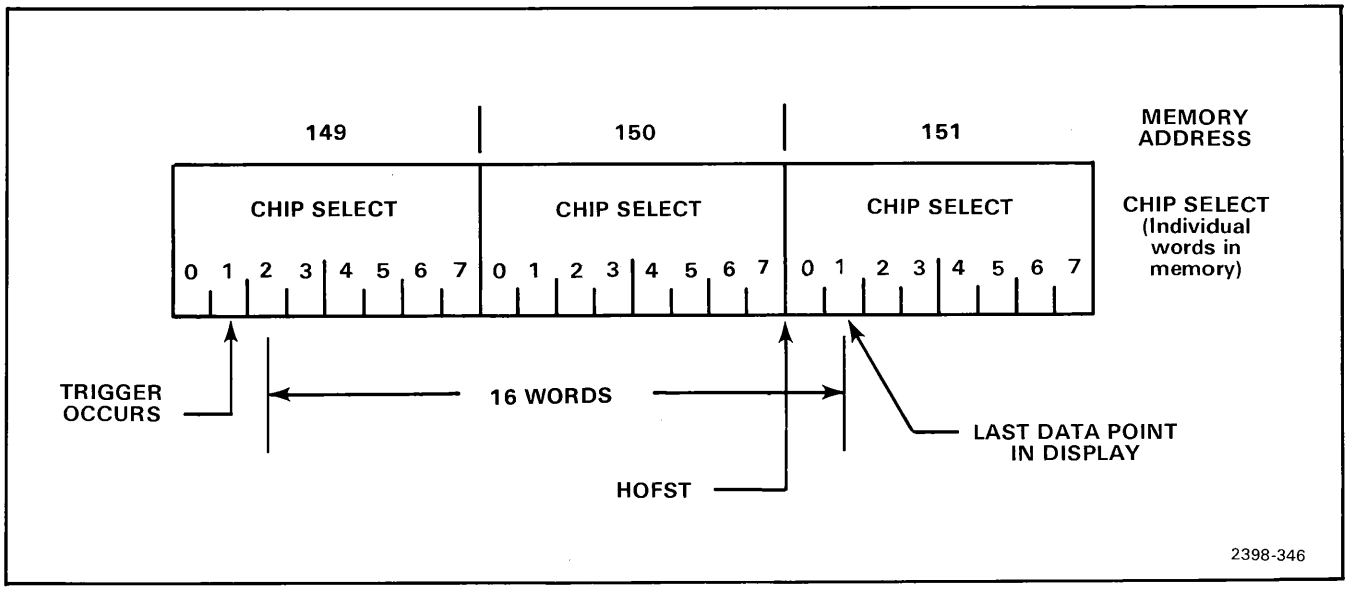


Figure 3-27. Locations of trigger, HOFST, and last data point with 2048-word record and 2032-word pre-trigger, when trigger occurs while memory address 149 is receiving data.

The following sequence of events will determine the end-of-record point.

Shift register U440 counts eight cycles of TB from the trigger; it does this by shifting a bit from its Q0 toward its Q7 output. U440 is in shift-left mode because:

a. Lows on TL5 and $\overline{\text{Write}}$ activate U246B, whose high output is clocked into U346C by PLCK. U346C asserts a high on the S0 line.

b. Lows on $\overline{\text{Write}}$ and HOFST disable U146B, which asserts a low on S1.

U340C and D generate PLCK for U440.

Table 3-7 shows how the S0 & S1 inputs determine U440's operating mode.

TABLE 3-7
Control Inputs vs. Operating Mode of U440

S0	S1	Mode
L	L	Load or latch new data.
L	H	Shift right (up, Q7 toward Q0), 7612D read mode.
H	L	Shift left (down, Q0 toward Q7), 7612D write mode.
H	H	Hold.

Because STRT is low before a trigger occurs, each PLCK will have entered a low into U440; its outputs will all be low.

When the trigger occurs, STRT will go high and PLCK #0 will enter a high into U440 Q0; U440 pin 5 will go high. (This is important only for record-keeping just now because the CS lines are all disabled by U316B.) Subsequent PLCK pulses will shift the high toward U440's Q7 output. The fifth PLCK will clock U440's pin 12 output high, and TL5 will disable U246B, causing a low to the D input of U346C. PLCK #6 will clock that low into U346C, which will assert a low on the S0 line. The low on S0 puts U440 in load mode. (Meanwhile, PLCK #6 also shifted the high to U440 pin 13, the TL6 line.) PLCK #7 will load U440. Because the 7612D is in write mode, Write will be low and will disable the eight gates that supply the P0-P7 inputs to U440. PLCK will load all zeros into U440; it will be as it was before the trigger occurred. PLCK #7 also clocks a high from FF U346C pin 8 into FF U346B, whose Q output will assert a high on the S0 line. The high on S0 will put U440 in shift-left mode. U440 will then contain all zeros. STRT will still be high because the trigger clocked U526B. The sequence will start again in response to PLCK pulses, and U440 will recycle every eight PLCK pulses. It will start counting when the trigger occurs.

The count in U440 at any time indicates how many PLCK pulses have occurred since the trigger. U440 will continue this cycle until holdoff start (HOFST) occurs. HOFST will go high after the trigger-location counter (U210 and U220 on diagram 8) indicates that a complete record has been stored into a particular address (when the last chip select occurs). In this example, HOFST occurs at the end of address 150, which is at CS7 of address 150, because address 150 is the last address that will receive eight words (eight chip-select signals). When HOFST occurs at address 150, chip-select 7, it sets U346C and activates U146B. Flip-flop U346C then asserts a high on S0 and U146B asserts a high on S1. These two highs put U440 in hold mode. U440 will have highs on its Q0 through Q5 outputs for two reasons:

1. It was reset to zero at CS1, and

2. Six additional PLCK pulses were needed to advance from CS1 to CS7 (the Q6 and Q7 outputs will be low).

The high on HOFST enables chip-select gates U430 and U436. The highs on U440's Q0 through Q5 outputs will activate gates U430C and B and U436B, C, F, and A, which will assert highs on the CS7, CS6, CS5, CS4, CS3, and CS2 lines. The highs on these CS lines prevent the associated memory chips from accepting new data. The lows on U440's Q6 and Q7 outputs will disable U436D and E, which will assert lows on the CS1 and CS0 lines. Because only the CS1 and CS0 lines are low, the next write enable (WE) pulse will store data only in the 0 and 1 chips of the next address (151 in this example), which was where we wanted the last data word stored.

To read this record from the memory, we want to start with the "oldest" data, which is located at address 151, chip-select 2.This will be the point adjacent to the newest (last) point stored, in address 151, chip-select 1 in this example. The memory address is stored in RAMs U236 and U320; the chip-select information must be stored.

U520 is a priority encoder whose output is a BCD version of its lowest-numbered high input. (In this case, when inputs D0 and D1 are low and D2-D7 are high, U520's output is 010. If D5 were the lowest-numbered high input, its output would be 101.) The output of U520 goes to RAM U426; the address inputs are the PC0-PC3 lines (the same lines that address RAMs U236 and U320). End Record ($\overline{\text{ER}}$) writes the chip-select information into U426 at the same time that the memory address is stored in U236 and U320.

To start reading data from memory, the system must first determine a starting point, which takes place as follows. The microprocessor will assert, by sending PTNRST and (15−record number) of PTNADV pulses to U220 on the PC0-PC3 lines, the address where the lowest output data from U520 was stored in RAM U426 for the record being read. The output of U426 will be the code that represents the lowest Q output of U440 that had a high output (Q5 in this example). The output of U426 goes to decoder U416, which asserts a low on the output that corresponds to the decimal value of its input. If the input is 010, the output will be a low on Q2 only. The output of U416 goes to gates U420 & U430, which will be enabled only during a read operation by a high on Write. In a read operation, one gate will

be disabled and will apply a low to one input of shift register U440 (U420D to U440 pin 18 in this example); the other gates will be activated and will apply highs to U440.

Lows on TL5 and $\overline{\text{Write}}$ will activate U246B, which will apply a high to the D input of U346C. The low $\overline{\text{Write}}$ will also disable U026A, which will apply a low to U146B pin 4. The low on HOFST will disable U146B, which will apply a low to the S1 line. The MPU will then remove PGM, $\overline{\text{Write}}$ will go high, and the MPU will assert LMAC. Gate U246B will be disabled by the high $\overline{\text{Write}}$ and will apply a low to the D input of U346C. The next PLCK will clock the low into U346C, which will assert a low on the S0 line. When S0 and S1 are low they put U440 in load mode; U440 will then accept the data at its inputs. Only the pin 18 input is low in this example, so U440's Q5 output will be low, which will disable U436A (all other gates will be activated because of highs from U316B and U440's other high outputs). When disabled, U436A will assert a low on the CS2 line. This designates CS2 as the starting point for the read operation.

To start a read operation, the MPU will do two things. First it will reset U220 with the PTNRST signal. Then, after resetting U220, the MPU will advance U220 with a number of PTNADV pulses. The number of PTNADV pulses will be (15 − number of records stored) + (number of the desired record − 1). For example, if we are storing three records and we want to read the second one, the microprocessor will send (15 − 3) + (2 − 1) = 12 + 1 = 13 PTNADV pulses to U220.

The low on Write will disable U006C and enable U100B. When the first read cycle signal ($\overline{\text{FRS}}$) goes low it will activate U100B, whose output will set FF U110B, and U110B will assert LMAC and $\overline{\text{LMAC}}$ (load memory address counter). The highs on LMAC and $\overline{\text{Write}}$ will activate U026D, whose high output will enable U006D. Read ($\overline{\text{RD}}$) pulses can then activate U006D, via U300D, to produce CMAC (clock memory address counter) pulses. When $\overline{\text{LMAC}}$ goes low it will put the memory address counter in load mode, and via U026A and U146B, will put U440 in load mode by applying a low to U440's S1 input. The first $\overline{\text{RD}}$ pulse will:

1. cause CMAC to clock the stored address from RAMs U236 and U320 into counters U230 and U226, and

2. via the Sample Interval Generator, cause PLCK to latch new data into shift register U440.

The first CMAC pulse also clocks FF U110B, causing its output to revert to a low on LMAC and high on $\overline{\text{LMAC}}$. The high on the $\overline{\text{LMAC}}$ causes three effects, as follows:

- It will prevent the MAC from loading new data.

- It will activate U026C, whose high output will enable U006B and hold U346C cleared. While $\overline{\text{LMAC}}$ is high, the TL signal will become CMAC via U006B. Because U346C is held cleared it will assert a low on the S0 line.

- It will activate U026A, whose high output will activate U146B to apply a high to the S1 line. The high on S1 and the low on S0 put shift register U440 in shift-right mode.

Subsequent $\overline{\text{RD}}$ pulses will clock the low in U440 toward its Q0 output. (U440 received one low and seven highs when it latched new data as described in 2.) When the low reaches U440's Q0 output, it will go low. This will disable U006B and end the first CMAC pulse. The next $\overline{\text{RD}}$ pulse will shift the low from the Q0 to Q7 output, TL will go high again and via U006B, produce another CMAC. This will advance the memory address counter to the next address. Figure 3-28 shows this timing.

This process will continue until the record has been completely read, when the microprocessor will stop sending $\overline{\text{RD}}$ pulses.

11 VERTICAL AMPLIFIER

The Vertical Amplifier accepts input signal(s) from the plug-in amplifier(s) via the Plug-In Interface, amplifies, and presents the signal(s) to the deflection plates of the EBS tube(s). Because the A and B channels are identical, only the A channel will be described here.

The input stage is composed of common-emitter amplifier Q716-Q712 and common-base amplifier Q714-Q710. The input signal reaches Q716 and Q712 via T-coils that are integral parts of the circuit board. These T-coils terminate the output of the plug-in amplifier in 50 Ω and provide frequency response peaking. Resistor R712 sets the low-frequency gain of the Q716-Q712 stage. Resistors R714 and R710 provide thermal compensation for the input stage. The RC networks of R715 and C715, R711 and C711 are high-frequency bypasses for the thermal compensation resistors. Resistors R617 and R618 set the low-frequency gain of Q714 and Q710. Transistors Q620 and Q626 form a pickoff amplifier that provides the OR (OverRange) signal for the Data Memory. The output of Q714 and Q710 goes to the output stage via T-coils.

The output stage consists of common-emitter amplifier Q514, common-base amplifier Q508 and Q518, and dc level-centering transistors Q512 and Q516. When a large signal is present, diodes CR614 and CR615 act to increase the gain of Q514A and B. This compensates for compression in the amplifier. Controlling the amount of dc current in Q512 and Q516 with R407 and R408 determines the dc level at the crt deflection plates.

Inductors L500 and L512, provide high-frequency peaking for Q508 and Q518. H811 provides high-frequency peaking and termination for the deflection plates of the EBS tube. Zener diode VR400, CR400, and Q410 provide about +38.2 V for the output stage.

12 HIGH VOLTAGE/CRT

The High Voltage/CRT diagram shows the circuitry that produces high voltages to operate the electron-bombarded semiconductor (EBS) tubes. The EBS tubes need −10 kV for their cathodes, about −10.04 kV for their control grids, and −3290 V and −2470 V, respectively, for the two focus electrodes.

A regulated high-voltage oscillator produces −10 kV. Individual peak-to-peak detectors referenced to the −10 kV generate negative bias voltages for the control grids of the ebs tubes. Individual circuits provide X and Y alignment, X position, and trace rotation for the two EBS tubes.

HIGH-VOLTAGE OSCILLATOR

Transistor Q002, T110 and related components compose the High-Voltage Oscillator, which produces the heater voltage for the EBS tubes and a high-amplitude input for the voltage quadrupler. The amplitude of Q002's oscillation is governed by Q906 in the Regulator, which conducts Q002's base current.

VOLTAGE QUADRUPLER (A74)

The Voltage Quadrupler rectifies, filters, and multiplies the ac output of T110 to produce −10 kV.

REGULATOR

Regulator U808 compares a sample of the −10 kV with ground potential and, by governing the Q906 output current, controls the output amplitude of oscillator Q002. If the −10 kV output should exceed −10 kV, U808 output will go more positive and reduce the conduction of Q906. Less current from Q906 will reduce the amplitude of Q002's oscillation and return the −10 kV output to its correct value.

The reverse sequence of events will take place if the −10 kV is low (less than −10 kV). In this situation the input to U808 will go more positive and U808 will produce a more negative output that will cause Q906 to conduct a greater current. The increased current from Q906 will increase the amplitude of Q002's oscillation and return the output to its correct value.

GRID BIAS SUPPLY

Two groups of identical circuitry provides grid bias for both EBS tubes. Only the circuitry for the "A" Channel tube is described here.

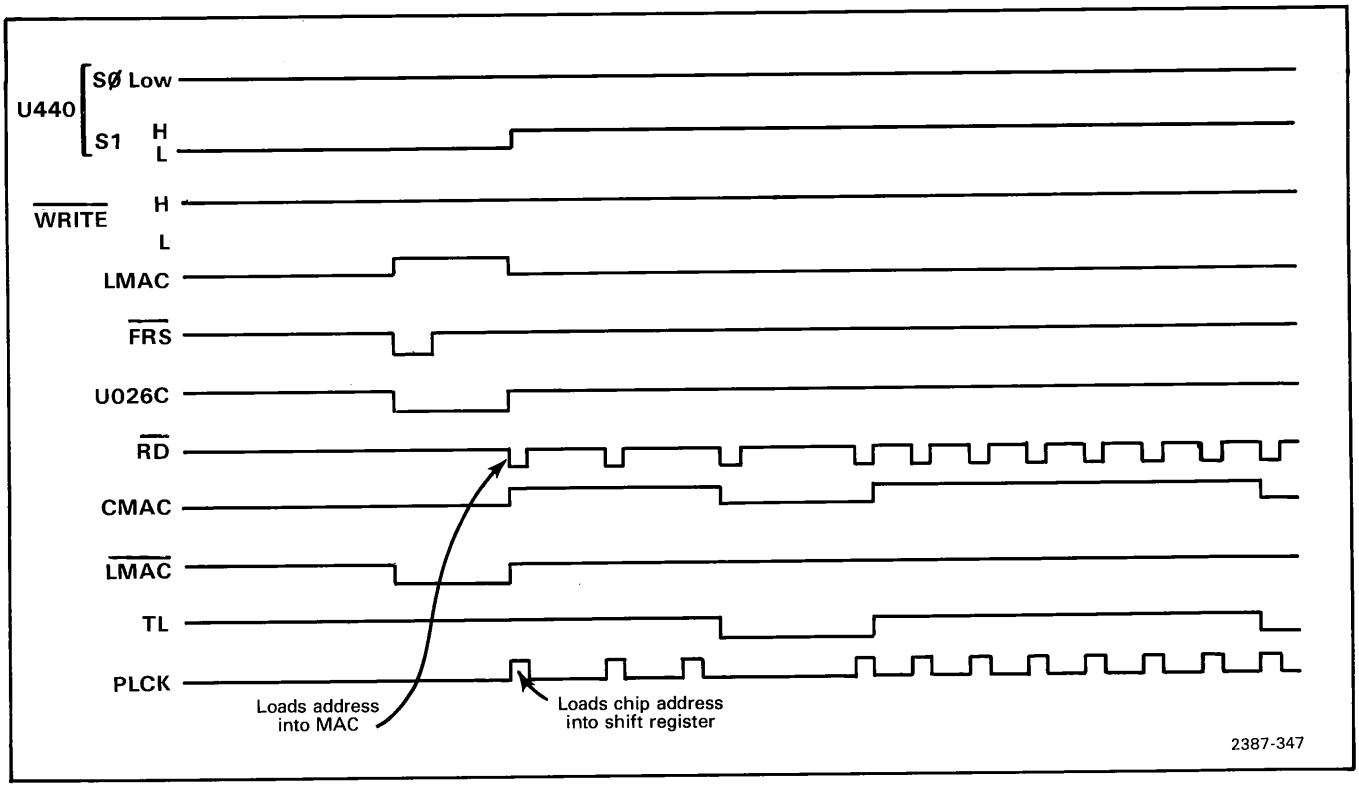


Figure 3-28. Timing of trigger locator and memory-address generator during a read operation.

Diodes CR946 and CR948 clamp the positive and negative excursions of the square wave from transformer T110 pin 2. The clamped square wave then reaches the input of the peak detector, which is shown inside the heavy border marked A72 Grid Supply. The peak detector produces a dc voltage equal to the peak-to-peak value of the clamped square wave, and applies it to the control grid of the EBS tube. This dc voltage sets the beam current in the EBS tube. Grids 2, 3, and 5 of the EBS tube sense beam current and apply a feedback voltage to pin 2 of U930A. Voltage follower U930A applies the sum of this feedback and the output of R306, the I_bA adjustment, to Q936. Transistor Q936 varies the positive voltage for the clamp circuit as needed to maintain a constant beam current.

When the I_bA control, R306, is set to produce 200 mV at TP 333 (see Header, diagram 4), the control grid will be about 40 V more negative than the cathode.

OTHER INPUTS TO EBS TUBES

Each EBS tube must have voltages to align the beam along its X and Y axes, focus voltage, X position voltage, and a means of rotating the electron beam.

Potentiometers and paraphase amplifiers provide means of adjusting the X and Y alignment and X position.

The A Rotation control, R310, controls the conduction of Q306 and Q308 so that up to 130 mA can be passed in either direction through the trace rotation coil.

13 PLUG-IN INTERFACE

Diagram 13 shows the wiring to the connectors for the Channel A and B plug-in units.

14 19 READOUT/7K ACQUISITION

Diagrams 14 and 19 show the 7612D readout acquisition system. The acquisition system has four main parts—the time-slot generator and the analog data multiplexer on diagram 14, and the readout control register and the analog data decoder on diagram 19. The MPU controls the time-slot generator and analog data multiplexer and reads the five-bit output word from the analog data decoder.

READOUT CONTROL REGISTER

The readout control register (U832, bottom-left of diagram 19) is the port through which the MPU controls the time-slot generator. The register address is 0EDF (hex) on the MPU bus. Table 3-8 shows the name and function of each bit in the register. The nonmaskable interrupt enable bit (NMIEN) is not part of the readout system.

TABLE 3-8
Readout Control Register Bits

Bit	Signal Name	Function
4-7	—	Unused
3	NMIEN	1 = enable MPU NMI
2	ROT	1 = assert next time-slot
1	RORST	1 = reset time-slot generator to TS-10
0	BLOKRST	1 = block reset (hold RORST low)

TIME-SLOT GENERATOR

The time-slot generator (TSG) transmits time-slot pulses to the plug-in units. The TSG operates under control of the MPU. Any combination of programmable and nonprogrammable plug-in units may be installed, so the time-slot generator must be able to detect the plug-in type and send parallel time-slot pulses (on the TS-1 to TS-10 lines) to nonprogrammable units and serial pulses on the TS-10 line to programmable units.

The Timeslot, ROT and RORST signals from the readout control register drive two decade time-slot counters (U220 and U224 at the center of diagram 14). Programmable plug-in units source at least 100 μA into the TS-10 line to continuously reset the counter to the TS-10 state which forces it to sum all time-slot pulses in a serial stream on the TS-10 line. Table 3-10 (later in this section) shows the control signal sequence and the resultant states of the time-slot counter for both programmable and nonprogrammable plug-ins. Refer to Table 3-9 as we go through the counter states. The time-slot counter states are indicated with numbers from one to ten with an A or an N to indicate whether the time-slot line is Asserted on Not asserted. For example, in state number 6, nonprogrammable plug-in units have TS-2 asserted and programmable plug-in units have TS-10 asserted.

When the cycle begins RORST (Readout Reset—bit 1) is asserted (high), it will reset the time-slot counters to state number 0. No time-slot lines are asserted in this state. When RORST goes low (state 1), the counter is released to assert TS1 on the next ROT (ReadOut Trigger) pulse. During state 2, bit 0 of the control register (BLOKRST) is set, turning Q728 on and holding RORST low. This prevents the current sourced to TS-10 by programmable plug-ins from resetting the time-slot counter. At state 3 ROT goes high. Because RORST (bit 1) is held low, TS-1 is asserted for both programmable and nonprogrammable plug-in units. TS-1 serves as the synchronizing pulse that tells programmable plug-in units the mainframe time-slot counter is starting a new cycle. Shortly after ROT goes high, the output of U636D (bottom-left of diagram 19) goes low, asserting

TABLE 3-9
TIME-SLOT COUNTER STATES

State Number	Control Reg. Bits			Time-Slot Counter States	
	ROT	RORST	BLOKRST	Nonprog. Plug-In	Prog. Plug-In
0	0	1	0	10N	10N
1	0	0	0	10N	10N
2	0	0	1	10N	10N
3	1	0	1	1A	1A
4	0	0	1	1N	1N
5	0	0	0	1N	10N
6	1	0	0	2A	10A
7	0	0	0	2N	10N
8	1	0	0	3A	10A
9	0	0	0	3N	10N
10	1	0	0	4A	10A
11	0	0	0	4N	10N
12	1	0	0	5A	10A
13	0	0	0	5N	10N
14	1	0	0	6A	10A
15	0	0	0	6N	10N
16	1	0	0	7A	10A
17	0	0	0	7N	10N
18	1	0	0	8A	10A
19	0	0	0	8N	10N
20	1	0	0	9A	10A
21	0	0	0	9N	10N
22	1	0	0	10A	10A
23	0	0	0	10N	10N

A = asserted; N = not asserted

Timeslot. The Timeslot pulse drives a voltage source formed by Q546, Q544, and Q448 left-center (left-center of diagram 14). The output of this circuit supplies the voltage source for the outputs of the time-slot counters.

ROT goes low at state 4 and TS-1 is unasserted. Then bit 0 of the control register goes low, Transistor Q728 (diagram 19) turns off and RORST is allowed to float. Next the reset current from programmable plug-in units forces the time-slot counters to reset to TS-10. If a nonprogrammable plug-in unit is installed, no current is sourced on TS-10 so the counter counts up normally with each ROT pulse as shown in Table 3-9. The reset current from programmable plug-in units resets the time-slot counter after each ROT pulse, so the counter sends all the pulses on TS-10. This cycle continues as shown in Table 3-9 until state 23, when the cycle is repeated and another TS-1 pulse is sent to tell the plug-in unit that a new cycle is beginning. The resultant pulse trains for programmable and nonprogrammable plug-in units are shown in Figure 3-29.

ANALOG DATA MULTIPLEXER

The plug-in units return row and column current levels to the mainframe during the time-slots that define the characters in the readout word. The current levels are time-multiplexed to four pairs of row and column lines—one pair for each channel of the vertical and horizontal plug-in units. The analog data multiplexer, under the control of the MPU, demultiplexes the analog data and feeds it to the analog data decoder. The MPU controls the multiplexer through an eight-bit serial shift register, U120 at the top-left of diagram 14. The MPU selects one multiplexer channel by writing to the shift address (OEBF) up to eight times. Each time, SHIFT is asserted and the state of $\overline{BD0}$ is shifted into the first bit (Q_A) of the register. On successive SHIFTs, the current state of $\overline{BD0}$ is shifted toward Q_H. Table 3-10 shows the data selected by each channel of the multiplexer. The $\overline{BD0}$ line is asserted for only one of the eight shifts, so only one of U1200's output is low. The low on this output forward-biases the output transistor for the selected channel. For example, if Q_A is low, the emitter-base junction of Q020 is forward biased and the analog current on this line is fed to the Analog Data Decoder. Transistors Q_B through Q_H are high, so the emitter-base junctions of the other output transistors are reverse-biased.

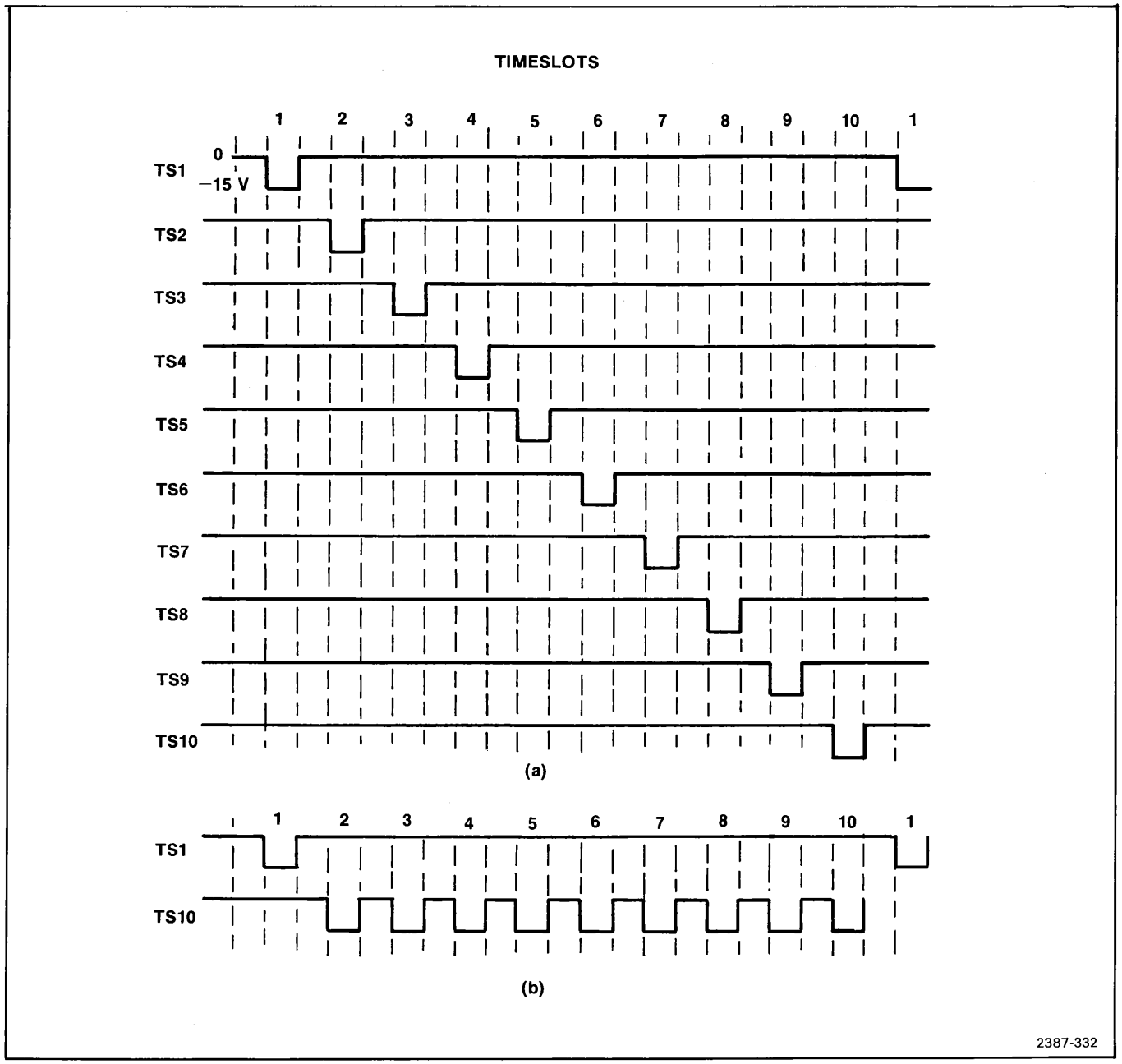


Figure 3-29. Timing of time-slot pulses for programmable and nonprogrammable plug-in units.

TABLE 3-10
Analog Data Multiplexer Channels

Channel	U120 Pin No.	Data Selected		
		Plug-in Compartment	Channel	Row/Column
1	3	Left vertical	1	Row
2	4	Left vertical	1	Column
3	5	Left vertical	2	Row
4	6	Left vertical	2	Column
5	10	Right vertical	1	Row
6	11	Right vertical	1	Column
7	12	Right vertical	2	Row
8	13	Right vertical	2	Column

ANALOG DATA DECODER

The Analog Data Decoder (U926, left-center of diagram 19) converts the current levels it receives from the analog multiplexer to a binary code. The MPU reads this code from the readout data register located at OEEF in the MPU address space.

The analog data is fed to current-input A/D converter U926 through a divider network. Potentiometer R932 provides an adjustment for correcting minor variations in the analog current levels. U926 converts the analog current to a one-of-ten (0-9) code. One output is asserted for each level between 100 and 900 μA; no outputs are asserted for a 0 μA input. U912 converts this one-of-ten code to its four-bit BCD equivalent and U814 buffers the data onto the MPU bus.

If the analog input current reaches 1.0 mA, the output of comparator U836 goes high, clearing bit 7 (BD7) of the readout register. Table 3-11 shows the output codes for each analog input current.

READOUT QUERIES

When the MPU receives a vertical scale factors query (VSL1?, VSL2?, VSR1?, VSR2?) or readout query (RD0?), it uses the information acquired through the readout acquisition system to respond.

15 16 MPU MEMORY & SELECT MPU MEMORY

Diagram 15 shows the circuitry that selects the ROMs shown on diagram 16.

The MPU Memory Board (A52 on diagram 16) contains the MPU system ROM, RAM and buffers.

Integrated circuit U311 (right side of diagram) is a bidirectional data bus buffer. When the MWR line is low (MPU writing data into memory), the $\overline{\text{MRD}}$ line will be high and the buffer will be enabled for input to the memory. If R/$\overline{\text{W}}$ is high (MPU reading data from memory), $\overline{\text{MRD}}$ will be low and the buffer will be enabled for output from the memory. Bidirectional data flow is disabled when $\overline{\text{ANSR}}$ goes high. This occurs only when all memory select lines (diagram 15) are unasserted.

RAM MEMORY

Two 1024 by four-bit RAM packages, U501 and U511, comprise the MPU memory. When $\overline{\text{MEMSEL}}$ 0 is asserted both chips are selected to provide eight bits of memory. The RAM is read when $\overline{\text{MWR}}$ is high and write-enabled when $\overline{\text{MWR}}$ is low.

ROM MEMORY

The 7612D firmware operating system is resident in eleven 2k eight-bit ROMs. Each of these chips is selected by one of the $\overline{\text{ROMSEL}}$ lines from diagram 15. U101, U201, and U411 buffer the three banks of ROM to data-bus buffer U311. These banks are selected by the $\overline{\text{BANKSEL}}$ lines from diagram 15.

MEMORY-SELECT LOGIC

Individual ROM chips in the MPU memory are selected and enabled by the MPU Memory Select logic shown on diagram 15. This logic decodes addresses on the MPU bus and enables the appropriate ROM.

TABLE 3-11
Readout Data Register Codes

Analog Input Current	Output Code								Row No.	Column No.
	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0		
0 mA	1	X	X	X	1	1	1	1	1	0
0.1 mA	1	X	X	X	1	1	1	0	2	1
0.2 mA	1	X	X	X	1	1	0	1	3	2
0.3 mA	1	X	X	X	1	1	0	0	4	3
0.4 mA	1	X	X	X	1	0	1	1	5	4
0.5 mA	1	X	X	X	1	0	1	0	6	5
0.6 mA	1	X	X	X	1	0	0	1	7	6
0.7 mA	1	X	X	X	1	0	0	0	8	7
0.8 mA	1	X	X	X	0	1	1	1	9	8
0.9 mA	1	X	X	X	0	1	1	0	10	9
>1.0 mA	0	X	X	X	X	X	X	X	14	10

The selection occurs in two parts. First, the address decoders shown in the center of diagram 17 generate the MEMSEL (Memory Select). One MEMSEL line is provided for each 4k bank of addresses. For example, all addresses in the range 1XXX (hex) cause MEMSEL1 to be asserted.

The MEMSEL lines connect to the MPU Memory Select logic where the second stage of the selection occurs. Here, each 4K bank is divided into two 2k banks by gating the MEMSEL signals with bit 11 of the MPU address bus (MA11). When MA11 is low, the low-order half of a 4k block is selected (e.g., ROMSEL10, ROMSEL20, etc.). When MA11 is high, the high-order block is selected (e.g., ROMSEL18, ROMSEL28, etc.).

MWR is also gated by the MEMSEL lines so that when the MPU is writing data on the bus (MWR is low) the ROMs are disabled.

The BANKSEL0, 1 or 6 lines are asserted when the appropriate MEMSEL lines are addressed. Setting the MEMSEL lines high disables the corresponding ROM bank on diagram 16. When all of the MEMSEL lines are high, ANSR is high, disabling all data flow to and from the MPU Memory.

MPU

Figure 3-30 shows a block diagram of the microprocessor (MPU) system in the 7612D. The MPU is the instrument master controller. It accepts and decodes commands from the front-panel or the IEEE 488 bus and sets instrument operating parameters in response to these commands. The MPU also controls the IEEE 488 interface and provides a transparent bus interface to programmable plug-in unit.

A 15-bit address bus and an eight-bit data bus provide the communication path between the MPU, MPU memory, and the instrument functions it controls. A set of bus buffers provides drive for the internal buses and generates select signals that allow the MPU to selectively communicate with each of the functions it controls. We will discuss the MPU bus in more detail later.

When one of the instrument functional blocks requires the MPU's attention, it asserts an interrupt line that sets a bit in the interrupt occurred register. The Interrupt Control logic signals the processor that an interrupt has occurred. If the MPU has not disabled (masked) interrupts, it temporarily suspends execution of the current task and jumps to a routine that determines the source of the interrupt. Then control

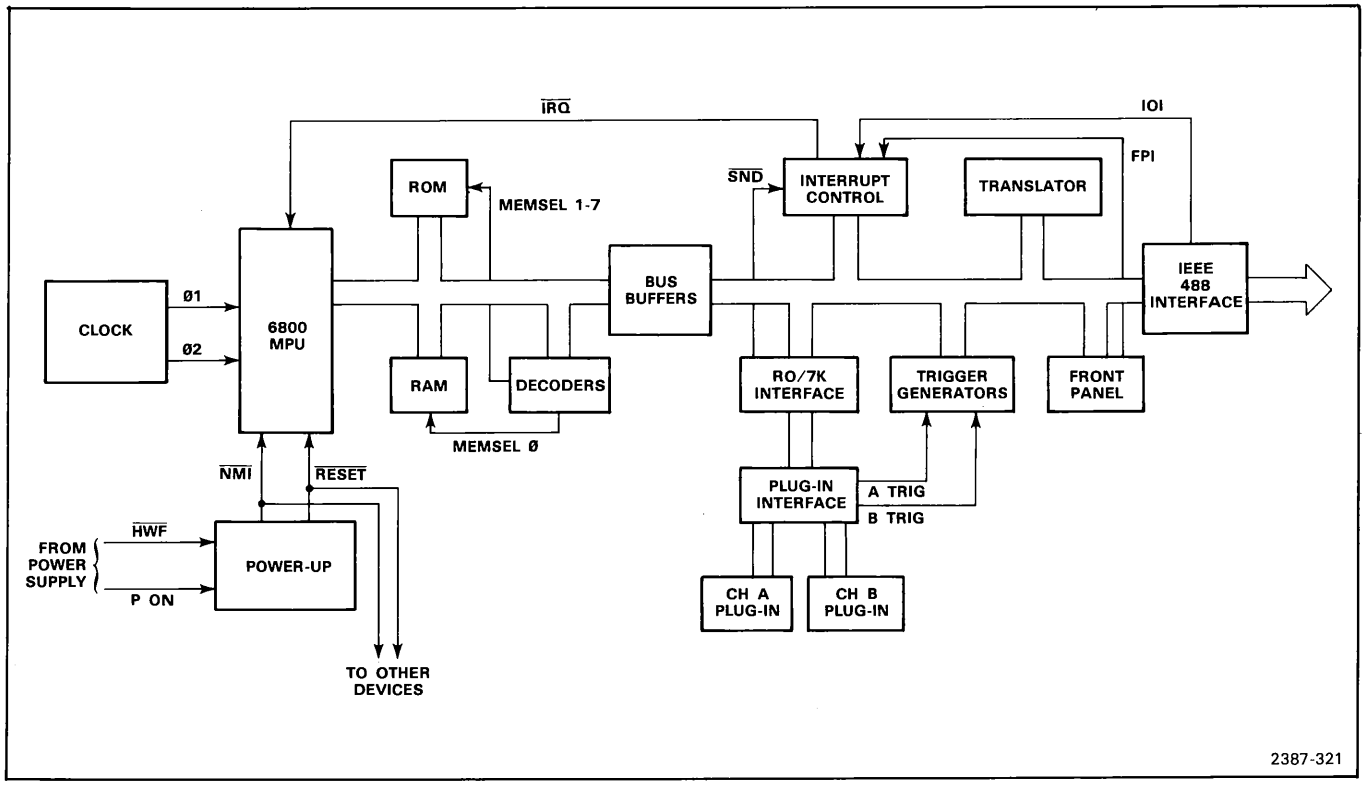


Figure 3-30. Block diagram of the MPU system.

is passed to an appropriate service routine. For example, assume the operator has just pressed a front-panel button. The MPU receives an interrupt from control logic. It suspends execution of the current task and reads the interrupt occurred register to determine the source of the interrupt. Then control is passed to a routine that services that interrupt. Finally, the processor resumes execution of the previous task. We'll discuss the interrupt sequence in more detail in the interrupt control logic area.

The firmware operating system that directs the MPU's activity is resident in 22k (1k = 1024) bytes of ROM on the MPU Memory Board (A52).

The MPU system also uses 1k bytes of RAM (Random-Access Memory) as a "scratch pad." A limited amount of the RAM space is available for diagnostic purposes.

MPU ARCHITECTURE

Before we discuss the microprocessor system as it is used in the 7612D, we will briefly review the MPU.

For more information on the MPU, refer to the Motorola M6800 Microcomputer Design Data Manual. Figure 3-31 shows a block diagram of the MPU internal architecture.

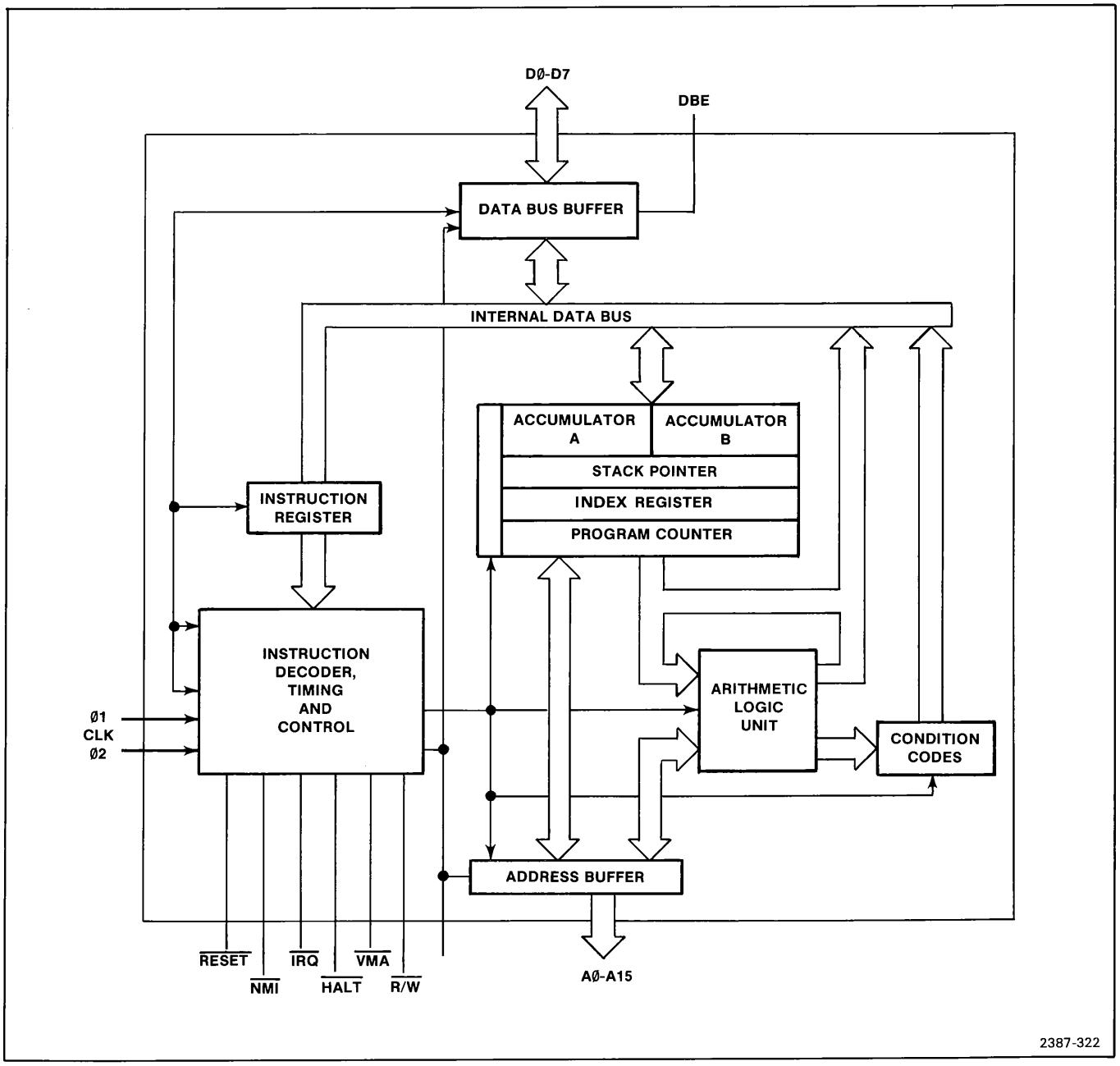


Figure 3-31. Block diagram of the MPU internal architecture.

The MPU is an eight-bit parallel processor with an eight-bit bidirectional data bus and a 16-bit address bus. The MPU consists of the following functional units:

Two eight-bit Accumulators
Program Counter
Stack Pointer
Index Register
Condition Code Register
Instruction Register and Decoder/Timing
Data and Address Buffers

Accumulators. The accumulators are used to hold operands and the results of ALU operations.

Condition Code Register. The condition code register indicates the result of ALU operations. Single bits in the register indicate a negative result (N), a zero result (Z), and overflow (V), carry from bit 7 (C), and half carry from bit 3(H). These bits are used by the conditional branch instructions in the MPU instruction set. Bit 4 of the condition code register masks the MPU's $\overline{IRQ}$ input. When set, the MPU ignores interrupts on the $\overline{IRQ}$ input. Unused bits (6 and 7) in the register are ones.

Program Counter. The program counter register contains a 16-bit address that points to the current program instruction.

Stack Pointer. The stack pointer is a 16-bit address that points to the next available memory location in the external LIFO (Last-In-First-Out) "stack." This stack is used to store the contents of the MPU registers when an interrupt occurs or when the MPU executes a subroutine. The stack is usually located at the highest RAM memory address and it grows toward lower memory addresses as data is added to it. The stack pointer is automatically decremented when data is "pushed" onto the stack and incremented when data is "popped" off.

Index Register. The index register can be used to store 16-bit data or an address used in the indexed mode of memory addressing. Instructions are provided in the MPU instruction set that load, increment, decrement, compare, etc. the index register.

Instruction Register and Decoder/Timing. During an instruction fetch (the first one, two, or three machine cycles, depending on the instruction), successive bytes of an instruction are loaded from the program memory into the instruction register. The contents of this register are, in turn, passed to the decoder and timing logic which decodes the byte(s) and generates the machine states and control signals necessary to execute the instruction. The timing and control block also generates and receives the external control signals.

Data and Address Buffers. These three-state buffers isolate the MPU internal buses from the external data and address buses. The data bus buffer is bidirectional.

THE INSTRUCTION CYCLE

The MPU is driven by a two-phase nonoverlapping clock. A machine cycle is defined as the interval between two successive positive-going transitions of the phase-one clock signal. An instruction cycle consists of from 2 to 12 machine cycles required to fetch and execute the instructions. The number of machine cycles required depends on the instructions and addressing mode. For more information on these cycles refer to the Motorola MMPU Microcomputer Design Data Manual.

MPU CONTROL SIGNALS

Clock Phase One and Phase Two (01, 02). The two-phase TTL-level clock signals are applied to these inputs.

HALT. When asserted, this input causes the MPU to halt all activity when the current instruction execution is complete. The HALT input is not used in the 7612D system.

Three-State Control (TSC). The TSC input causes the MPU address bus and Read/Write line to go to the high-impedance state. The input is tied low (unasserted) in the 7612D.

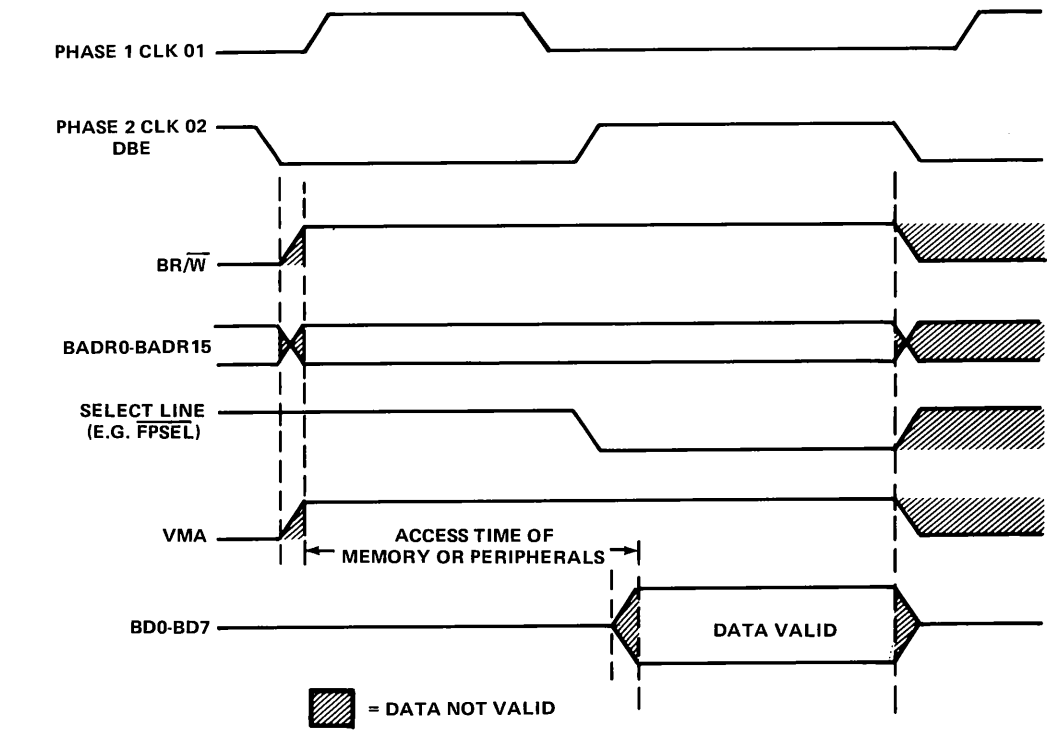
Read/Write (R/$\overline{W}$]). This output tells the peripheral and memory devices on the MPU bus whether the processor is reading from the data bus (R/$\overline{W}$ line high) or writing data onto the bus (R/$\overline{W}$ line low.) The standby state of the line is the read state.

Valid Memory Address (VMA). The VMA output is asserted (high) when the MPU has a valid address on the bus. When VMA is asserted, the memory and peripherals decode the address to determine if it is theirs. In the 7612D, VMA enables the Address Decoding Logic to generate the select signals.

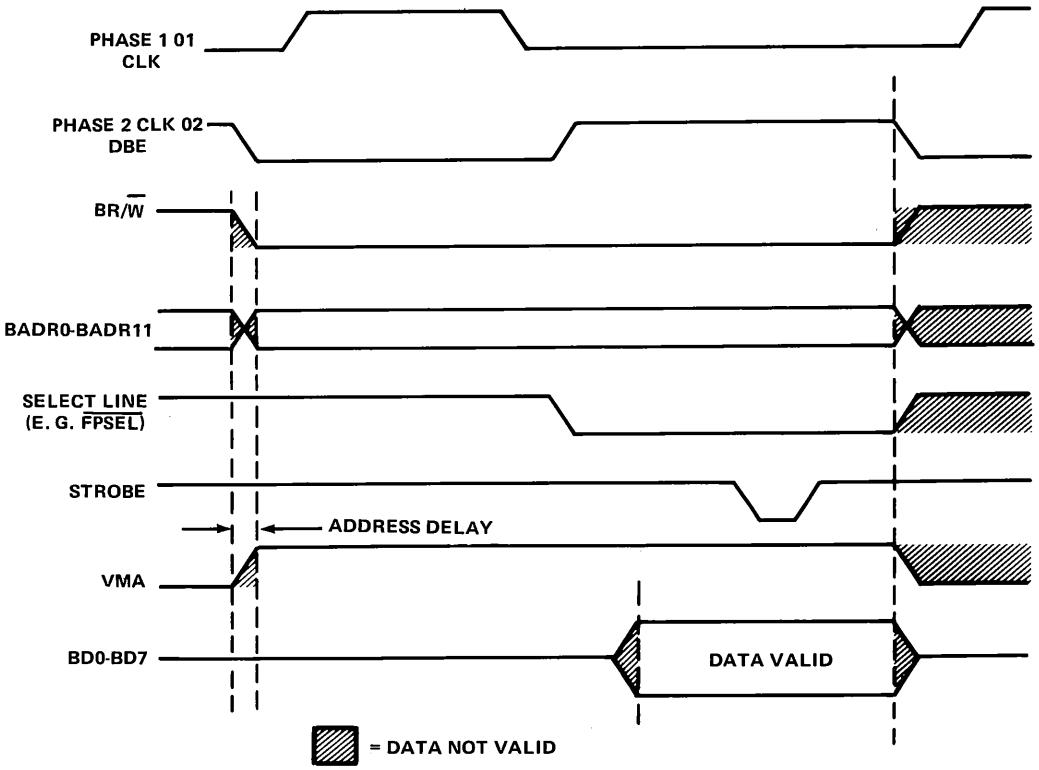
Data Bus Enable (DBE). This input is the three-state control signal for the MPU data bus. The MPU bus drivers are enabled when DBE is high. This input is normally tied to the phase-2 clock signal.

Figure 3-32 shows read- and write-cycle timing on the MPU bus and the relationship of these control signals to the cycles.

Interrupt Request ($\overline{IRQ}$). When asserted, this input requests an interrupt sequence in the MPU. The processor completes its current instruction before recognizing the interrupt. Then it tests the interrupt mask bit in the condition code register. If it is set, the interrupt is ignored, otherwise, the following sequence is executed:



(a) Read cycle timing on the 6800 bus.



(b) Write cycle timing on the 6800 bus.

2387-323

Figure 3-32. Read- and write-cycle timing on the MPU bus.

1. Push the contents of the program counter, index register, accumulators, and condition code register onto the stack, decrementing the stack pointer for each byte stored.

2. Set the interrupt mask bit and load the address stored at FFF8 and FFF9 (7FF8 and 7FF9 in the 7612D, because bit 15 of the address bus (A15) is unused).

3. Execute the interrupt service routine that begins at the address stored at FFF8 and FFF9 (7FF8 and 7FF9 in the 7612D).

4. At the end of the interrupt routine, return to the interrupted task by retrieving the previous register contents from the stack.

External devices are wired-ORed to the $\overline{IRQ}$ input. Because multiple devices are connected, the service routine must determine which device generated the interrupt and take appropriate action.

NonMaskable Interrupt ($\overline{NMI}$). A negative transition on this input causes the processor to execute an interrupt sequence as just discussed. The $\overline{NMI}$ input differs from the $\overline{IRQ}$ input in two ways: First, the interrupt mask bit has no effect on the $\overline{NMI}$ input and second, the pointer address (called a vector) to the NMI interrupt routine is stored at FFFC and FFFD (7FFC and 7FFD in the 7612D).

Table 3-12 shows the interrupt vectors for the Reset, $\overline{NMI}$, and $\overline{IRQ}$ interrupts. An additional interrupt vector, the software interrupt vector, is also shown. This vector is used when an interrupt is generated by the program running on the MPU.

TABLE 3-12
MPU Interrupt Vectors

Vector		Interrupt
High Byte	Low Byte	Type
7FFE	7FFF	Reset
7FFC	7FFD	NonMaskable Interrupt
7FFA	7FFB	Software Interrupt
7FF8	7FF9	Interrupt Request

Figure 3-33 shows the MPU's main decision paths when it is executing a program.

NOTE

All addresses are in hexadecimal unless otherwise noted.

THE MPU BUS

The MPU communicates with the program memory (ROM) RAM, and the instrument functions it controls through a 15-bit address bus, an eight-bit data bus, and a set of device select lines. The MPU bus, bus drivers, and decoders are shown on diagram 17.

The 15-bit address bus allows the MPU to address 32k (8000 hex) unique locations including ROM, RAM, and instrument control/status registers. Figure 3-34 shows a map of the MPU address space. Each of the functions controlled by the MPU is addressed by the low-order 11 bits of the address bus and one or more select signals derived from A10-A14. For example, to address a location in the range of 2000 to 2FFF in ROM, the MPU asserts the address of the location on address lines A0-A14. After a short address-settling time, the MPU asserts VMA. The reset signal, RST, is high, and during the phase-2 clock period, pins 4 and 5 of U132 (center of diagram 17) will be low, enabling the decoder. U132 decodes A12-A14 and asserts pin 13 ($\overline{MEMSEL2}$), enabling ROM bank to be addressed by A0-A11. The low-order bits (A0-A11) select the individual location within the ROM bank. The other ROM banks, RAM, and instrument control registers are addressed in a similar manner where U132 and U234A decode the five high-order bits of the address bus (A10-A14) to generate the select signals. Table 3-13 shows the functions selected by each of these signals.

TABLE 3-13
MPU Bus Select Signals

Signal Name	Lowest Address	Function Selected
$\overline{FPSEL}$	0D00	Front Panel
$\overline{INTESEL}$	0F00	MPU Interrupt Control.
$\overline{IOMSEL}$	0400	Unused ROM
$\overline{PISEL}$	0E00	Plug-in Readout and 7k Bus.
$\overline{ORSEL}$	0C00	Unused ROM
$\overline{TLTRSEL}$	0D80	Translator
$\overline{TRGSEL}$	0DC0	Trigger.
$\overline{PISEL}$	0E00	RO 7k Bus Interface.
$\overline{MEMSEL0}$	0000	RAM.
$\overline{MEMSEL1}$	1000	Unused ROM.
$\overline{MEMSEL2}$	2000	ROM (1/2 unused).
$\overline{MEMSEL3}$	3000	ROM.
$\overline{MEMSEL4}$	4000	ROM.
$\overline{MEMSEL5}$	5000	ROM.
$\overline{MEMSEL6}$	6000	ROM.
$\overline{MEMSEL7}$	7000	ROM.

BUS BUFFERS

Buffers U322, U332, and U334 (top-right of diagram 17) compose the address bus buffer for the MPU system bus. The enable inputs (pins 1 and 15 of each buffer) are tied to ground, so the buffers are always enabled. This buffer also drives the BR/$\overline{W}$ and $\overline{Strobe}$ lines. The $\overline{Strobe}$ pulse occurs at the center of each phase-2 clock period. This pulse tells devices that the address on the bus is valid and initiates

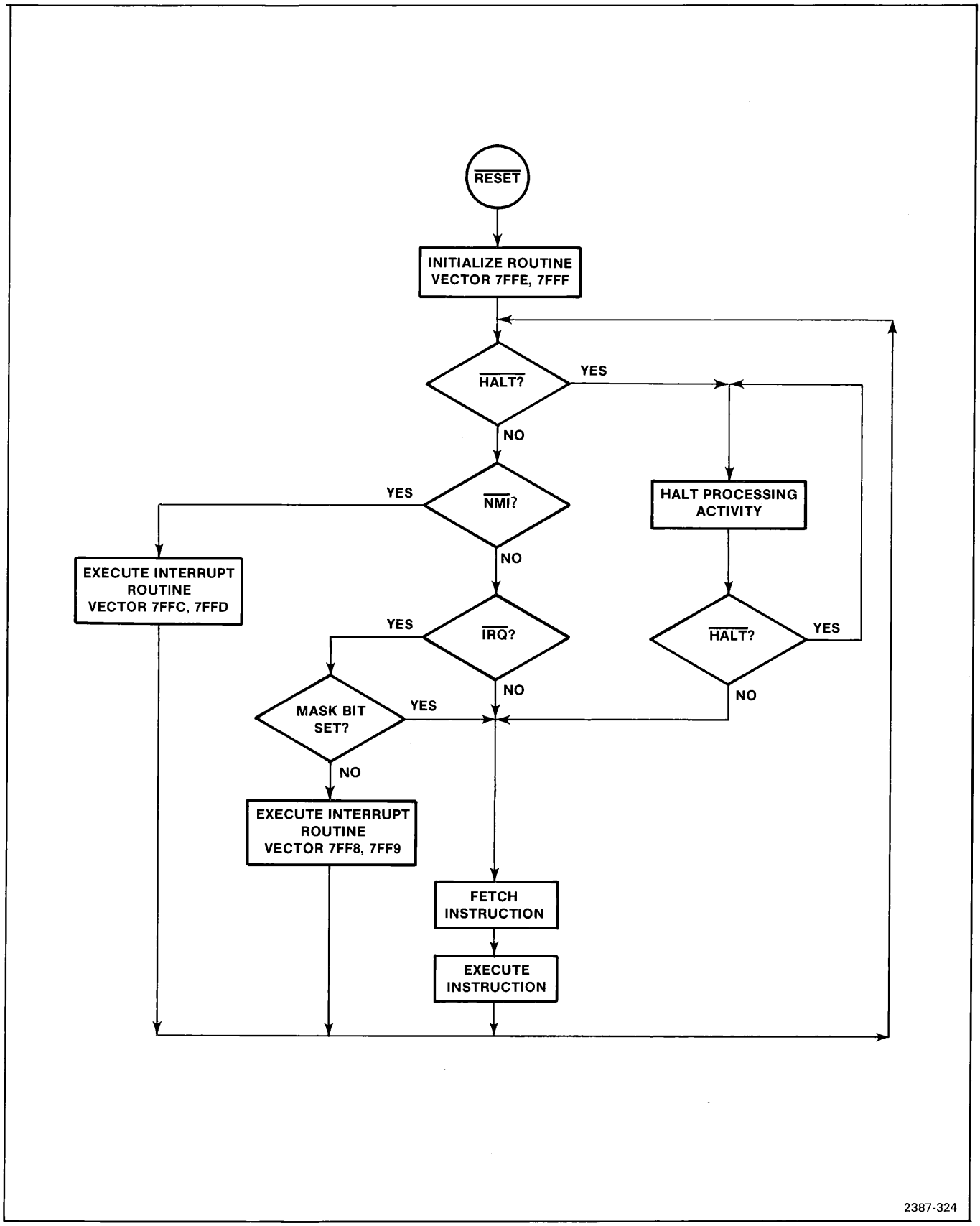


Figure 3-33. Flow chart of the MPU's main decision paths.

data transfer to or from the selected device. The BR/$\overline{W}$ line is driven by the MPU R/$\overline{W}$ output. When Write is asserted, the MPU is writing data to the bus. When the MPU is reading data, BR/$\overline{W}$ is high. The R/$\overline{W}$ line also controls the MPU data bus buffers, U312 and U314 (top-left of diagram 17). When R/$\overline{W}$ is low, the output of U402B is high and the output of U206C is low, enabling the buffer output drivers. If the MPU is reading data from the bus, R/$\overline{W}$ is high and the buffer receivers are enabled.

MPU CLOCK CIRCUIT

The MPU system clock is provided by a 10 MHz master clock on the Translator board (A16 on diagram 5). The clock signal is fed to the MPU clock circuit in the bottom-left of diagram 17. The 10 MHz clock drives the clock input of a four-bit binary counter (U032). This clock signal is also inverted by U102D and the inverted signal drives three flip-flops (U102A, U001A and U001B). The outputs of counter U032 go to a 4-to-16 line decoder (U022). This decoder asserts one of its 16 outputs (five outputs are used in this circuit) for each of the counter's states. The outputs of the decoder drive the inputs of the three flip-flops.

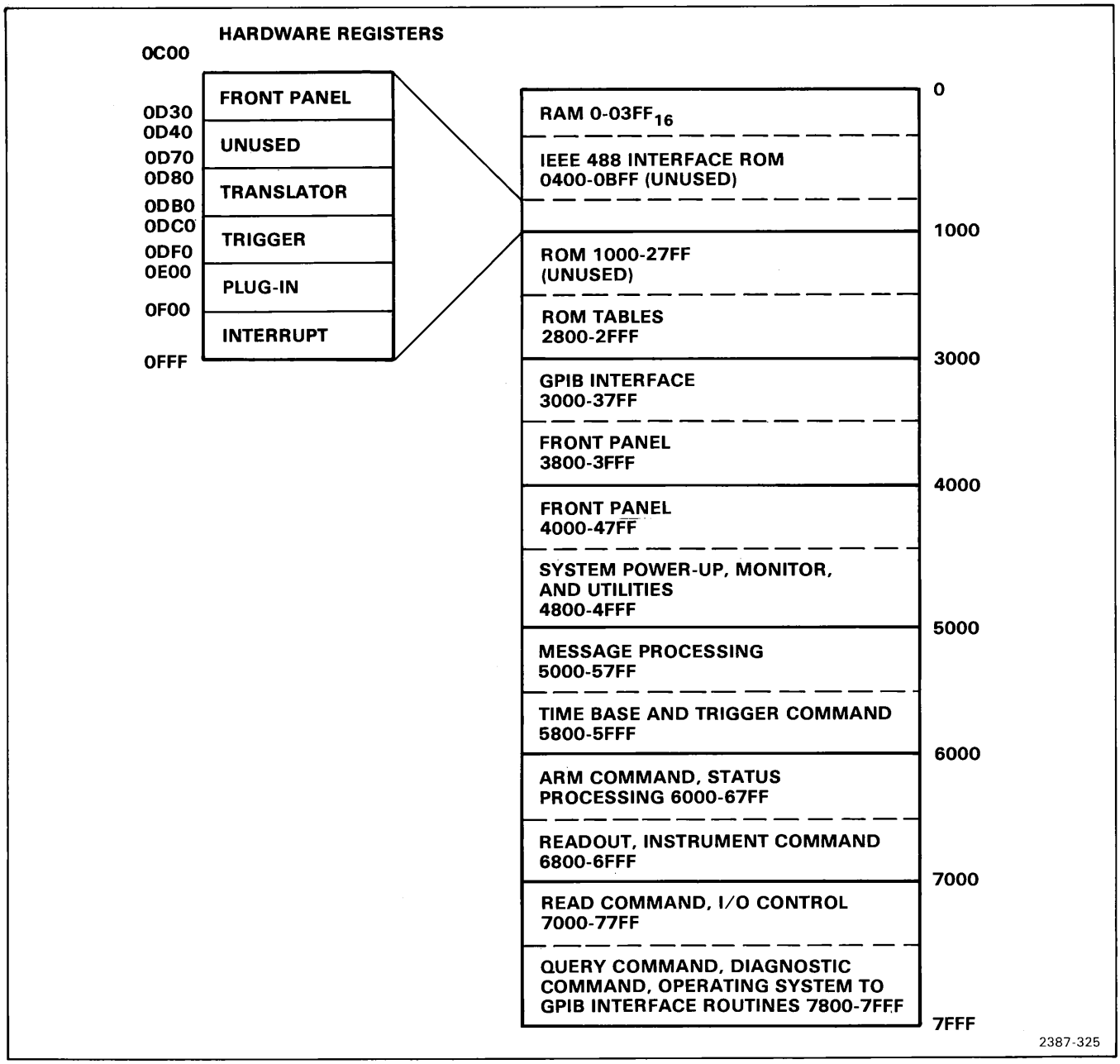


Figure 3-34. Address map of the MPU system.

Refer to Figure 3-35 as we discuss the operation of the Clock circuit. Assume that counter U032 is cleared (set to zero).

Decoder U022 decodes the counter's outputs and asserts pin 1. The output of U012A goes high and on the falling edge of the inverted clock, the $\overline{Q}$ output of U001A goes low. This output stays low until the fifth 10 MHz clock pulse. At that time, the counter's outputs are set to a binary five (0101) and the decoder asserts pin 6. As a result, the K input of U001A goes high and on the next clock, the $\overline{Q}$ output goes high. On the sixth clock pulse, the output of U001B goes low and stays low until the 13th pulse. On the rising edge of the 13th pulse, pin 15 of U022 goes low, clearing the counter and starting the process over again. The result is a two-phase nonoverlapping clock with a period of about 1.4 μs.

The outputs of U001A and U001B are fed to the inverter/driver circuits formed by Q212, Q218, Q114D, and U114E. Transistors Q212 and Q218 are active pull-ups for open collector inverters U114E and U114D. On the falling edge of the noninverted clock, the transistor turns on, pulling the output of the inverter high very quickly. The transistor stays on just long enough to pull the inverter output up. On the rising edge of the noninverted clock, the transistors are unaffected. This circuit improves the rise time of clock pulses to meet the MPU clock pulse specifications.

The clock circuit also generates the $\overline{STB}$ (Strobe) pulse previously discussed. When the four-bit counter, U032, counts to ten, pin 11 of U022 is asserted. On the rising edge of the next clock, the Q output of U102A goes low, asserting $\overline{STB}$.

On count 11, pin 1 of U022 goes high and the $\overline{STB}$ line goes high on the 12th clock. The result is a 100 ns pulse near the middle of each phase-2 clock period. See Figure 3-35.

RESET CIRCUIT

When power is applied to the 7612D, the reset circuit shown at the left-center of diagram 17 will assert the MPU's $\overline{RESET}$ input, forcing it to execute the initialize and self-test routines that begin at the address stored in 7FEE and 7FFF.

When the 5.1 V power supply comes up, U102B will be cleared by the RC network of R106, C106, and CR106. The Q output of U102B will then be low, so the output of U402A will go high and $\overline{RST}$ (Reset) will be asserted. The low on $\overline{RST}$ will hold the MPU in an idle state until PON makes a positive transition to indicate that the power supplies are stable. During the delay while the power supplies stabilize, C106 will charge through R106 and the clear input of U102B will go high (unasserted). The positive transition on PON will clock the Q output of U102B high and trigger one-shot U204A. The low on U204A's $\overline{Q}$ output will hold RST low through U402A. About 14 ms later, U204A will time out, $\overline{RST}$ will go high, and the MPU will begin executing the initialization and self-test routines.

The $\overline{RST}$ pulse also resets logic circuits in other parts of the 7612D.

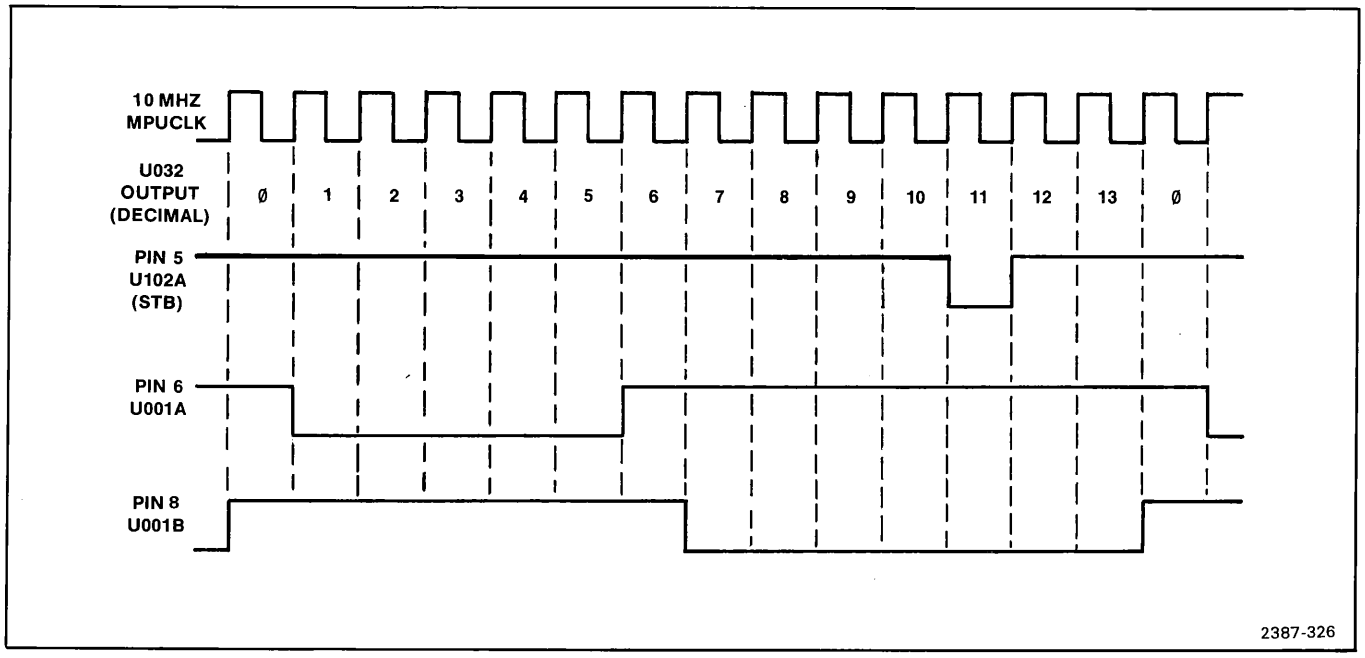


Figure 3-35. Timing of the MPU clock circuit.

POWER FAIL AND HARDWARE FAILURE INTERRUPTS

If any of the 7612D's analog power supplies fall out of tolerance, $\overline{HWF}$ (Hardware Failure) will go low. If the line input power is interrupted, PON will go low. In either case, the output of U206A will go high. If NMIEN (Nonmaskable Interrupt Enable) is high, the output of U206B will go low, generating a nonmaskable interrupt to the MPU. The NMIEN line is held low (interrupts disabled) during the power-up routine and set high after power-up and self-test are complete.

MPU INTERRUPT CONTROL

The Interrupt Control Logic consists of two Interrupt Occurred Registers, U524 and U712 (Table 3-14), and two Interrupt Mask Registers, U728 and U732 (Table 3-15). This control logic receives interrupt signals from instrument functions controlled by the MPU. These interrupt signals are OR'ed together through the Interrupt Mask Registers to drive the $\overline{IRQ}$ input of the MPU.

TABLE 3-14
Contents of Interrupt Occurred Registers

Bit	Register	
	U524	U712
7	R-REN	IOI
6	XMTI	FPI
5	A:AQI	Jumper
4	B:AQI	Jumper
3	not used	Jumper
2	not used	not used
1	not used	not used
0	not used	send
Register Address	0F00 (read only)	0F02 (read only)

0F00 Bit 0-3: Unused.

0F00 Bit 4-B:AQI: When set, indicates a time base B acquisition interrupt has occurred.

0F00 Bit 5-A:AQI: When set, indicates a time base A acquisition interrupt has occurred.

0F00 Bit 6-XMTI: When set, indicates memory data has been transmitted to the IEEE 488 Interface bus or X-Y output.

0F00 Bit 7-R-REN: When set, this bit indicates that REN has gone false.

0F02 Bit O-SND: When set, this bit indicates that a SND interrupt from the 7K interface has occurred.

0F02 Bit 1,2: Unused

0F02 Bit 3-5: Jumpered for normal operation.

0F02 Bit 6-FPI: When set, a front-panel interrupt has occurred.

0F02 Bit 7-I0I: Set when an I/O interrupt from the IEEE 488 interface has occurred.

When an interrupt occurs, a corresponding bit in one of the Interrupt Occurred Registers is set (to logic one). If the interrupt is not masked, the IRQ line will be asserted, interrupting the MPU. As part of its interrupt service routine, the MPU reads the Interrupt Occurred Registers to determine the source of the interrupt. If any set bits are found, the MPU will jump to a service routine for the highest priority interrupt. If no set bit is found, the MPU will return to its previous task, and an unrecognized interrupt will be reported.

All interrupts except $\overline{SND}$ and $\overline{R\text{-}REN}$ will remain asserted until the MPU clears them as part of the service routine. U702B latches the $\overline{SND}$ interrupt. The positive transition at the end of the $\overline{SND}$ will clock U702B and its output will go high. This sets bit 0 of the Interrupt Occurred Register. The MPU will clear U702B by writing to address 0F02, and U234B (bottom-center of diagram 18) will decode the address and assert IA2. When $\overline{IA2}$ and BR/$\overline{W}$ are low, the output of U514A (left center of the diagram) will go low. The MPU clears U702B by asserting $\overline{BD0}$. When $\overline{BD0}$ is low, the output of U606D will go low, clearing U702B and resetting the $\overline{SND}$ interrupt.

The MPU can mask (disable) $\overline{IRQ}$ interrupts in two ways. All $\overline{IRQ}$ interrupts can be internally masked by setting a bit in the MPU's condition code register. If this bit is set, the Interrupt Control Logic will pass interrupts as usual but the MPU will ignore its $\overline{IRQ}$ input. The 7612D firmware operating system sets this interrupt-mask bit while the MPU is executing the power-up routine. The mask is also set when routines that should not be interrupted are being executed. The IEEE 488 message processor is such a routine.

Interrupts may also be individually masked by setting the appropriate bit(s) in the Interrupt Mask Registers.

U728 masks the IOI, FPI and SND interrupts. U732 masks the $\overline{REN}$, XMTI, A:AQI, and B:AQI interrupts. This register's address is OF01.

For example, to mask the I/O interrupt from the IEEE 488 Interface (IOI), the MPU will write to OF03. U234B will decode the address and assert $\overline{IA3}$. When $\overline{IA3}$ and BR/$\overline{W}$ are low, the output of U514C will go low. The byte on $\overline{BD0}$-$\overline{BD7}$ is latched on the positive transition at the end of the BR/$\overline{W}$ cycle. To mask IOI, the MPU holds $\overline{BD7}$ low. This will set bit 7 of U728 and pin 6 will go low. As a result, the output of U614B goes high and IOI interrupts are disabled.

19 READOUT/7K INTERFACE

The 7K/IEEE 488 Interface provides the interface between the 7k bus and the MPU. The MPU echoes 7k bus transactions onto the external IEEE 488 bus and vice versa (7k is an abbreviation for the Tektronix 7000-Series of oscilloscope mainframes and plug-in units). The IEEE 488 bus is, in effect, extended through the 7612D to the plug-ins. Figure 3-36 shows a simplified diagram of the complete 7K/IEEE 488 Interface system.

The 7k Bus. The 7k bus that connects programmable plug-in units and mainframes is very similar to the bus specified in the IEEE Standard 488-1975. The 7k bus has three groups of lines: an eight-line data bus, a four-line transfer bus (this part of the bus is modified from the IEEE standard) and a five-line management bus.

The data bus (DI01-8) is an eight-bit bidirectional bus. All data, device-dependent messages, and addresses are transferred over this bus. The commands, data, and addresses are sent, one eight-bit byte at a time, in a byte-serial bit-parallel fashion.

The transfer bus carries the handshake sequences that are executed to transfer every byte on the bus. The handshake ensures that the data is transferred between the 7612D and plug-ins in an orderly fashion. The 7k transfer bus contains the three handshake lines specified in the IEEE standard with one additional line. The lines are briefly described below:

7KNRFD (Not Ready For Data)—When addressed to listen or when an ATN message is received, the plug-in(s) assert this line until they are ready to receive a data byte. The 7612D echoes $\overline{7KNRFD}$ onto the external $\overline{NRFD}$ line on the IEEE 488 bus. When the plug-in is ready to listen, it releases $\overline{7KNRFD}$ and the 7612D releases $\overline{NRFD}$, allowing the talker to place a byte on 7KDI01-8.

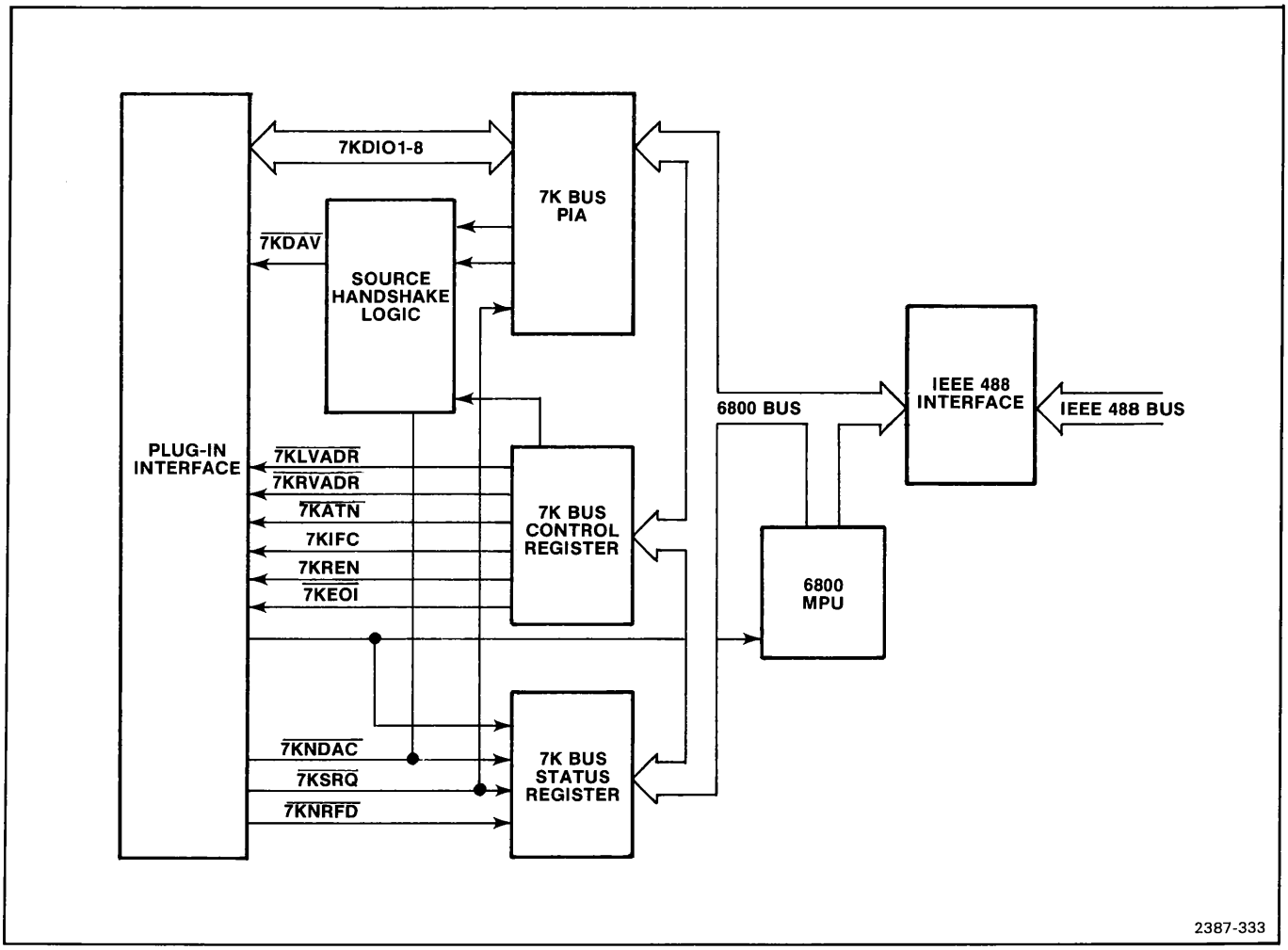


Figure 3-36. Block diagram of the 7k/IEEE 488 interface system.

7KDAV (Data Valid)—The $\overline{7KDAV}$ line is asserted by the 7612D when it has placed a valid byte on the 7k bus for a listen-addressed plug-in; the positive transition at the end of the $\overline{7KDAV}$ pulse tells the plug-in that the byte is received.

7KNDAC (Not Data Accepted)—When addressed to listen or when an ATN message is received, the plug-in(s) assert this line until they have captured the byte on the bus. The 7612D echoes this line onto the external $\overline{NDAC}$ line. When the plug-ins have received the byte, $\overline{7KNDAC}$ is released. Then the talker can remove the byte from the bus and release $\overline{DAV}$. This completes the handshake process.

7KSND (Send)—This signal is unique to the 7k bus. The plug-in uses the standard three-wire handshake just described for the acceptor handshake. However, for the source handshake the plug-in and the mainframe use a two-wire, noninterlocked protocol. The plug-in asserts $\overline{7KSND}$ when it places a byte on the bus. The 7612D accepts the byte and sends it out through its IEEE-488 interface using the standard source handshake. While the 7612D is sending the byte, the plug-in monitors the state of $\overline{7KDAV}$. When $\overline{7KDAV}$ makes a low-to-high transition at the end of the handshake, the plug-in assumes that the byte was successfully transferred unless 7KATN was asserted during the delay.

The management bus is a group of five lines that control the interface and data transfer. These lines communicate interface messages to detect an interrupt from one of the plug-ins, enable remote operation, and denote the end of a message on the data bus. Most of these lines are direct counterparts of the lines on the IEEE 488 bus. The functions of these lines are briefly described below:

$\overline{7KATN}$ (Attention)—Asserted by the 7612D when the IEEE 488 bus $\overline{ATN}$ line is asserted. When low, information on the data bus is interpreted as an interface message. When $\overline{7KATN}$ is high (not asserted), the byte is interpreted as a device-dependent message or data.

$\overline{7KIFC}$ (Interface Clear)—Asserted by the 7612D in response to a low on the external IFC line. When asserted, the IEEE 488 interfaces in the plug-ins are initialized to their idle state.

$\overline{7KSRQ}$ (Service Request)—Asserted by the plug-ins to request service from the controller-in-charge on the external IEEE 488 bus. The 7612D asserts the external $\overline{SRQ}$ line to signal the controller-in-charge. The controller usually interrupts its current task and conducts a serial poll to determine the source of the interrupt. The plug-in unit reports its status through the 7612D when polled.

$\overline{7KEOI}$ (End Or Identify)—Asserted by the plug-in when it is talking or by the 7612D when the plug-in is listening. A low on $\overline{EOI}$ indicates that the byte currently on the bus is the last byte.

$\overline{7KREN}$ (Remote Enable)—The $\overline{7KREN}$ line is not a direct copy of the external $\overline{REN}$ line. The 7612D asserts $\overline{7KREN}$ when it receives the first attention message with $\overline{REN}$ asserted (e.g., the 7612D listen address). $\overline{7KREN}$ remains asserted until one of three conditions occur: The 7612D receives the GTL (Go To Local) command, the front-panel LOCAL button is pressed (when the instrument is not set to remote with lockout state), or the external REN line is unasserted. When $\overline{7KREN}$ is unasserted, the plug-in is forced to go to local state.

The 7k bus enters the 7612D through the Plug-in Interface board, A46 (diagram 14). Programmable plug-ins use time-slot lines TS2-TS9 for the 7KDI01-8 lines. The 7k data bus is isolated by the set of diodes shown at the center of diagram 14. These diodes keep the time-slot pulses off the 7k bus when a nonprogrammable plug-in is installed. The 7k management and transfer buses do not share their lines with other functions.

The MPU controls and communicates with the 7k bus through three devices—the 7k Bus PIA (U424, diagram 19), the 7k Bus Control Register (U538), and the 7k Bus Status Register (U524). Table 3-15 summarizes the registers and their MPU addresses.

TABLE 3-15
7k Interface Registers

Addresses	Register
0E7X	7k Interface PIA
0E7C	Input Port (Data Reg. A)
0E7D	Input Control (Control Reg. A)
0E7E	Output Port (Data Reg. B)
0E7F	Output Control (Control Reg. B)
0EF4	7k Bus Status Register
0EF8	7k Bus Control Register

Peripheral Interface Adapters (PIA). The MPU communicates with the 7K/IEEE 488 interface and the main IEEE 488 interface through two Peripheral Interface Adapters (PIAs). A brief discussion of the PIA's internal architecture will be helpful in understanding the IEEE 488 interfaces.

Two separate I/O ports, two data direction registers, and two control registers comprise each PIA (see Fig. 3-37). Each line in the I/O ports can be programmed to be an input or output by setting bits in the data direction registers. Two interrupt outputs, $\overline{IRQA}$ and $\overline{IRQB}$, signal the MPU that the PIA has data to be read or needs service.

Two interrupt inputs (CA1 and CB1) are individually programmable as positive- or negative-edge sensitive. Two more lines (CA2 and CB2) can be programmed as edge-sensitive interrupt inputs or peripheral control outputs. The function of these inputs and outputs is programmed through the control registers. The internal interrupt flags are also read from the control registers.

The chip select lines (CSO-$\overline{CS2}$) are used to address the PIA, while the register select lines (RSO-RS1) select the individual registers within the PIA.

7k Bus PIA. The 7k Bus PIA, U424 at the top center of diagram 19, handles all communication on the 7k data bus (7KDI01-8). It also controls the $\overline{7KDAV}$ line. The data bus is bidirectional, so one of the PIA ports is used for reading data from the 7k bus and the other is used for writing data.

When one of the plug-ins is talking, it will place a byte on the bus and will pulse $\overline{7KSND}$. The positive transition at the end of the pulse will latch the data from the bus into U412. The positive transition on $\overline{SND}$ also will generate an interrupt to the MPU via FF U702B and U614C on diagram 18. The $\overline{IRQ}$ will signal the MPU that the PIA has data to be sent on the IEEE 488 bus. The MPU will read the data from the A port of the PIA. If the other plug-in is not addressed to listen (the usual case), the peripheral control output (CA2) is programmed to go low when the MPU reads the data. The low on CA2 will cause the output of U636A to go high which will activate U638B. When active, U638B will cause $\overline{7KDAV}$ to go low. On the next rising edge of the CK2 clock (pin 25 of the PIA), the CA2 output returns to its high state. The positive transition that results on $\overline{7KDAV}$ tells the plug-in unit that the 7612D has accepted the byte.

If one plug-in unit is addressed to talk and the other to listen, the CA2 output of the PIA (pin 19) is set to go low when the MPU writes the data to the output port. When the CB2 output goes low as the result of writing data to the PIA output port, FF U522A will be cleared and the low on its Q output will enable bus driver U512. The next positive transition on the CK2 line will cause the PIA's CB2 output to return to its high state. The high on CB2 and the high on the $\overline{Q}$ output of U522A will activate U532A whose high output will activate U638B. Gate U638B will assert a low on $\overline{7KDAV}$, which will signal the listening plug-in unit that the data on the 7k bus is valid. When the plug-in unit accepts the data, it will release $\overline{7KNDAC}$. The positive transition on $\overline{7KNDAC}$ will clock U522A, and the high on its Q output will disable the bus drivers. The low on U522A's Q output will

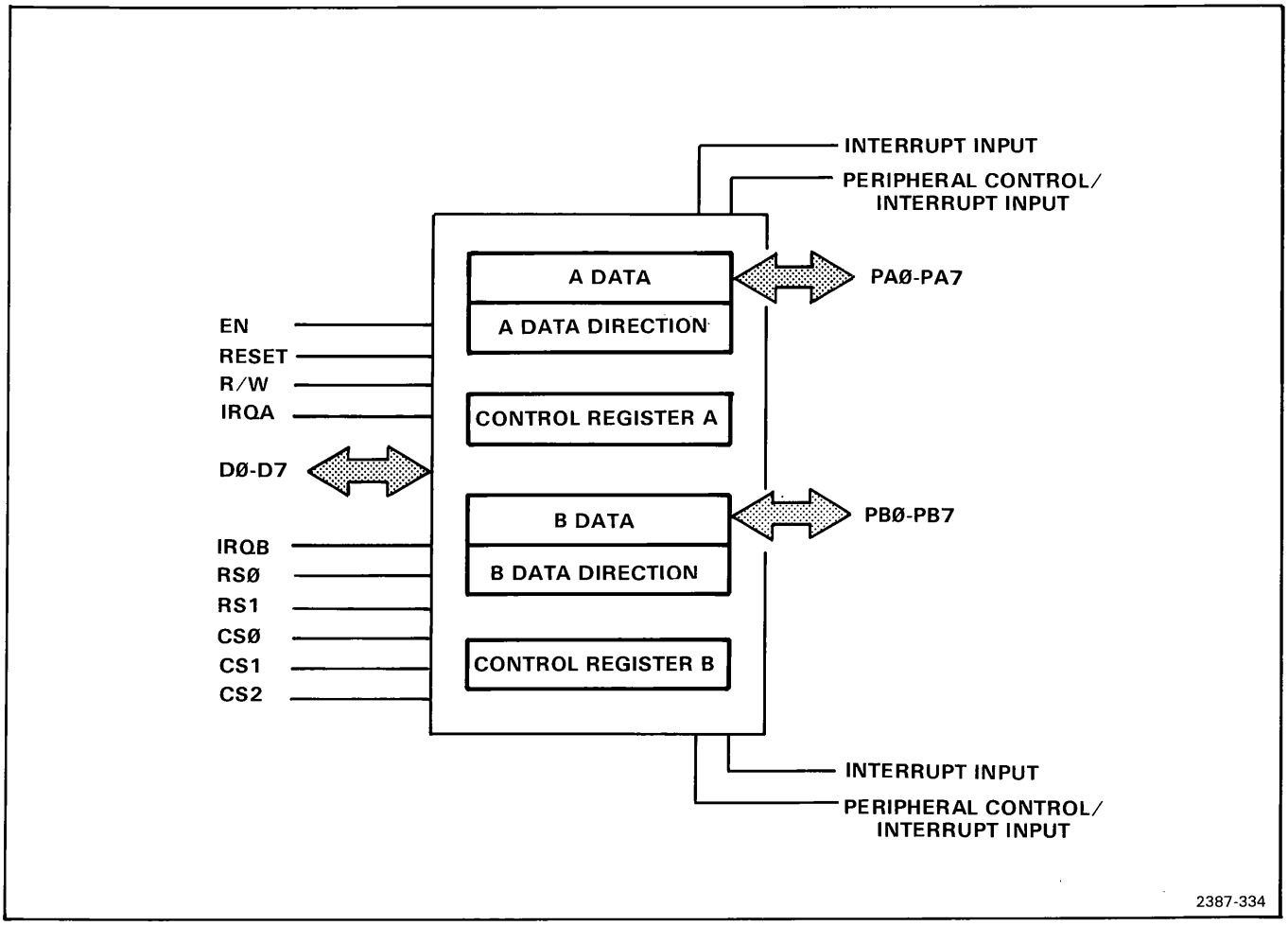


Figure 3-37. Block diagram of the PIA internal architecture.

disable U532A, which will cause a high on $\overline{7KDAV}$. The positive transition on $\overline{7KDAV}$ will signal the talking plug-in that the transfer is complete. The positive transition on the Q output of U522A also will generate an interrupt through the CA1 input of the PIA. This interrupt will tell the MPU that the source handshake was completed. If, for some reason, the listening plug-in doesn't release $\overline{7KNDAC}$, the source handshake can be terminated by clearing bit 1 of the 7k bus control register (pin 19 of U538). Clearing this bit will assert the set input of U522A, resetting it to its idle state.

If either of the plug-ins assert $\overline{7KSRQ}$, the PIA will generate an interrupt to the MPU (on diagram 17) through IRQB. The MPU will echo this SRQ to the external IEEE 488 bus. The plug-in will report its status when polled by the controller-in-charge.

7k Bus Control Register. The MPU controls the 7k management bus and other 7k bus functions through the 7k Bus Control Register. The register, U538 in the bottom-center of diagram 19, is located at 0EF8 in the MPU address space. When the MPU places the register's address on its bus, PISEL (pin 13 of U822D, lower left of diagram 19) is asserted. The $\overline{STROBE}$ pulse occurs near the middle of each phase-2 clock period. As a result, the output of U822D ($\overline{PISTROBE}$) will follow the $\overline{STROBE}$ line when PISEL is asserted. Data from the MPU bus will be latched into the 7k Bus Control Register on the rising edge of $\overline{PISTROBE}$.

Table 3-16 lists the name and function of the bits in the register.

TABLE 3-16
7k Bus Control Register Bits

Bit	Name	Function
0	—	Unused
1	HSRST	Resets source handshake
2	7KRVADR	Addresses right plug-in unit
3	7KLVADR	Addresses left plug-in unit
4	7KREN	7K Remote Enable (inverted)
5	7KATN	7K Attention (inverted)
6	7KIFC	7K Interface Clear (inverted)
7	7KEOI	7K End or Identify (inverted-output with source handshake only)

Bits 4-7 of the 7k Bus Control Register drive the 7k management bus lines through inverters U536A through D. The function of these lines was previously discussed. Bits 1, 2, and 3 of the register drive the $\overline{HSRST}$, $\overline{7KVADR}$ and $\overline{7KLVADR}$ lines, respectively.

The $\overline{HSRST}$ (HandShake ReSeT) line resets the source handshake logic if a listener fails to release 7KNDAC.

The 7612D decodes the primary and secondary addresses it receives on the IEEE 488 bus and generates the $\overline{7KLVADR}$ (7k Left Valid Address) and $\overline{7KRVADR}$ (7k Right Valid Address) signals to address the plug-ins. When the secondary address for the right plug-in is received, the MPU will set bit 2 of the control register, asserting $\overline{7KRVADR}$. $\overline{7KLVADR}$ (bit 3) will be asserted when the vertical plug-in is addressed. The 7612D also passes bits 2, 6, and 7 of the addresses to the plug-in units. The plug-in units decode bits 6 and 7 to determine if the address is a talk or listen address and bit 2 to detect the UNT (UNTalk) and UNL (UNListen) messages.

7k Bus Status Register. The MPU reads the status of several important 7k bus lines through the 7k Bus Status Register, U524, shown in the bottom-right of diagram 19. The MPU accesses the register by reading from address 0EF4. Table 3-17 shows the function of each bit in the register.

TABLE 3-17
7k Bus Status Register Bits

Bit	Name	Function
0-3	Not used	
4	7KSRQ	7K Service Request
5	7KNDAC	7K Not Data Accepted
6	7KNRFD	7K Not Ready For Data
7	7KEOI	7K End Or Identify

IEEE 488 CONTROL

INTRODUCTION

The IEEE 488 interface handles all communication over the IEEE bus for both the mainframe and plug-in units. The interface is controlled by the MPU. All data received from the bus is processed by the MPU; however, data can be sent from the MPU or from either waveform memory. The interface also sends data from the waveform memories to an XYZ monitor. Figure 3-38 illustrates the three basic data transfer paths in the interface.

In this section we will discuss the control and status registers through which the MPU controls the interface. Figure 3-37, in the 7k Interface description, shows a block diagram of the interface. Notice that the PIA (Peripheral Interface Adapter) forms the major control and I/O port for the MPU.

NOTE

This description of the IEEE 488 interface refers frequently to two different buses: the MPU bus and the IEEE 488 bus. The discussion refers to the buses by name in most cases, but be careful not to confuse them.

IEEE 488 PIA. The heart of the IEEE 488 interface control system is the PIA, U412, shown in the upper-left of diagram 20. Half of the PIA is used as a bidirectional data port. The other half is dedicated to an interface control port.

The internal architecture of the PIA was described in the 7K Interface section. A review of that description may be helpful.

The MPU addresses the PIA by placing an address in the range 0C0C-0C0F on its bus. The $\overline{\text{IORSEL}}$ line (I/O SELect) is asserted for all addresses in the 0C00-0CFF range, enabling decoder U522 (bottom right of diagram 20). U522 decodes the address and asserts PIA to select the PIA. The two least-significant bits, BADR0 and BADR1, connect directly to the PIA's register-select inputs to select one of the six internal registers (two of the registers are accessed by setting a bit in the control registers).

The PIA serves an I/O register and a control port. The A port of the PIA is an eight-bit bidirectional port through which the MPU writes and reads data to or from the IEEE 488 bus. The B port is used as a control port. The lines in this port control the handshake logic or drive one of the IEEE 488 management bus lines. The control signals are listed and briefly defined below:

$\overline{\text{IFCL}}$ (Interface Clear)—This line is connected to one of the PIA's interrupt inputs and is asserted when the external IEEE 488 bus $\overline{\text{IFC}}$ line is asserted. A negative transition on $\overline{\text{IFCL}}$ causes the PIA's $\overline{\text{IRQB}}$ line to be asserted, generating an IOI interrupt to the MPU. The MPU responds by initializing the IEEE 488 interface to its idle state, clearing $\overline{\text{TALK}}$ and $\overline{\text{LISTEN}}$. The instrument operating modes are unaffected.

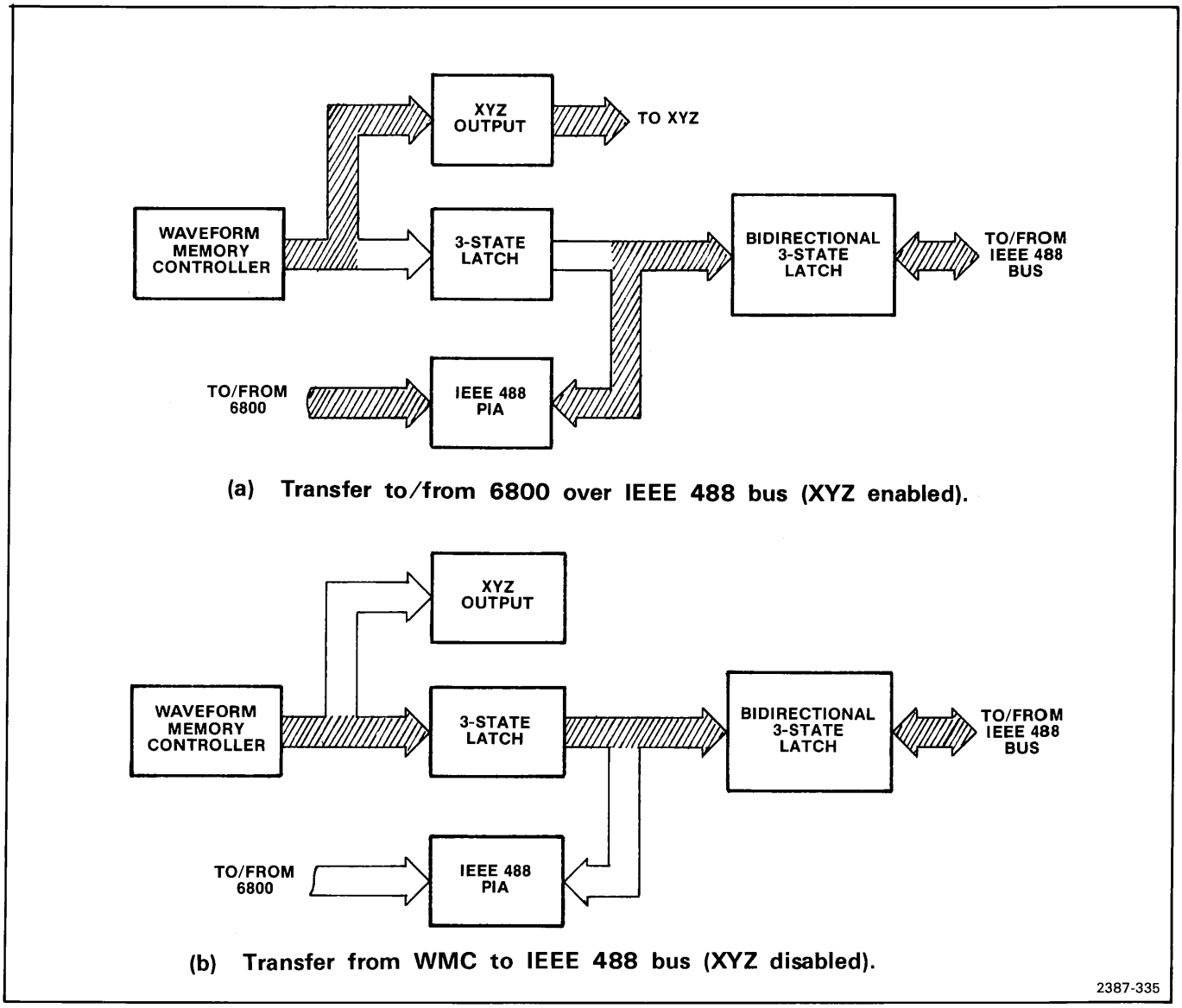


Figure 3-38. IEEE 488 Interface configuration.

R-ATN (Received ATN)—This line is asserted when the IEEE 488 bus $\overline{ATN}$ line is asserted. A positive transition on R-ATN generates an IOI interrupt to the MPU. The interface must stop talking and listen to all bytes sent with $\overline{ATN}$ true (low).

EOI-MPU (End or Identify)—When the last byte of a message is being sent over the bus, the MPU asserts this line. The IEEE 488 $\overline{EOI}$ line is asserted when EOI-MPU goes high.

$\overline{SRQ\text{-}MPU}$ (Service Request)—This line is asserted by the MPU to notify the IEEE 488 controller-in-charge that the 7612D or one of its plug-ins needs service. When $\overline{SRQ\text{-}MPU}$ is asserted, the external $\overline{SRQ}$ line is asserted.

BUSY—The MPU asserts BUSY when the MPU is busy and will not accept bytes from the IEEE 488 bus. If the 7612D or a plug-in is addressed as a listener and $\overline{ATN}$ is false (high), the $\overline{NRFD}$ bus line is asserted. BUSY goes low when the MPU is prepared to accept more input.

NBAP (New Byte Available from the Processor)—This line is asserted by the MPU when it has a byte to send on the IEEE 488 bus. NBAP initiates the source handshake and remains asserted until the handshake is successfully completed or interrupted by $\overline{ATN}$ and $\overline{DAV}$.

$\overline{XMT\text{-}MPU}$ (Transmit)—The MPU asserts this line to enable transfers from the waveform memory controller to the IEEE 488 bus. $\overline{TALK}$ must also be true to enable the source handshake required to transfer the bytes over the bus. $\overline{XMT\text{-}MPU}$ remains asserted throughout the transfer and goes high (unasserted) when the transfer is complete or an $\overline{ATN}$ message interrupts the transfer. If the transfer is interrupted, $\overline{XMT\text{-}MPU}$ goes low again as soon as $\overline{ATN}$ goes high.

B SELECT—When this line is asserted, data from U332 (right center of diagram 22) is shifted one-half scale to display the bottom (B) channel.

$\overline{LISTEN\text{-}MPU}$—This line is asserted to enable the acceptor handshake while ATN is false. $\overline{LISTEN\text{-}MPU}$ is always asserted when the 7612D is addressed as a listener. The line goes high when the instrument is addressed to talk or when it receives the UNL or IFC messages.

$\overline{TALK\text{-}MPU}$—This line is asserted to enable the source handshake. $\overline{TALK\text{-}MPU}$ goes high if $\overline{ATN}$ or $\overline{IFC}$ are as serted. If an attention message other than UNT (UNTalk), DCL (Device CLear), or MLA (My Listen Address) causes TALK to go high, it is asserted again when $\overline{ATN}$ goes high.

R-REN (Receive Remote Enable)—When the IEEE 488 REN line goes false (high), R-REN goes low, generating an IOI interrupt to the MPU. If REN is high, the 7612D will not execute any commands that affect the front-panel settings or data memory.

$\overline{DATVAL}$ (Data Valid)—This line is asserted by the acceptor handshake logic when valid data is available from the IEEE 488 bus. The high-to-low transition on DATVAL generates an IOI interrupt.

IEEE 488 BUS STATUS REGISTER

U500 and U302 (top-right of diagram 20) comprise the IEEE 488 Bus Status Register. This is a read-only register used by the MPU to determine the cause of an IOI interrupt or to read the status of the interface lines. Table 3-18 defines each bit in the register. The MPU accesses this register by reading from address 0CI0.

TABLE 3-18
IEEE 488 Bus Status Register Bit Definitions

Bit	Name	Function
0	$\overline{IFCL}$	Cleared when $\overline{IFCL}$ is asserted.
1	R-REN	Set when $\overline{REN}$ is asserted.
2	R-EOI	Set when the IEEE 488 $\overline{EOI}$ line is asserted.
3	R-ATN	Set when $\overline{ATN}$ is asserted.
4	SENT	Set when a source handshake is successfully completed.
5-6	—	Unused.
7	$\overline{DATVAL}$	Cleared when $\overline{DATVAL}$ is asserted.

Talk/Listen Address Register. The Talk/Listen Address Register contains the five low-order bits of the IEEE 488 primary bus addresses. The addresses are set by S400 on the IEEE 488 interface board. Buffers U410 and U610D (right of diagram 20) place the address set by S400 on the MPU bus when the MPU reads from address 0C20. Decoder U522, in the lower-right of the diagram, decodes the address and asserts TLA (Talk/Listen Address), enabling the three-state outputs of U410 and U610D.

The upper three bits of the eight-bit primary addresses are determined by the type of address—talk or listen. The addresses can be set within the full range specified by the standard: 32 to 63 for MLA (My Listen Address) and 64 to 95 for MTA (My Talk Address). Because the talk and listen addresses share the same five low-order bits, there is a correspondence between them. For example, if the switches are set for a MLA of 33, the MTA is set to 65.

Base Secondary Address Register. This register contains the base secondary address for the mainframe and plug-ins as set by S402. The mainframe MSA (My Secondary Address) is equivalent to the address set by S402. The left and right plug-in units' secondary addresses are set by the 7612D MSA in the following manner:

Compartment	Plug-in MSA
Left	7612D MSA+1
Right	7612D MSA+2

Buffers U610C, U410, and U500 place the base secondary address from S402 on the MPU Data bus when the MPU reads from address 0C30. The MSA is selectable within the full range of IEEE 488 standard: 96 to 127.

Address Decoding, Bus Drivers and ROM. Diagram 20 also shows the address decoding logic for the IEEE 488 interface and the MPU bus drivers.

All MPU registers for the IEEE 488 interface are in the range 0C00-0CFF. In this range the $\overline{\text{IORSEL}}$ (I/O Select) line is also asserted. When $\overline{\text{IORSEL}}$ is asserted (addresses 0C00-0CFF), U522 decodes the addresses and asserts one of its outputs to enable the addressed register. Table 3-19 shows the MPU address of each of the interface registers and functions.

TABLE 3-19
IEEE 488 Interface Register Addresses

Address	Register or Function
0C0X	IEEE 488 PIA
0C0C	Data Register or Data Direction Register A
0C0D	Control Register A
0C0E	Data Register or Data Direction Register B
0C0F	Control Register B
0C1X	IEEE 488 Bus Status Register
0C2X	Talk/Listen Address Register
0C3X	Base Secondary Address Register
0C4X	Assert DATACC (Data Accepted)
0C5X	Assert CLRSNT (CLeaR SeNT flip-flop)
0C6X	Clr DISPLAY latch and Init.
0C7X	Set DISPLAY latch (Enable XYZ)

Buffers U512 and U502 form a bidirectional data bus buffer for the MPU bus. The buffer will be enabled when the PIA or ROM is addressed. If the MPU WRITE line is asserted, the buffers's T_x inputs will be asserted, enabling input from the bus. Otherwise the R_x input is asserted, enabling the buffers for output to the MPU bus.

21 IEEE 488 HANDSHAKE

The IEEE 488 Handshake circuitry transfers data through the Interface Board (A56) under the control of the MPU. We will discuss the handshake sequences in two parts—the source handshake (7612D talking) and the acceptor handshake (7612D listening). Remember that the source and acceptor handshakes are opposite ends of a single handshake protocol.

Source Handshake. We will make frequent reference to Figures 3-39, 3-40 and diagrams 20 and 21 as we discuss the source handshake. Figure 3-39 shows a simplified schematic diagram of the source handshake logic when the MPU is sending data. The process is slightly different when waveform memory data is being transmitted. Figure 3-40 shows the timing of the handshake signals and relates these signals to the source and acceptor handshake states. The complete handshake logic circuitry is shown on diagram 21.

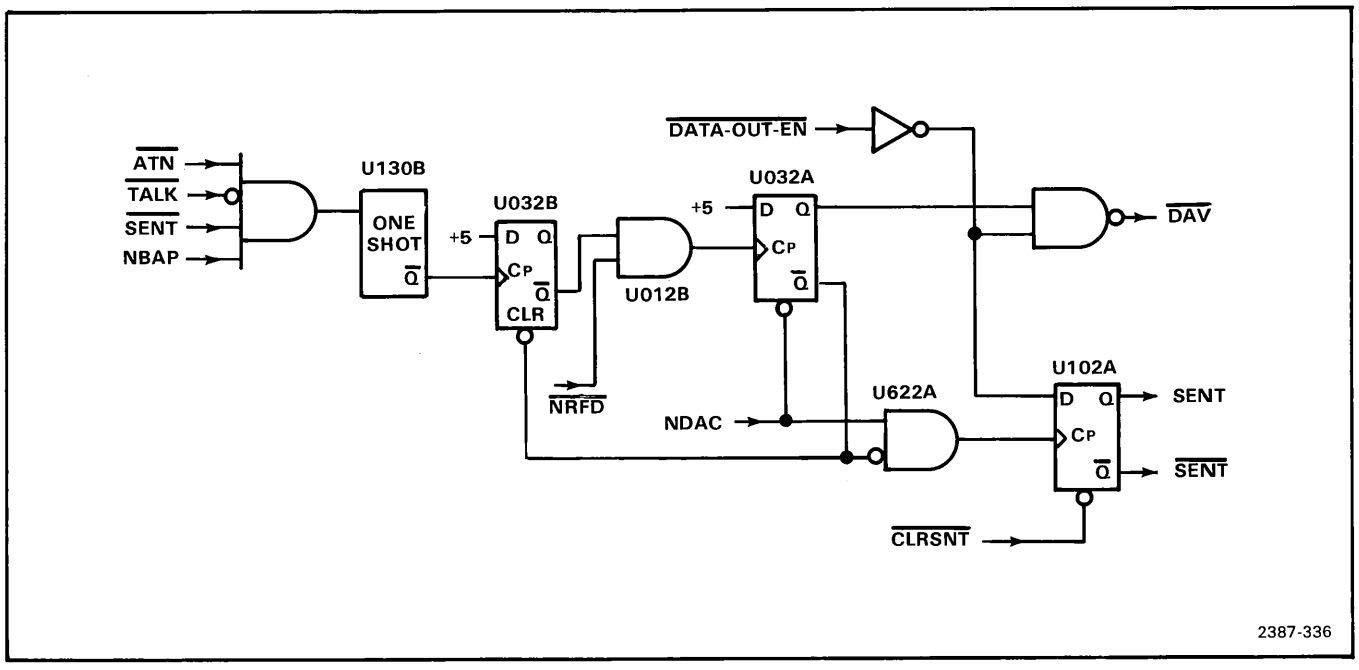


Figure 3-39. Simplified schematic of the source handshake logic.

When the 7612D is addressed to talk, the MPU will assert TALK-MPU by writing to the control output port (port B) of the PIA. The low on TALK-MPU will cause DATA-OUT-EN to be asserted, enabling IEEE 488 bus drivers U530 and U532 (upper right of diagram 21). At this point the interface is in the Source GeNerate State (SGNS-at number 1 in Fig. 3-40). Then the MPU writes the byte it wants to send to port A of the PIA and pulses CLRSNT by writing (or reading-either operation will assert the address on the bus) to address 0C50. The low on CLRSNT will clear the Sent FF U102A (see Fig. 3-39). Because the bus drivers are enabled, the byte from the MPU will be asserted on the IEEE 488 bus. Then the MPU will write to port B of the PIA, asserting NBAP (New Byte Available from the Processor). This signals the handshake logic that the byte has been placed on the bus and that it is time to move to the Source DelaY State (SDYS-number 2 in Fig. 3-40).

Referring to Figure 3-39, the output of the first AND gate will go high when NBAP is asserted. The positive transition from this gate will trigger one-shot U130B. The delay generated by U130B will give the data on the bus time to stabilize before DAV is asserted. When U130B shot times out, the positive transition on its Q output will clock U032B. The Q output of U032B will go low, and if NRFD is high the output of U032B will activate U012B. The output of U012B will go high, clocking U032A. The high on U032A's Q output is inverted by U610B to assert the IEEE 488 bus DAV line (number 4 in Fig. 3-39). The low on DAV tells listeners that a valid byte is on the bus. This is defined in the IEEE 488 standard as the Source TRansfer State (STRS).

The high on the Q output of U032A also goes to the Sent FF via U132A and U622A. The interface waits until all the listeners have accepted the byte and released NDAC. The NDAC line is a wired-OR line, so all listeners must release it before the bus line goes high. When it does, the output of U622A will go high, clocking Sent FF U102A and asserting SENT. The MPU waits for SENT (bit 4 of the bus status register) to go high, indicating that the byte was successfully transmitted. The high on NDAC will also clear U032A, releasing DAV (number 7 in Fig. 3-40). Then the listeners will assert NDAC, completing the handshake process. The interface is left in the SWNS (Source Wait for New cycle State-number 7).

If the MPU has another byte to transmit, it will pulse CLRSNT to clear the Sent FF. Then it will write the new byte to the bus, repeating the process. If the byte being transmitted is the last in a message, the MPU will also assert EOI-MPU, which will assert EOI while transmitting the byte. If the instrument is strapped to delimit messages with a carriage-return and line-feed, these two bytes will be added to the message and EOI will be asserted with the line-feed. TALK-MPU and DATA-OUT-EN will remain asserted until the 7612D receives an ATN message, UNT (UNTalk), or MLA (My Listen Address).

To transmit data the MPU asserts XMT-MPU and TALK MPU. Via U612D, Talk-MPU activates U602B, which asserts a low on Data Out En. Via U222D and U222A, the Data Out En and XMT-MPU signals enable U420, which transmits data from the HD bus to the receiving device

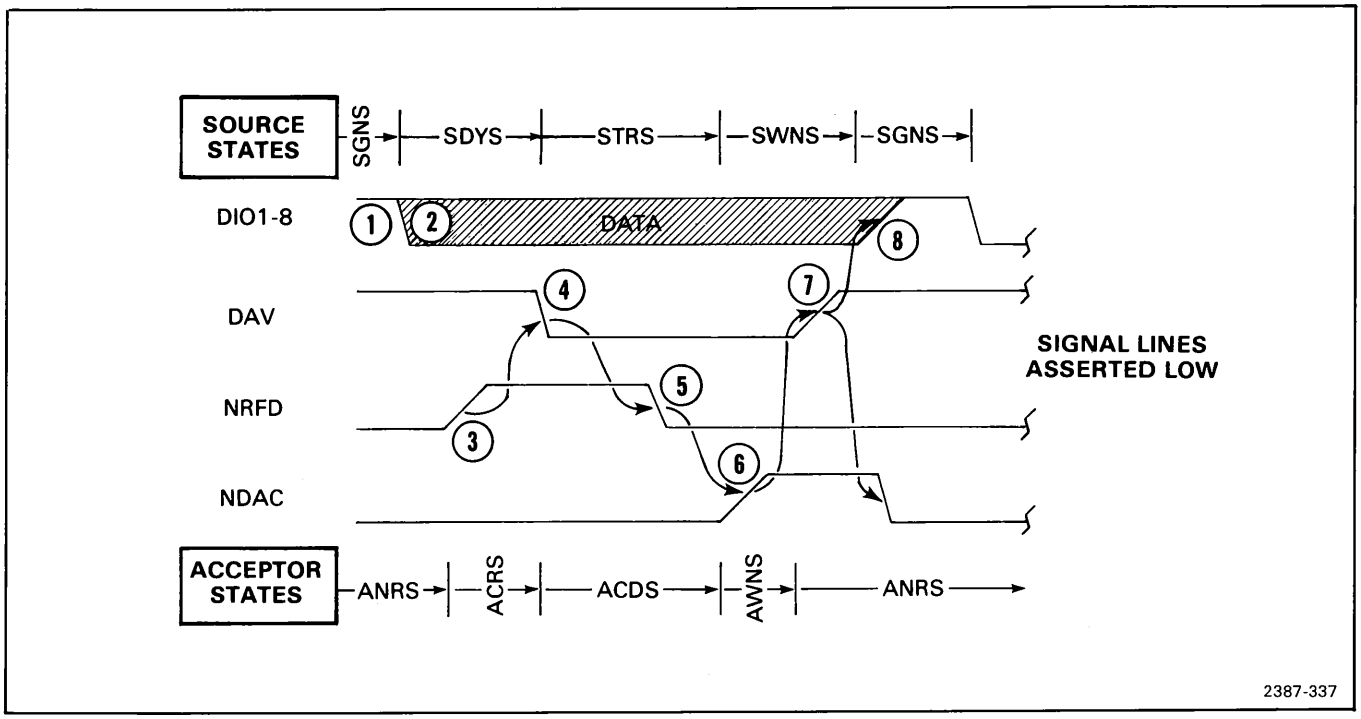


Figure 3-40. Handshake protocols on the IEEE 488 bus. (The numbers are used in the text.)

through output transceivers U510 and U520 and bus drivers U532 and U530. The MPU then starts the data transmitter (located on the Translator Board), which will cause a low on L Send. The low on L Send activates U132C, whose output clocks data into register U420 and sets U022A via U220C. The low output from U022A pin 6 causes U232C to send a high Y Sent to the data transmitter. The high output of U022A clocks one-shot U130B via U110D, U600A, U112A, U110A, and U012C. After the delay time of U130B, the $\overline{Q}$ output of U032B will go low and, via U012B when R-NRFD is low, will clock U032A. The Q output of U032A will go high, enabling U622A and asserting DAV. When the receiving device accepts the data, it will signal with a low on R-NDAC. The low on R-NDAC will activate U622A, whose high output will go through U602B, U320D and A to clear U022A. When U022A is cleared its high $\overline{Q}$ output will disable U232C, causing a low on Y Sent and ending one cycle of data transmission.

Acceptor Handshake. The acceptor handshake logic is shown in the right-center of diagram 21. We will refer to Figure 3-40 to relate the handshake sequence to the timing of the signals on the bus.

When the 7612D is addressed to listen, the MPU will assert LISTEN-MPU and DATA-IN-EN through port B of the PIA. At this point, the interface is in the Acceptor Not Ready State (ANRS-number 1 in Fig. 3-40). Because DAV is not asserted, R-DAV will be low and U330A will be cleared. The high on the $\overline{Q}$ output of U330A will assert T-NDAC (Transmit NDAC) which will assert the external NDAC line. If the MPU is not busy, BUSY will be low, and the output of U400B will be high. DAV will not yet be asserted, so DATVAL will be high. As a result, the output of U400A will be low and NRFD will not be asserted. This will move the interface into the ACceptor Ready State (ACRS-number 3 in Fig. 3-40).

When the talker asserts DAV, DATVAL will go low, interrupting the MPU. The byte will be stable on the IEEE 488 bus and, because the bus receivers are enabled, the PIA will have the byte on port A. Notice that port A of the PIA is now being used to input data, so the MPU must turn the lines around by writing zeros into data direction register A. Then the MPU will read the byte from port A. The low on DATVAL will cause the output of U400A to go high, asserting T-NRFD, and AH-EN is high, activating U230A. The high output of U230A will cause a high on the BTNRFD line.

When DAV is asserted, R-DAV will go high, releasing the clear input of U330A. When the MPU has received the byte from the PIA, it will pulse DATACC by writing to address 0C40 (hex). The positive transition of DATACC will clock U330A and its Q output will go low, releasing T-NDAC (Transmit NDAC) and disabling U230B. The low output of U230B will cause a high on the BTNDAC line via U112F. The high on NDAC will tell the talker that the 7612D has accepted the byte. The interface is now in the ACcept Data State (ACDS-number 5 in Figure 3-40).

When NDAC goes high, the talker will release DAV. The low on R-DAV clears U330A and NDAC will be asserted. Because DAV is not asserted, DATVAL will be high. The MPU will continue to assert BUSY until it finishes processing the byte. When BUSY goes low, the output of U400B will go high. Now that the output of U400B and DATVAL are high, the output of U400A will go low, releasing NRFD. This will complete the acceptor handshake.

Attention Messages. When the controller-in-charge of the IEEE 488 bus asserts the ATN line, all devices on the bus must listen regardless of their present status. When R-ATN goes low (asserted), the negative transition will generate an interrupt to the MPU. The MPU will temporarily suspend its current task and prepare to receive input from the bus.

The low on R-ATN will cause the output of U600C (lower right center of diagram 21) to go low. The low on PFCA (Power Fail, interface Clear, or Attention) will stop the source handshake in progress. The low on R-ATN will also cause the output of U400B (right-center of the diagram) to go high, unasserting T-NRFD and, via U230A and U030A, BTNRFD.

If the 7612D was transmitting a byte when ATN was asserted and if the attention message did not abort the transmission (e.g., the message was not DCL, MLA, or UNT), the interface will resume talking when R-ATN goes high. The IEEE 488 standard requires that the talker wait at least 1.1 μs after R-ATN goes high before talking. One-shot U130A generates this delay. On the positive transition of R-ATN, R-ATN will go low, triggering U130A. The high on U130A's Q output will prevent U032A from being clocked and asserting DAV. If another byte is ready to be sent when U130A times out, U032A will be clocked and will assert DAV. The handshake process will then continue as previously described.

Interface Clear Latch. When the IEEE 488 bus IFC line is asserted the interface will be reset to its idle state. The low on IFC will assert R-IFC, setting interface clear latch U622C and U622D (bottom center of diagram 21). The output of the latch, IFCL will go low, interrupting the MPU and disabling the output drivers for the IEEE 488 bus. The high on R-IFC will also cause the output of U600C to go low, asserting PFCA and clearing the source handshake logic.

The interface clear latch will remain set until the MPU responds by releasing the TALK-MPU or LISTEN-MPU levels if either was asserted. Then the output of U620A will go high, clearing the latch.

22 XYZ DISPLAY

The XYZ Display circuitry converts the 7612D's digital data into three analog voltages suitable to operate an external display device.

The X voltage is developed by first setting counter U022B, U210A and B, and U212A and B to zero with the CLP pulse. A high level on the Display line then permits Send pulses to increment the counter. The changing digital value on the X0 through X9 lines is connected to D/A converter U310, which produces an analog current proportional to the digital input. Amplifier U300 changes U310's current output to the X output voltage.

The Y voltage is developed by applying the Y data lines, which come via FF U430 from the Code Converter/Check-Sum Generator, to D/A converter U332. There are nine Y data lines. The Y0-Y7 lines are data and the Y8 line is the position bit, which designates the data as A or B data. Converter U332 produces an analog current that amplifier U200 changes to the Y output voltage.

To generate the Z output, U600B monitors the outputs of exclusive-OR gates U030 and U322, and one-shots U120A and B. The exclusive-OR gates will produce a high output when the HD data is at either end of its Y range, zero or 255. For all intermediate values the gates' output will be a low that will, via U122D, enable U600B. When a Send pulse clocks one-shots U120A and B, they produce pulses of about 1.5 μs and 10 μs, respectively. Because the 1.5 μs pulse from U120A is negative, U600B will be activated when the 1.5 μs pulse ends, until the 10 μs pulse ends, when the Y value is between 1 and 254. Figure 3-41 shows this timing.

Selector P300 has the following two positions:

1. $\overline{\text{WF-EN}}$, which permits the circuit to operate normally, and
2. $\overline{\text{Test-EN}}$, which will substitute the four less-significant bits of data from the microprocessor for the Y5-Y8 bits, and will substitute the four more-significant bits of microprocessor data for the X6-X9 bits.

23 L TRIGGER

The L Trigger circuit generates the L Gate pulse for the Data Memory Control (diagram 10). It selects the trigger source, the level, the slope, and method of coupling.

INTERNAL AND EXTERNAL TRIGGERS

The L Int Trig In is a push-pull signal. Transformer T508, R504 and R508 balance and terminate the trigger signal. The ac component of the L Int Trig In reaches U722 via C524, and the dc component goes to U502.

The L Ext Trig In is separated into ac and dc components. The ac component reaches U722 via C612, and the dc component goes to U608.

Complementary MOS switch U522C selects the ac signal that will reach the trigger amplifier, U722. The LIT signal from the Trigger Control circuit, on diagram 25, controls U522C. Switch U522C connects the unselected input to −5 V through a resistor.

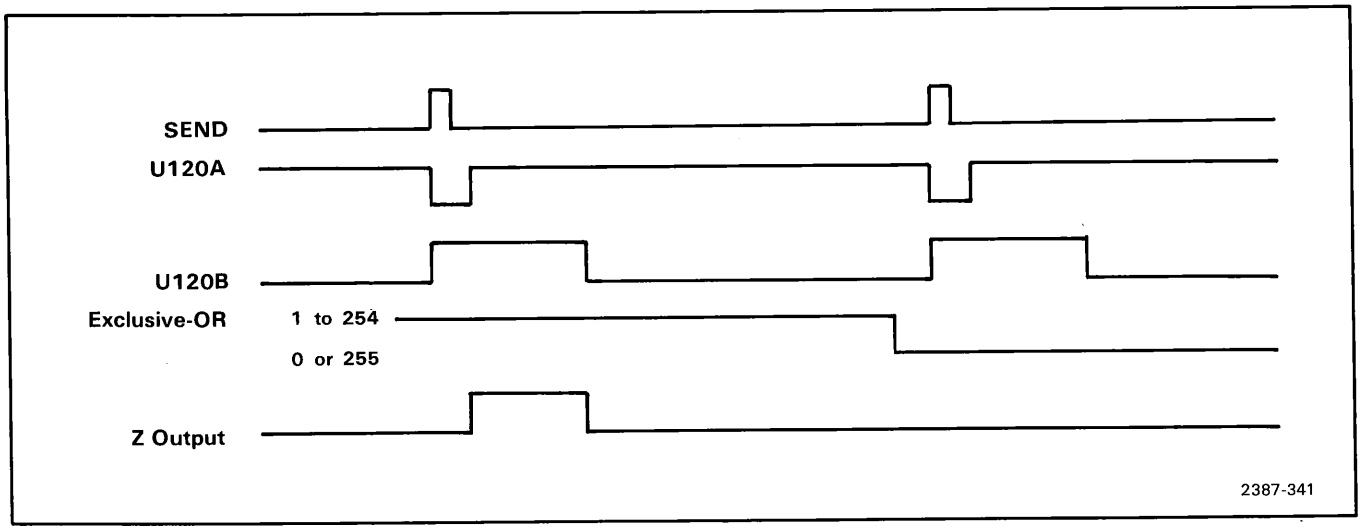


Figure 3-41. Timing of the Z signal.

When Internal Trigger source is selected, LIT will be high and U522C will connect U722's pin 2 input to −5 V through R522, which will turn on CR528 and CR529. The internal signal then reaches U722 pin 4, and the external signal is shunted to ground via CR528 and CR529.

When External trigger source is selected, LIT will be low and U522C will connect U722's pin 4 input to −5 V via R524. The negative voltage at pin 4 will turn off that input. Only the external signal will reach U722. Offset adjustment R702 provides a means of setting the output to zero when the input is grounded.

TRIGGER LEVEL

The Trigger Level circuitry provides a dc level to U722. This dc level determines the dc level of U722's output.

Converter U828 produces a current analogous to the eight L DAC inputs; U818 converts the current to a voltage that represents the selected trigger level.

Switch U522A selects a dc level from U502 or the external dc level from U608. When External trigger source is selected, the low on LIT will cause U522A to select the external signal. When Internal trigger source is selected, LIT will be high and U522A will select the internal signal.

Amplifier U716 sums the output of the trigger-level converter with the dc level of the selected trigger signal and applies it to the level control input of U722. When external trigger mode is selected the low on LIT will cause U816A to connect R806 in parallel with R704, which will effectively quadruple the influence of the trigger level. The L Norm Offset adjustment provides a means of setting the pin 10 input of U722 to zero when the Trigger Level is set to zero and there is no input signal.

COUPLING

When ac coupling is selected, the high on LAC will cause U522B to select its pin 3 input, which has C426 in its path. For dc coupling, the low on LAC will cause U522B to select its direct-coupled input.

When high-frequency reject is selected the low on LHFR will turn on CR538, which will reverse-bias Q624. In this condition, C629 and internal parts of U722 form a low-pass (high-frequency reject) filter, and only low-frequency signals will reach U722's output.

SLOPE SELECTOR AND GATE GENERATOR

Integrated circuit U732 converts the output of U722 to differential gate pulses for the Data Memory Control (diagram 10) and the L Trig'd pulse generator.

The level on the $\overline{\text{L +Slope}}$ line determines the slope on which U732 will produce its output. When $\overline{\text{L +Slope}}$ is low U732 will switch on the positive slope of its input signal. A high level on $\overline{\text{L +Slope}}$ will cause U732 to trigger on the negative slope of its input. The L Slope Balance adjustment, R703, permits the trigger points for + and − slopes to be centered about zero, or balanced.

Level-shifters Q626 and Q628 produce the ECL-compatible L Gate Out signal for the Data Memory Control. The output of Q626 also goes, via Q632, to one-shot U544A and U836. When U732's pin 3 output goes positive Q632 will trigger one-shot U544A, which will produce a 110 ms positive-going pulse on the L Trig'd line for the front-panel L TRIGGERED indicator. The Q output of U544A goes to gated inverter U746E; a low on Read Enable will gate the output of U544A to the MPU via the Trigger Control circuit (diagram 25) as a low on B05. Read Enable also gates U746C, which will invert the Trig'd level from the R Trigger and send it through the Trigger Control circuit to the MPU.

24 R TRIGGER

The R Trigger circuit generates the R Gate Out Pulse for the Data Memory Control (diagram 10). It selects the trigger source, the level, slope, and method of coupling.

The R Trigger circuit is functionally identical to the L Trigger circuit. Only the component numbers differ. Refer to the description of the L Trigger circuit for details of operation.

25 TRIGGER CONTROL

The Trigger Control circuit routes control data from the MPU BD bus to the L and R Trigger circuits.

Decoder U644 receives the BADR0, BADR1, and BADR2 lines. When the $\overline{\text{TRG SEL}}$ line is low and the BR/$\overline{\text{W}}$ line is low, a Strobe pulse can activate U644. When activiated, U644 will decode its inputs and produce a low output that will clock data into one of the flip-flops. The output of FFs U848, U542, U442, and U246 are the trigger level and setup information for the left and right trigger circuits, respectively.

The pin 9 output of U246C (ECK) selects the source of the clock signal; when ECK is high it selects the external clock.

26 27 28 29 POWER SUPPLY

The Power Supply consists of the Line Input/Fan, Power Control, Inverter Rectifier, and Regulators circuits, shown on diagrams 26, 27, 28 and 29 respectively.

The Power Supply provides operating power for all 7612D circuits and its plug-in amplifiers. The supply also provides regulated ac power for the cooling fan to ensure adequate cooling at all line voltages. REMOTE ACTUATE and REMOTE ENABLE input connectors on the rear panel allow the 7612D to be connected as part of a system with "daisy-chained" power control.

Figure 3-42 shows a simplified block diagram of the Power Supply.

LINE INPUT/FAN

Diagram 26 shows the Line Input/Fan circuit.

Line Input & EMI Suppression

Line power reaches the supply via FL5020 (top left of diagram 26). Line filter FL5020 suppresses interference from the power line and keeps the inverter signal from entering the power line.

Spark Gaps, Rectifiers, Thermistors, Filters

Thermistors RT651 and RT661 limit the surge current demanded by the supply when it is first turned on. After the instrument is in operation, the resistance of the thermistors drops so they have little effect on the operation of the supply. The rear-panel PRINCIPAL POWER SWITCH (S5020) disconnects all input power from the instrument. During normal operation, S5020 is left on and power is controlled by the front-panel ON/OFF switch. If the internal temperature of the instrument rises beyond safe limits, thermal switch S5022 opens the power input circuit. Spark gaps E641 and E721 protect the rectifier and filter circuits from line surges over 230 Volts peak-to-peak.

Line Selector Switch S5021 allows the 7612D to operate from either a 132- or 250-volt nominal line voltage. In the 132-volt position, CR531 and CR532 operate as a full-wave voltage doubler. On alternate cycles of the line input, C461 and C542, and C161 and C361 charge to near the peak voltage. The capacitors are in series with the input of the inverter, so the voltage applied to the inverter transformer is the peak-to-peak line voltage. When S5021 is set to the 250-volt position, CR531, CR532, CR533 and CR534 operate as a full-wave bridge rectifier, and the output voltage across C461 and C361 is the peak value of the line voltage. As a result, the output voltage applied to the inverter stage is about the same for 132- and 250-volt operation. The output of the rectifier passes through L451, C341, R341, and L261, C241, R251, and goes to the main inverter.

EMI Suppressor

Transformer T421, R431, L321, L331 and C121 suppress any electromagnetic interference on the rectified output that goes to the main inverter.

Fan Drive

The Fan Drive circuit, shown at the top of diagram 26, generates regulated 90 V, 60 Hz power for the cooling fan. Figure 3-43 shows a simplified block diagram of the fan circuit.

Oscillator U611A produces the 60 Hz clock signal for the fan supply. The clock signal is fed to U611B, which acts like an RS flip-flop, and one input of U611D, which acts an exclusive-OR gate. On each transition of the clock signal, a pulse passes through differentiator C601-R602. Negative-going pulses pass through CR601 to the noninverting (+) input of U611B, and positive-going pulses pass through CR701 to the inverting (−) input. The result is a negative-going output on every clock transition. Positive feedback through R706 causes U611B to latch the output in its low state on each transition. Figure 3-44 shows the timing of events in the fan circuit.

Referring to Figure 3-44, when the 60 Hz clock has a negative transition, the output of U611B goes low, forward-biasing CR702. This pulls pin 13 of U611D low, and the output (pin 14) goes high. Because the output of U611A is low, current flows from the output of U611D through the primary of T511 to the output of U611A. This provides base drive to one output transistor (Q501 and Q502) and reverse-biases the other.

A sample of the fan-drive voltage is fed back to integrator R621-C721, and C721 starts charging toward the fan voltage. Diodes CR611, CR612, and U611C comprise a full-wave rectifier with unity gain. When the charge on C721 reaches +10 V, the output of U611C forward-biases CR711, forcing pin 5 of U611B high enough to set the FF. Now the output of U611B is high and the output of U611A is low. The voltage on the inverting input (pin 6) of U611D is more positive than the voltage on the noninverting input (14 V), so the output of U611D goes low. Because both ends of the transformer primary are low, no current flows and both output transistors are cut off.

When the clock signal goes high, U611B is reset and its output goes low. Current flows in the opposite direction through T511, providing base drive to the other output transistor. Capacitor C721 begins charging toward the fan voltage. When the voltage reaches −10 V, FF U611B is set and its output goes high, setting the output of exclusive-OR U611D high. With both sides of the transformer high, no primary current flows and the output transistors are turned off. When the 60 Hz clock goes low the cycle repeats.

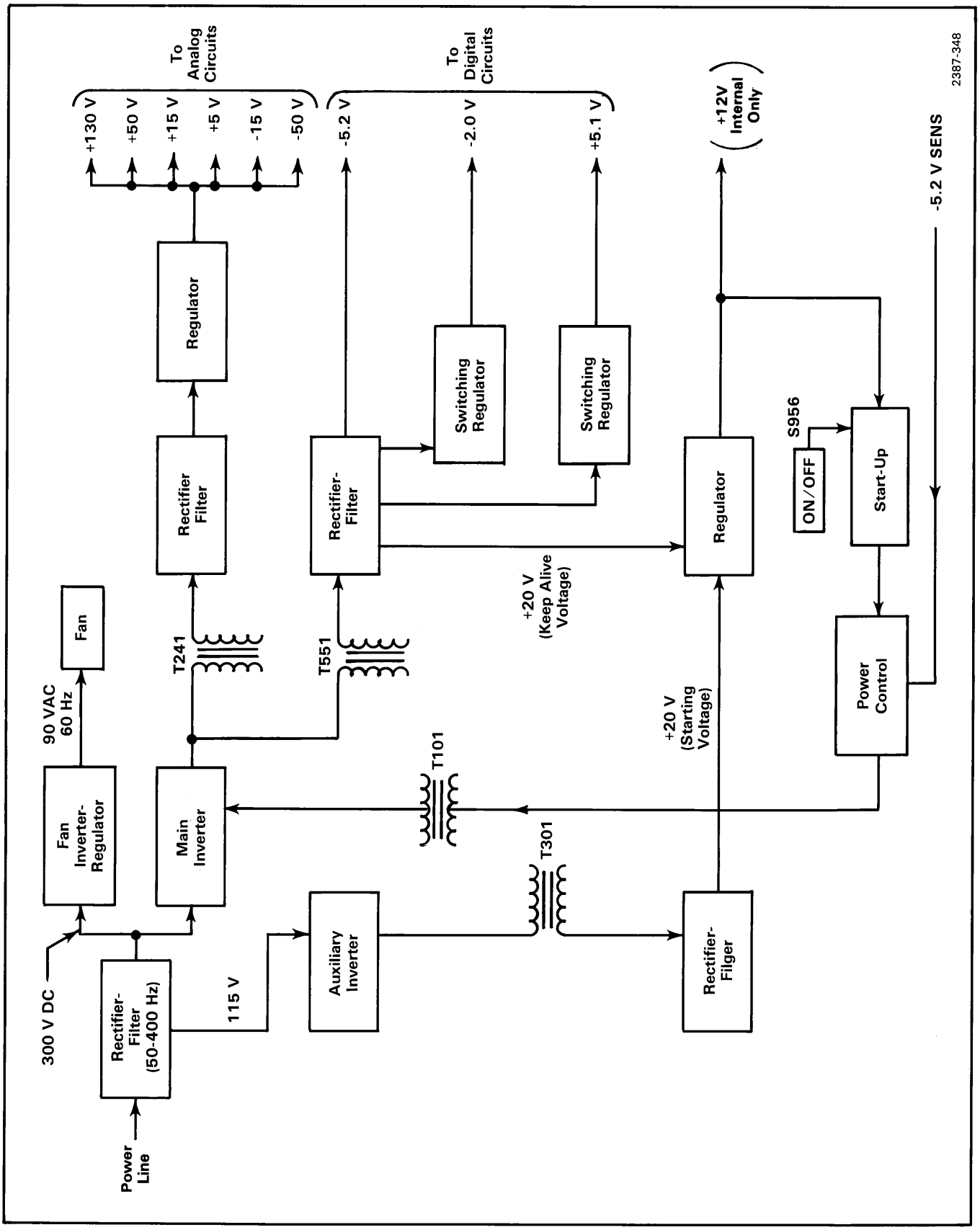


Figure 3-42. Simplified block diagram of Power Supply.

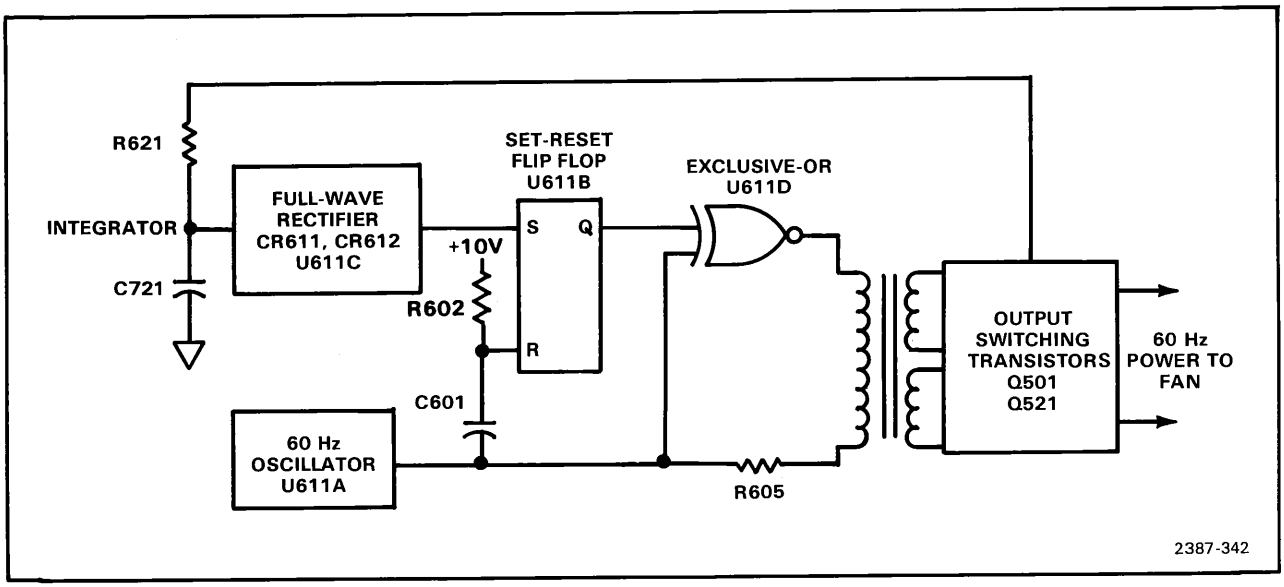


Figure 3-43. Simplified block diagram of the fan circuit.

If the fan voltage drops, the charge on C721 takes longer to reach the 10 V "set" threshold of FF U611B. As a result, the output current flows for a longer time, producing a constant volt-seconds product. Because the fan is an inductive load, a constant volt-seconds product causes a current that makes the motor run at a constant speed.

Auxiliary +20 V Supply

The Auxiliary +20 V Supply produces +20 V for the +12 V Supply shown on diagram 27. The Auxiliary +20 V Supply consists of rectifier CR321, amplifier U405, inverter transistors Q411 and Q412, transformer T301, diodes CR311-CR314, and filters L301 and L302.

Amplifier U405 operates as an oscillator at a frequency of 25-30 kHz. Transistors Q411 and Q412 drive the primary of transformer T301, and diodes CR311-CR314 rectify the output.

Main Inverter

The Main Inverter "chops" the dc output of the rectifiers to form an ac drive signal for the two input transformers for the analog and digital power supply voltages. The Main Inverter consists of T101, Q011, Q012, Q031, Q041 and related parts.

Transformer T101 receives the 20 kHz output of the Base Drive stage (on diagram 27). The outputs of T101's four secondary windings control switching transistors Q011, Q012, Q031 and Q041 as follows:

a. One alternation causes pins 3, 4, 6 and 10 of T101 to be positive with respect to pins 2, 3, 7, and 9. (Pin 3 is mentioned twice because two windings connect to it.) This turns on Q012 and Q031, and turns off Q011 and Q041. When they conduct, Q012 connects the negative rectifier voltage to pin 5 of P124, and Q031 connects the positive rectifier voltage to pin 1 of P124.

b. The other alternation causes pins 3, 4, 6 and 10 of T101 to be negative with respect to pins 2, 3, 7 and 9. This turns on Q011 and Q041, and turns off Q012 and Q031. When they conduct, Q011 connects the positive rectifier voltage to pin 5 of P124, and Q041 connects the negative rectifier voltage to P124 pin 1.

By repetitively switching the rectifier output voltage, the main inverter furnishes ac voltage for the transformers that drive the rectifiers for the analog and digital supply voltages.

+10, +28 V Supply

The +10 V, +28 V Supply is used to operate the circuitry in the Fan Drive circuit on diagram 26. The supply consists of rectifier CR241, filter L521-C521-R622-C711, and zener diodes VR601 and VR602. The +10 V, +28 V Supply is shown on the lower-right corner of diagram 26.

POWER CONTROL

Diagram 27 shows the Power Control circuit.

Power On-Off Switching

The Power On-Off Switching (POOS) circuitry can turn the Power Supply on and off. It does this by governing the oper-

ation of the Base-Drive Logic circuit that controls the Main Inverter. The principal parts of the POOS circuit are Q151, U141A and U261F.

The POOS circuit has two inputs, the ON/OFF switch on the front panel, and the REMOTE ACTUATE input connector. When the ON/OFF switch (S956 on diagram 2) is pressed it causes a negative transition on the POWER ON line. (The on-off circuit produces a brief low each time the ON/OFF button is pressed.) Via U261F, the $\overline{\text{POWER ON}}$ signal clocks FF U141A, which produces a low level on its pin 2 (Q) output. The low level from U141A pin 2 causes:

a. via U261C, a high that enables the Base-Drive Logic, and

b. via U451C, Q062 and Q061, a low level on the REMOTE ENABLE line. Resistor R363 and C361 provide a 150 ms delay before the REMOTE ENABLE signal occurs.

While the 7612D is operating, U141A stays in the "set" condition—with its $\overline{\text{Q}}$ output applying a low level to the Base-Drive Logic and Remote Enable circuits, and to its own D input.

When the ON/OFF switch is pressed while the power supply is operating, the negative transition on the $\overline{\text{POWER ON}}$ line clocks U141A via U261F. Because its D input is at a low level, U141A switches to the reset state when it is clocked. When reset, the high level on the U141A's $\overline{\text{Q}}$ output causes:

a. via U261C, a low level that disables the Base-Drive Logic, and

b. via U451C, Q062 and Q061, a high level on the REMOTE ENABLE line. When a low level is applied to the REMOTE ACTUATE line, it will turn off Q161. The collector voltage of Q161 will set FF U141A, which will enable the Base-Drive Logic circuit and cause a low on the REMOTE ENABLE line. In this condition the ON/OFF switch is locked out because U141A is held set.

When the switch closure is removed from the REMOTE ACTUATE line, Q161 conducts and applies a negative transition to Q151. Transistor Q151 then produces a positive pulse that resets FF U141A.

+5.1 V Reference

The +5.1 V Reference serves as the reference voltage for the −2 V and +5.1 V switching regulators. Zener diode VR421, potentiometer R521 and filter L341-C441 comprise the +5.1 V Reference.

40 kHz Clock

The 40 kHz Clock generates the reference signal that operates the Base-Drive Logic circuit. Comparator U451D and related parts comprise the 40 kHz Clock circuit. The level on the output of U261C controls the clock. A low output from U261C turns off the clock; a high output from U261C enables the clock.

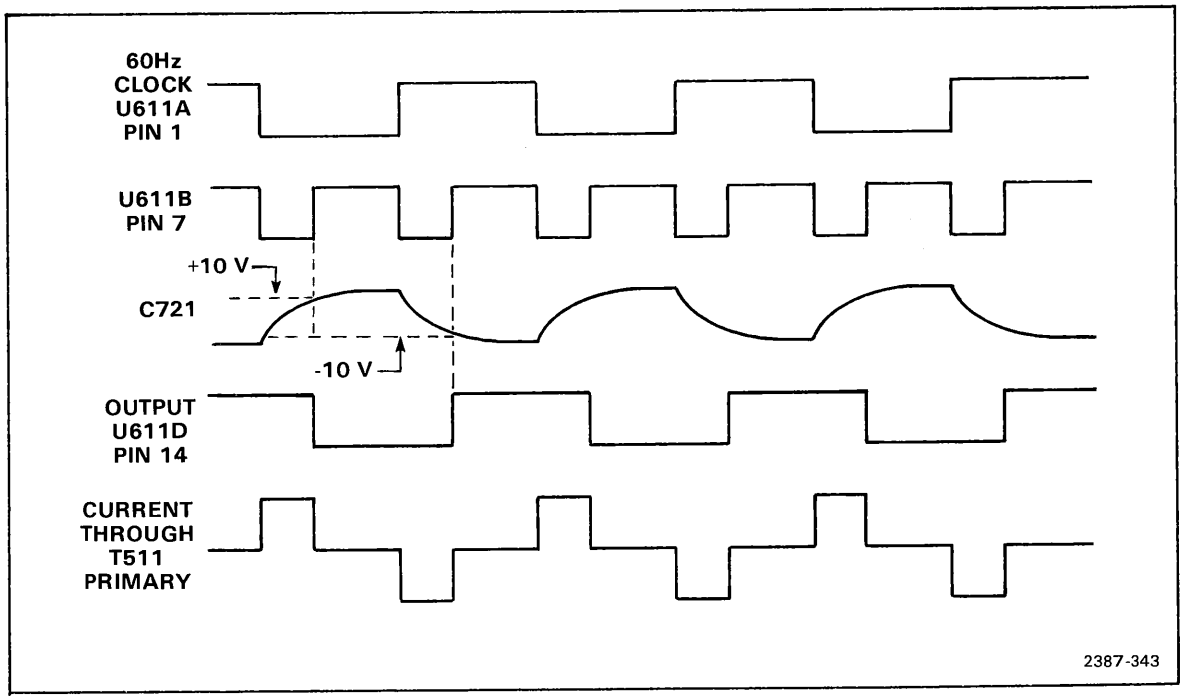


Figure 3-44. Timing of the fan circuit.

Power Control

Base-Drive Logic

The Base-Drive Logic (BDL) circuit produces pulses to drive the transistors that operate the Main Inverter. The BDL receives an input from the −5.2 V Voltage Regulator Comparator and adjusts the duration of the drive pulses to regulate the −5.2 V output. The BDL consists of U141B, U231A, B and C, and U251B, C and D.

Via U231A, negative transitions of the clock signal from U451D clock FF U141B. The positive transitions of clock reset U231B and C. When U231B-C is set, its pin 10 output activates U251B. The high output of U251B enables gates U251C and D, which receive the outputs of FF U141B. Because of this, U251C and D will always turn on one output driver and turn off the other when they are enabled, depending on the state of FF U141B. When the Voltage Regulator Comparator senses that the output of the −5.2 V supply is more negative than −5.2 V, U451B will produce a negative transition that flips U231B and C. The output of U231C disables U251B, whose low output disables U251C and D and ends the pulse to the Driver stage. This sequence repeats during the next clock cycle, this time turning on the other Driver stage. Figure 3-45 shows the timing of signals in the Base-Drive and Driver circuits.

−5.2 V Regulator & Current Limiter

Two comparators serve as Voltage Regulator and Current Limiter for the −5.2 V power supply. Comparator U451B is the Voltage Regulator and U451A is the Current Limiter.

Voltage Regulator U451B compares the sum of the −5.2 V output voltage and the +5.1 V Ref with the Com Sense voltage. During each cycle, the main inverter drives the −5.2 V rectifier until the −5.2 V output voltage causes comparator U451B to switch. Comparator U451B then produces a negative output that flips U231B and C, which ends the drive to the main inverter. The −5.2 V output then falls below −5.2 V and U451B produces a positive output that permits U231B and C to be "set" by the next clock pulse to start another drive cycle to the main inverter.

Current Limiter U451A senses the voltage across R111 (diagram 28). If the output current reaches 32 amperes, the voltage developed across R111 will cause pin 4 of U415A to become 160 mV more positive than pin 5. This will cause U451A to switch, and produce a low output that will flip U231B and C and shut off the driver stage. Consequently, the output current stops increasing—it is effectively limited.

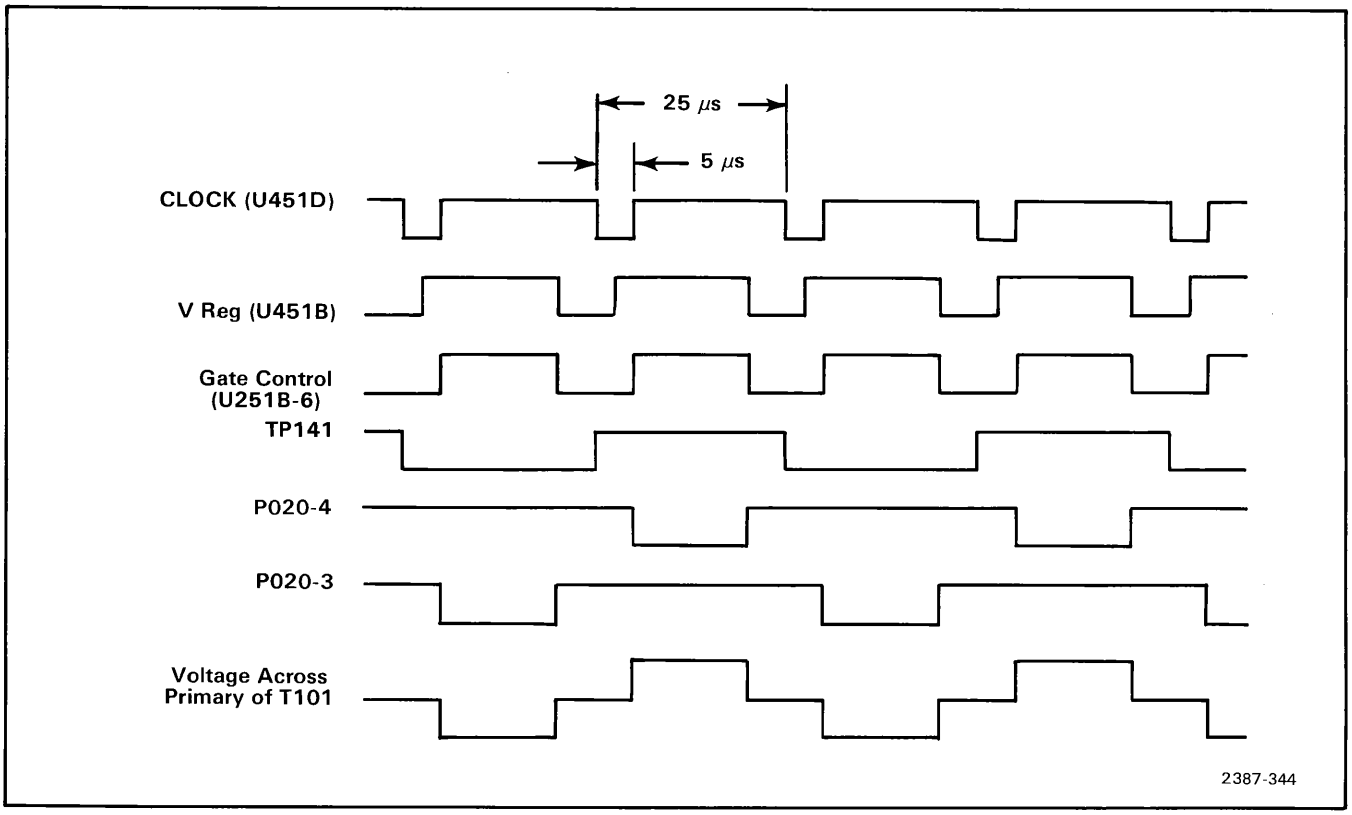


Figure 3-45. Timing of signals in base-drive logic and driver circuits.

Power-On Sense

The Power-On Sense (POS) circuit senses the outputs of the −5.2, −2, and +5.1 V supplies, and the input to the Base-Drive Logic circuit. When all is well with these four voltages, the POS circuit will assert a high level on the PON line. If one of these levels is at a level below its correct level, the POS circuit will signify that by asserting a low level on PON. The POS circuit consists of inverters U261A and B and comparators U331A, B, C, and D.

Comparators U331A, B, C, and D are referenced to the +5.1 V Ref either directly (U331C) or via voltage dividers. The dividers produce reference voltages about 0.23 V less than the supply voltages the comparators sense. Comparator U331C compares the input to the Base-Drive Logic and the +20 V with the +5.1 V Ref voltage, which will be more positive than +5.1 V when the power supply is turned on and the line voltage is at least 80 (or 160) V rms. (The +20 V is proportional to the line input voltage.) As long as the output of U261B is +5.1 V or higher, U331C will produce a high output. If the output of U261B goes below about +4.6 V, U331C will produce a low level on the PON line. As long as the −5.2 V and −2 V supply outputs are at their correct levels, U331A and U331D will assert high outputs. If either the −5.2 or the −2 V supplies goes about 0.3 V more positive, its comparator will produce a low level on the PON line. In like fashion, if the +5.1 V falls about 0.3 V more negative U331B will produce a low on the PON line.

+12 Volt Supply

The +12 V Supply furnishes +12 V for the Power-On Sense, Power On-Off Switching, 40 kHz Oscillator, and Base-Drive Logic parts of the Power Control circuitry; and for the −2 V and +5.1 V Supplies on the Rectifier Board.

The +12 V Supply consists of VR411, Q412, Q413, Q411 and VR412, which establish a reference of +12.5 V. Via emitter-follower and filter network Q311, C312, Q301, C311 and C252, the +12 V is applied to the output.

INVERTER RECTIFIER

Diagram 28 shows the Inverter Rectifier circuit.

Rectifier

+5.1 V Supply

The +5.1 V Supply produces regulated +5.1 V for the digital circuits in the 7612D. Comparators U501 and U601B, transistors Q211, Q411, and Q501, transformer T211 and related parts comprise the +5.1 V Supply.

When the 7612D is first turned on, the +5.1 V Reference voltage comes on. Because the output of the +5.1 V Supply is low, U501 applies a low to the base of Q411, which turns on Q411. The collector current of Q411 turns on Q211, which conducts current through a winding of T211. This current in T211 causes T211 to increase the forward bias on Q411, which saturates it. Transistor Q211 supplies the unregulated dc to a filter consisting of L421, C112, C101, L001, and C031. While Q211 conducts, the output voltage increases until it reaches +5.1 V; then comparator U501 switches and turns off Q411 and Q211. The output voltage now decreases and turns on U501. This action continues, providing regulated +5.1 V.

Resistor R201 senses the output current. When the output current approaches 14 A, R201 causes the pin 5 input of U601B to be 0.14 V more negative than its pin 6 input. This bias causes U601B to produce a negative output which turns off Q501 and U501. When it is turned off, U501 turns off Q411, which turns off Q211 and stops the output current.

−2 V Supply

The −2 V Supply provides regulated −2 V for the digital circuits in the 7612D. Comparators U511 and U601A, transistors Q421, Q502 and Q511 comprise the −2 V Supply.

Comparator U511 compares the sum of the −2 V and the +5.1 V Ref with the sum of the Com Sense and Com Ramp voltages. When the 7612D is first turned on, the +5.1 V Ref comes on. Because the output of the −2 V Supply is low (more positive than −2 V) and because there is no inversion between U511's minus input and its inverting output, U511 produces a positive output that turns on Q502. Transistor Q502 then turns on Q511 and Q421, and Q421 conducts power to the output. When the output reaches −2 V it turns off U511, and the −2 V output goes positive enough to turn on Q511. This action occurs repetitively, producing the regulated −2 V output.

If the −2 V output current approaches 10 A, the voltage on R532 will bias U601A (pin 3) 0.1 V more negative than pin 2. Comparator U601A then produces a negative output that turns off Q502, whose high level output turns off Q511 and Q421, thereby limiting the output current.

−5.2 V Supply

The −5.2 V Supply provides regulated −5.2 V for digital circuits in the 7612D. Rectifiers CR531, CR631, and filter L121, L221, C113, C111, L011, and C011 comprise the −5.2 V Supply.

The −5.2 V rectifier and filter is located on the Rectifier Board (A86) and the regulator is situated on the Control Board (A82). Regulation is accomplished by using the output of the −5.2 V to control the conduction cycle of the main inverter. Refer to "Base-Drive Logic" for details of the regulation.

Rectifiers for Digital Supplies

Three pairs of rectifiers provide input voltages for the −5, −2, and +5.1 V regulators, and for the +12 V Supply. Rectifiers CR531 and CR631 provide about −6 V for the −5.2 V and −2 V regulators. Rectifiers CR231 and CR331 provide about +12 V for the +5.1 V regulator. Rectifiers CR561 and CR562 provide +20 V for the +12 V Supply on the Control Board (diagram 27).

Rectifiers for Analog Supplies

The Rectifiers for Analog Supplies produce the unregulated dc voltage for the regulators that provide power for the analog circuits in the 7612D. There are four rectifier circuits, as follows:

1. Bridge rectifier CR041, CR042, CR043 and CR141 produce + and −17 V for the + and −15 V regulators.

2. Full-wave rectifier CR142 and CR143 produce +7 Volt for the +5 V regulators.

3. Bridge rectifier CR351, CR352, CR353 and CR451 produce + and −54 V for the + and −50 V regulators.

4. Bridge rectifiers CR161, CR162, CR261 and CR262 produce 86 Volts, which is added to +54 V to become +140 V for the +130 V regulator.

+20 V Unregulated Supply

The +20 V Unregulated Supply produces the +20 V Unregulated voltage for the +12 V Supply. When the Main Inverter is operating, rectifier CR561 and CR562 and filter C461 provide the unregulated +20 V, which is greater than +20 V.

REGULATORS

Diagram 29 shows the Regulators.

Hardware Fault (HWF) Detector

The HWF Detector senses the outputs of the +130, +50, +15, +5, −15, and −50 V supplies. If a failure occurs on any of them, the HWF Detector will produce a low level on the HWF line. The HWF Detector consists of VR504, U510A, B, C, and D.

Zener diode VR504 acts as a reference for the HWF Detector. When the analog supplies are operating normally, the minus inputs of U510B and D are more negative than their plus (reference) inputs, and the plus inputs of U510A and C are more positive than their minus (reference) inputs. The four comparators produce high outputs, and the HWF line will be at a high level. If a fault should occur on any of the six analog supply voltage lines, one section of U510 will produce a negative output on the $\overline{\text{HWF}}$ line.

+22, +5.6, −5.6, −22 V Supplies

These supplies provide operating power for the six regulators that produce the +130, +50, −15, and −50 V. The +22 Volt source consists of Zener diode VR316, emitter-follower Q414, and filter capacitors C506, C202, C218, and C226. The +5.6 V source consists of Zener diode VR324 and filter capacitors C326, C248, and C336. The −5.6 V source consists of Zener diode VR344 and filter capacitors C346, C102, C220 and C232. The −22 V source consists of Zener diode VR348, emitter follower Q446, and filter capacitors C240 and C246.

+130 V Regulator

The +130 V Regulator is a series-pass regulator that accepts the +140 V pre-regulated voltage and produces regulated +130 V for the 7612D's analog circuits. The +130 V Regulator consists of comparator Q620, error amplifier Q524, driver Q532, series-pass transistor Q636, and current-limit transistor Q436.

Comparator Q620 compares the sum of the +130 V output to the −50 V. If the +130 V output rises above +130 V, Q620B will rob current from Q620A and Q620A's collector voltage will rise. Error amplifier Q524 will invert and amplify Q620A's output, causing a lower dc level to driver Q532. The lower voltage at Q636's base will reduce the output voltage to the correct level.

If more than 50 mA is drawn from the +130 V supply, the voltage it develops across R532 will turn on Q436. When turned on, Q436's output voltage will reduce the drive to Q532, which will reduce the output current.

+50 and −50 V Regulators

The +50 and −50 V Regulators operate identically. The −50 V Regulator is described here.

Comparator U244B compares the sum of the −50 V and the common voltage with −6.2 V from VR256. The output of U244B causes the output stage (driver Q050 and pass transistor Q044) to produce the output of −50 V. Potentiometer R255 permits the output to be set to exactly −50 V.

Transistor Q148 senses the voltage developed across current-sensing resistor R056. In noncurrent limiting (normal) operation, Q148A conducts about 4 mA and Q148B is turned off. When the output current approaches 500 mA, the voltage at the emitter of Q044 becomes more negative than the −50 V output, and turns on Q148B. When Q148B conducts, it robs base current from Q050, which reduces drive to pass transistor Q044 and limits the output current. As the output voltage falls, R147 reduces the output current-limit point (fold back).

The −50 V Sens line is the voltage reference for the other analog regulators.

+15, +5, −15 V Regulators

The +15, +5, and −15 V Regulators are functionally identical. The +15 V Regulator is described here.

Comparator U216B compares the +15 V output voltage to the −50 V Sens voltage. The output of U216B controls driver transistor Q018, which drives pass-transistor Q014. If the output voltage rises above +15 V, U216B's minus input will go positive by a small amount and U216B will then produce a negative output that will reduce the output voltage to its correct value.

If excessive current is drawn from the +15 V supply, R112 will cause a positive-going signal at U216A's minus input. Comparator U216A will then produce a negative-going output that will reduce the output of the pass transistor, limiting the output current.

REAR PANEL

Diagram 30 shows the sources and destinations of the signals connected to the rear panel connectors.

INSTALLATION AND MAINTENANCE

This section contains installation and maintenance instructions for service personnel. The Installation part tells how to: a) install the 7612D in a rack, b) connect ac power and signal cables, c) configure an IEEE 488 system, and d) select internal jumpers. The Maintenance part gives detailed information about performing preventive maintenance, troubleshooting, and performing corrective maintenance.

INSTALLATION

INSTALLING THE 7612D IN A RACK

Hardware is supplied with the 7612D to mount it in a standard 19-inch rack. Part numbers and drawings of the hardware are shown with the accessories in the mechanical parts list in the back of this manual. The 7612D is supplied with the chassis slide tracks already in place.

The following rack dimensions are required:

Rack rail hole spacing	0.500 inches	(12.7 mm)
Minimum rack depth	27.5 inches	(700 mm)
Minimum width between rack rails	17.650 inches	(448 mm)

To attach the hardware to the rack, refer to Figure 4-1 and follow this procedure:

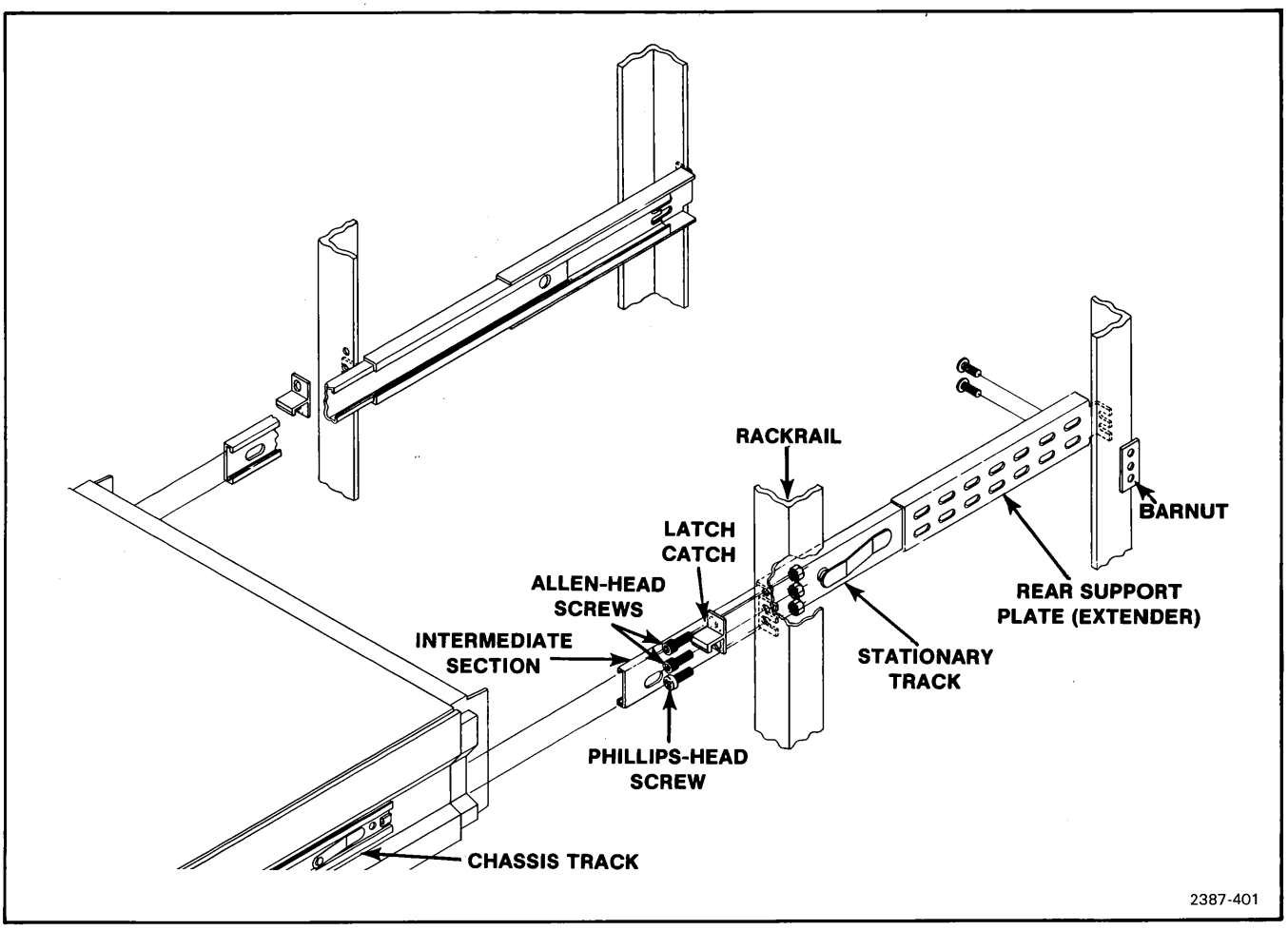


Fig. 4-1. Assembling the 7612D rackmounting hardware.

1. Measure the distance between the front and rear rails. Attach the rear support plates to the stationary slide tracks with bolts and bar nuts to match the rail spacing. Do not fully tighten the bolts. For shallow racks, the rear support plates can be reversed as shown in Figure 4-2. However, the rack cabinet must allow the 7612D to extend out the rear of the rack.

2. Install the latch catches on the front rack rails. The right and left catches are different. Install them so that the slots are toward the outside and the lip of the catch points down. If the rack rail is not threaded, install a nut on the top screw of each catch.

3. Install the assembled stationary tracks and rear supports. The right and left tracks are different; compare them to the chassis slide tracks on the sides of the 7612D to install correctly. Use nuts or bar nuts at the rear if the rack rail holes are not threaded.

4. Tighten the rack rail bolts enough to secure the stationary track and rear support, but still allow movement. Fully tighten the bolts that attach the rear supports to the stationary tracks.

5. Slide the intermediate sections into the stationary tracks so they lock in their extended positions.

6. Carefully lift the 7612D into place so the chassis tracks align with the intermediate sections (this may require two people). Slide the 7612D chassis tracks into the intermediate sections and push the instrument part way into the rack.

7. The sliding track sections should align themselves as the 7612D is pushed into the rack. Tighten all bolts with the sections aligned.

8. Push the 7612D into place in the rack and check that the latches catch properly.

Before operating the 7612D, check the environmental and physical specifications at the end of Section 1; the operating temperature and airflow requirements of the instrument must be met. Be sure there is nothing blocking the fan intake (screen on rear panel).

SIGNAL CABLES

Connect the X, Y, and Z outputs to a compatible display monitor with coaxial cables. Compatible monitors include the Tektronix 600-series monitors. Refer to the monitor manuals for correct connection at the monitor and for operating information. Because the signals are of relatively low

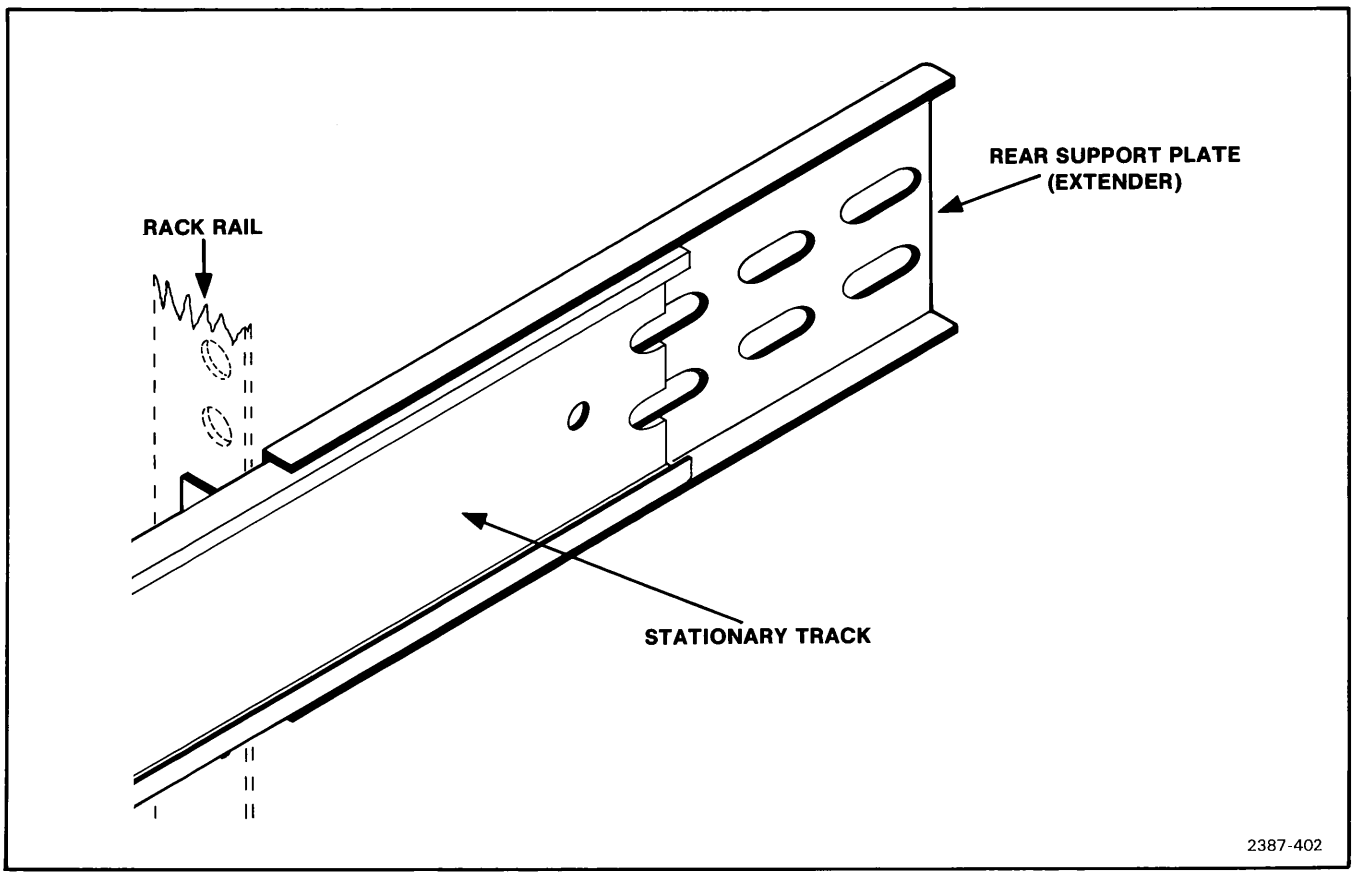


Figure 4-2. Reversing the rear support plates for a shallow rack.

frequency, the cable and termination impedance are not critical.

POWER CORD INFORMATION

WARNING

AC POWER SOURCE AND CONNECTION. This instrument operates from a single-phase power source. It has a three-wire power cord and a two-pole, three-terminal grounding-type plug. The voltage to ground (earth) from either pole of the power source must not exceed the maximum rated operating voltage of 250 volts rms.

Before making connection to the power source, determine that the instrument is adjusted to match the voltage of the power source, and has a suitable two-pole, three-terminal grounding-type plug. Refer any changes to qualified service personnel.

GROUNDING. This instrument is safety class I equipment (IEC designation). All accessible conductive parts are directly connected through the grounding conductor of the power cord to the grounding contact of the power plug.

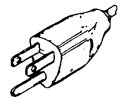
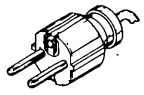
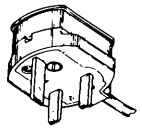
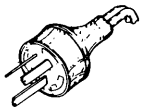
The power input plug must only be inserted in a mating receptacle with a grounding contact. Do not defeat the grounding connection. Any interruption of the grounding connection can create an electric shock hazard.

For electric shock protection, the grounding connection must be made before making connection to the instrument's input or output terminals.

TABLE 4-1
Power-Cord Conductor Identification

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral) Blue	White	
Grounded (Protective Ground)	Green-Yellow	Green-Yellow

The power-cord plug required depends upon the ac input voltage and the country where the instrument is to be used. Should you require a power-cord plug other than that supplied with your instrument, refer to the Reference Standards listed in Figure 4-3.

Plug Configuration	Usage	Nominal Line-Voltage (AC)	Reference Standards	Option #
	North American 120V/15A	120 V	[1]ANSI C73.11 [2]NEMA 5-15-P [3]IEC 83	STANDARD
	Universal Euro 240V/10-16A	240 V	[4]CEE (7), II, IV, VII [3]IEC 83	A1
	UK 240V/13A	240 V	[5]BS 1363 [3]IEC 83	A2
	Australian 240V/10A	240 V	[6]AS C112	A3
	North American 240V/15A	240 V	[1]ANSI C73.20 [2]NEMA 6-15-P [3]IEC 83	A4

[1]ANSI—American National Standards Institute
[2]NEMA—National Electrical Manufacturer's Association
[3]IEC—International Electrotechnical Commission
[4]CEE—International Commission on Rules for the Approval of Electrical Equipment
[5]BS—British Standards Institution
[6]AS—Standards Association of Australia

2387-413

Fig. 4-3. Power cord and plug identification information.

CONNECTING AC POWER

1. With the power cord disconnected from the power source, set the line voltage selector switch to the correct position for the local ac power line voltage. Either 115 V ac or 230 V ac, nominal, can be selected.

2. The 7612D power cord has a polarized, three-terminal power connector. If the connector does not match the power outlet, the user will need to replace the connector with one that meets local safety codes and connects the instrument for proper operation. Hook up a replacement connector according to Table 4-1.

3. Connect the 7612D power cord to an ac power line with the correct voltage and frequency. See the power input specifications in Section 1 for more information on the power requirements of the 7612D. Failure to supply the correct voltage and frequency on the ac power input can damage the instrument.

4. Set the PRINCIPAL POWER SWITCH on the 7612D rear panel to ON.

5. Connect input signals at the rear panel, if desired. Four inputs are provided: 1, 2, 3, and 4. These connect directly through 50 Ω coaxial cables to, respectively, 1, 2, 3, and 4 on the front panel. These straight-through connections are intended for routing signals through the instrument to or from the front panel for connection to the plug-ins or rear-panel inputs. For details, see the External Connectors specification in Section 1.

6. If remote power control of the 7612D is desired, connect a device capable of asserting a TTL active low to the 7612D REMOTE ACTUATE rear-panel connector. When it is turned on, the 7612D will assert a TTL active low on its REMOTE ENABLE output to provide a daisy-chain path for the remote power-control signal. The REMOTE ENABLE signal is delayed slightly to evenly distribute power-up surges if more than one system instrument is connected this way. For more information, refer to the power supply specification in section 1.

CONFIGURING AN IEEE 488 SYSTEM

A typical IEEE 488 system includes a controller, a talker, and one or more listeners. More than one function can be combined in a single instrument as is the case in the 7612D, which can be set either to talk or to listen by the controller. A system including a controller and the 7612D is shown in Figure 4-4.

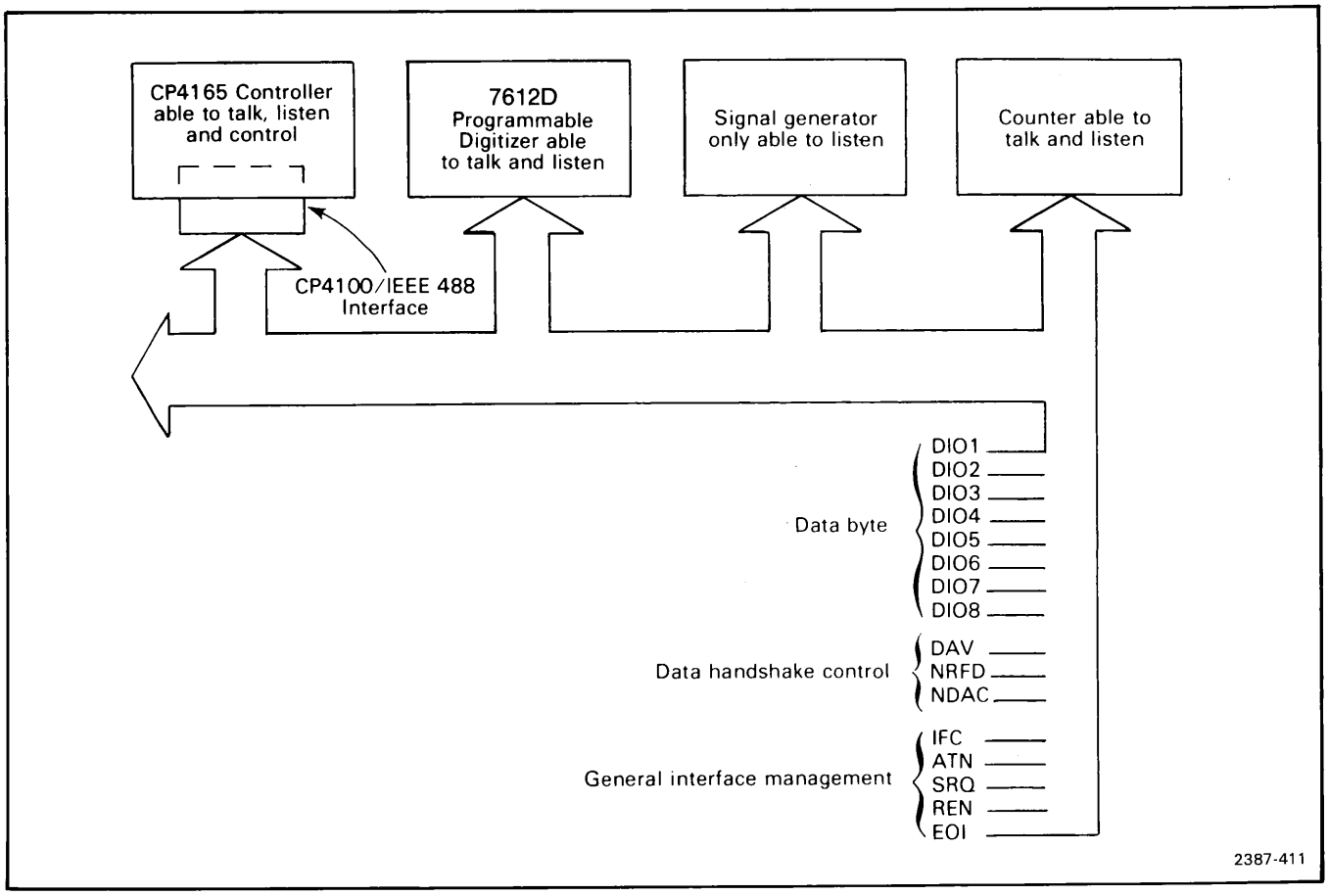


Fig. 4-4. An IEEE 488 system with typical instruments connected to the bus.

Up to 15 devices, connected by not more than 20 meters total cable length, can be interfaced to a single IEEE 488 bus. More than 15 devices can be interfaced if they do not connect to the bus but are interfaced through another device. Such a scheme is used for programmable plug-ins housed in the 7612D mainframe; the 7612D provides a transparent interface between the bus and the plug-ins.

IEEE 488 is a flexible system; it works either in a star or linear configuration (Fig. 4-5). To maintain the bus electrical characteristics, a device load must be connected for each two meters of cable and more than half the devices connected at any time must be powered-up. Although devices are usually spaced no more than two meters apart, they can be separated farther if the required number of device loads are lumped at any point. These lumped device loads, of course, must be included in the total instrument count.

To interface the 7612D to an IEEE 488 system, connect the IEEE 488 cable supplied with the 7612D between the rear-panel IEEE 488 port and the nearest instrument connected to the bus. If the system includes only the 7612D and a controller, the two-meters-per-instrument rule allows the cables from the two instruments to be connected for a total of four meters in bus length between the controller and instrument.

SELECTING IEEE 488 BUS ADDRESSES

Two sets of switches on the IEEE 488 Interface board (A56) select the primary and secondary addresses for the 7612D and programmable plug-ins (if used). The switches are shown in Figure 4-6.

S400 assigns either a one or a zero to each of the lower five bits in the 7612D primary bus addresses, My Talk Address (MTA) and My Listen Address (MLA). These bits are identified as T5 through T1 of MTA and L5 through L1 of MLA in the IEEE 488 standard. Values are assigned according to the following:

S400 Switch #	Address Bit
1	T5, L5
2	T4, L4
3	T3, L3
4	T2, L2
5	T1, L1

S402 assigns either a one or a zero to each of the lower five bits in the 7612D My Secondary Address (MSA). These bits are identified as S5 through S1 in the IEEE 488 standard. Values are assigned according to the following:

S402 Switch #	Address Bit
1	S5
2	S4
3	S3
4	S2
5	S1

Programmable plug-in units in the 7612D respond to the same primary bus addresses as the mainframe. The 7612D MSA is used to determine the plug-in unit MSAs according to the following:

Plug-in Compartment	MSA
CHANNEL A Plug-In Unit	7612D MSA + 1
CHANNEL B Plug-In Unit	7612D MSA + 2

For the first instrument connected to a controller with TEK SPS BASIC Software, the recommended bus addresses are:

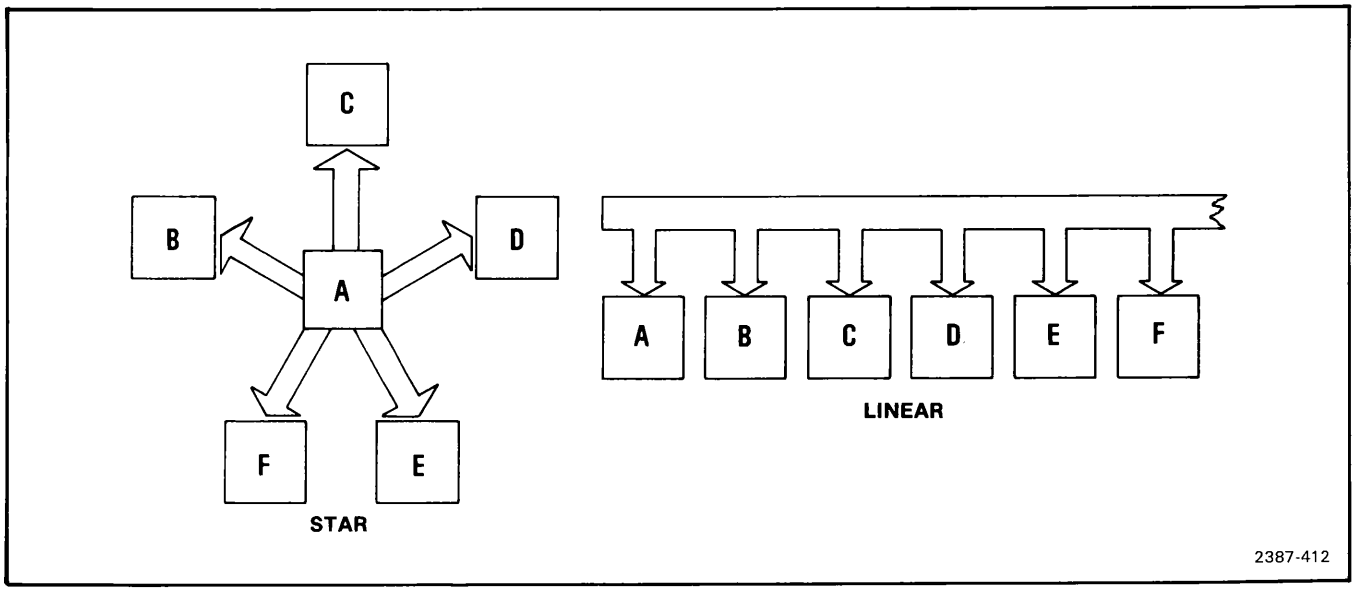


Fig. 4-5. Star and linear configurations of IEEE 488 systems.

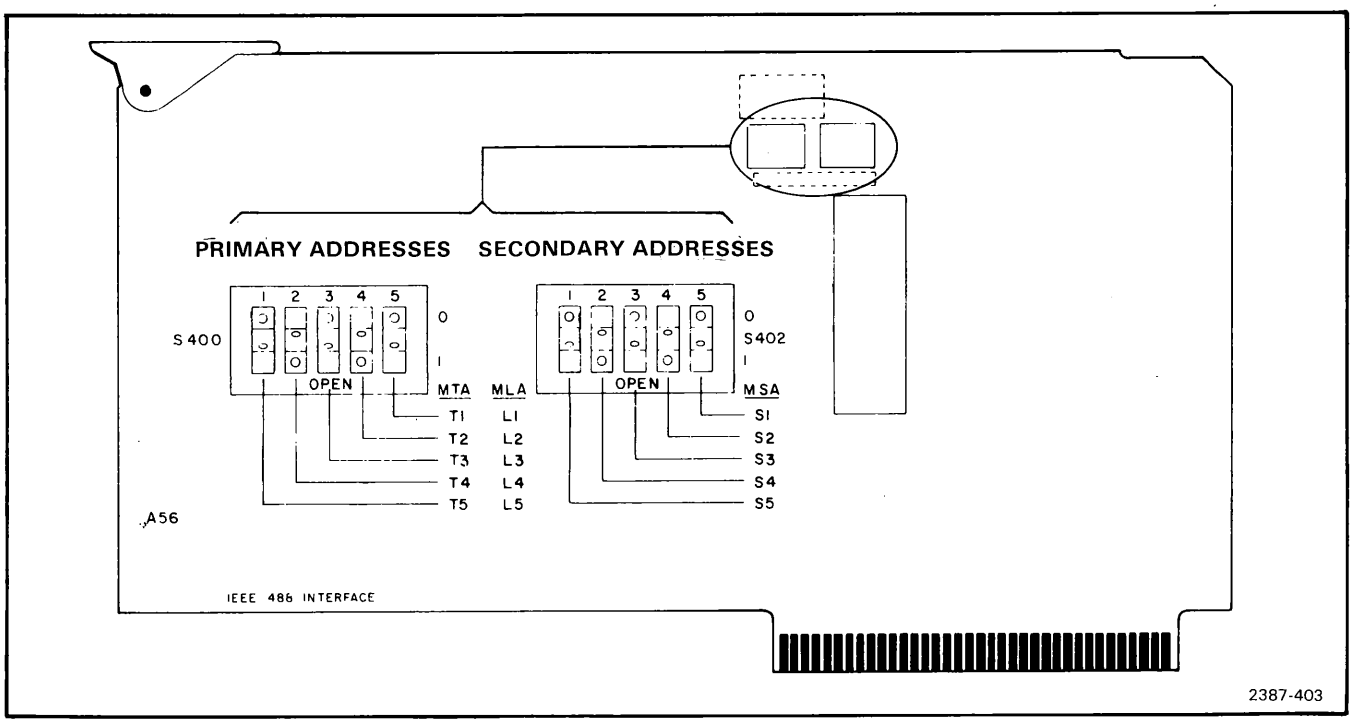


Fig. 4-6. The 7612D IEEE 488 bus address switches.

7612D Address	Value (hex)	(decimal)
MTA	20	32
MLA	40	64
MSA	60	96

For the above recommended addresses, set all switches on S400 and S402 to zero (up). Increment these addresses for each instrument added to the system.

For example, to set the primary talk address to 33 and the primary listen address to 65, set S400 as follows:

Switch #	Setting
1	Closed (Up, 0)
2	Closed (Up, 0)
3	Closed (Up, 0)
4	Closed (Up, 0)
5	Open (Down, 1)

To select other addresses, check the requirements in the IEEE 488 standard. Also, if programmable plug-in units are used, select a 7612D MSA no higher than 7C (hex).

SELECTING INTERNAL JUMPERS

Jumpers on circuit boards in the 7612D shown in the following illustrations are set to the standard position.

CLOCK BUFFER (A12)

Set jumper J510 for normal operation as shown in Figure 4-7. The other position is used to disable the clock outputs when troubleshooting.

DEFLECTION AMPLIFIER (A26)

Jumpers are required for normal operation as shown in Figure 4-8.

MICROPROCESSOR (A54)

Set the jumpers on J012, J224, J216, and J234 to RUN for normal operation as shown in Figure 4-9. Other positions are used only for special purposes during debugging.

Jumpers J712, J714, and J718 are set as shown in Figure 4-9 for normal operation. Set the jumpers to the opposite pins for the following:

J712—Ignore skip character in readout.
J714—CR/LF delimiter.
J718—Continue on power up error.

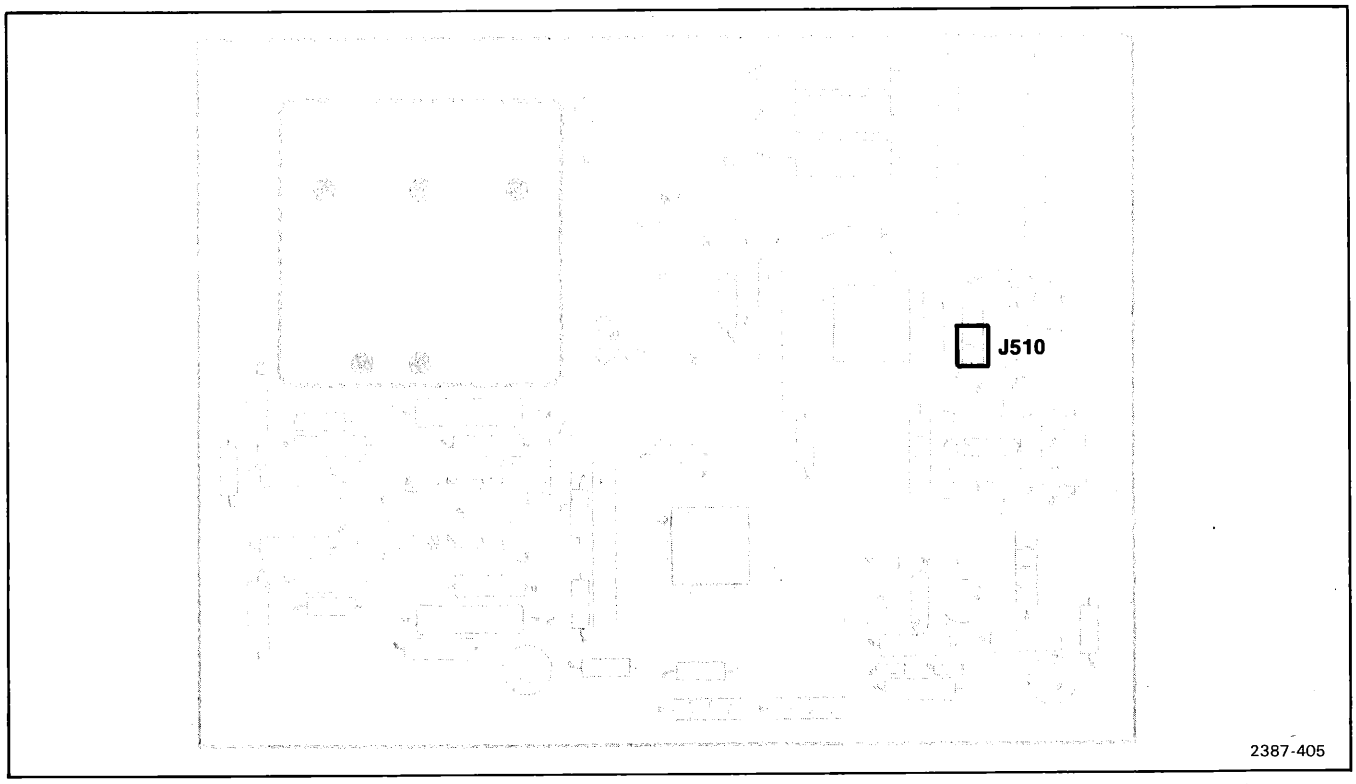


Fig. 4-7. Normal position of jumper J510 on Clock Buffer Board (A12).

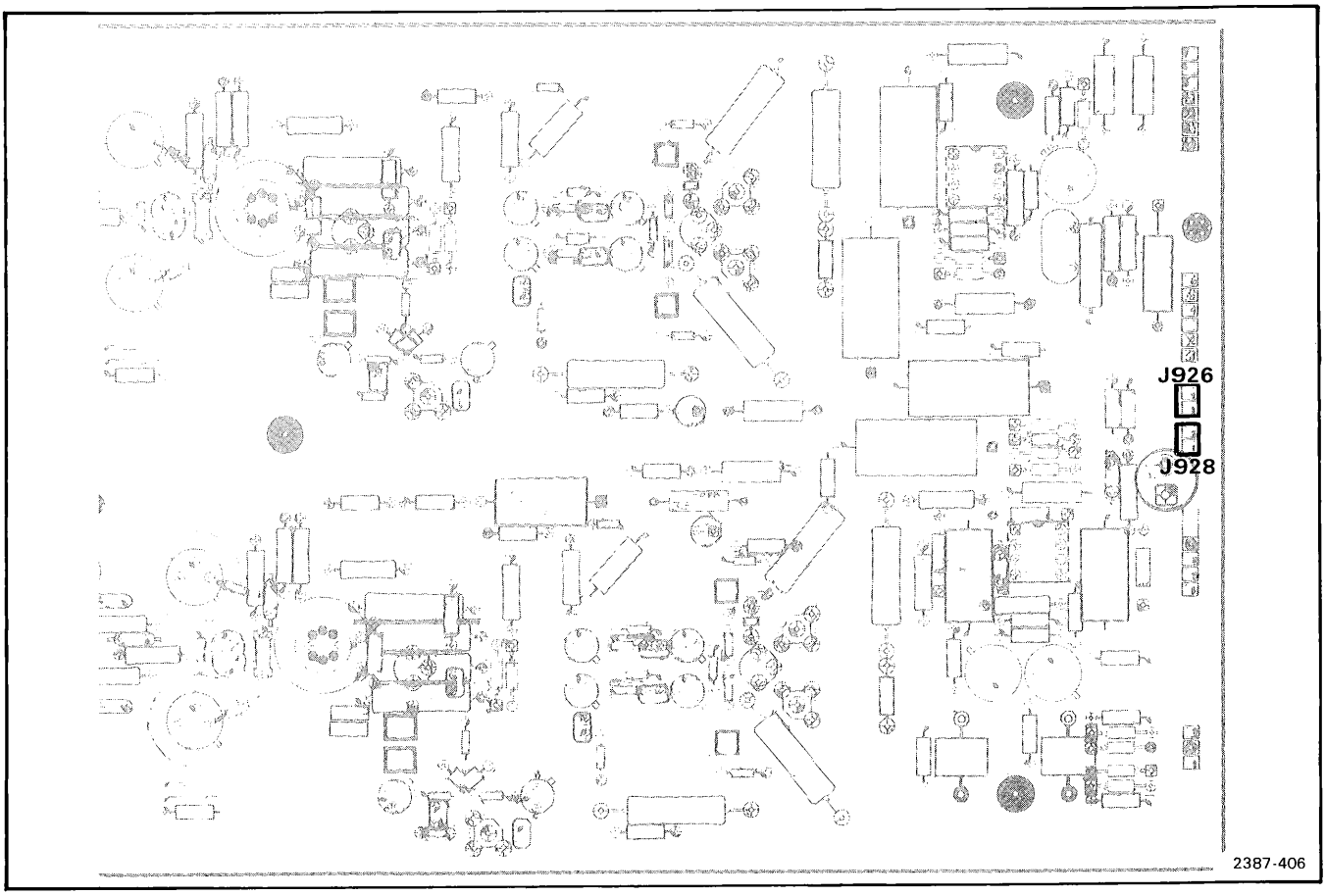


Fig. 4-8. Normal positions of jumpers J926 and J928 on Deflection Amplifier Board (A26).

IEEE 488 INTERFACE (A56)

J030 provides blanking of the XYZ display at upper and lower limits when set in the normal position as shown in Figure 4-9. J300 selects the XYZ display when set in the normal position (connecting pins 1 and 2) as shown in Figure 4-10. Install J300 on pins 2 and 3 to display an address map of the 6800 system on the XYZ monitor for diagnostic purposes.

Always install J602 between pins 1 and 2.

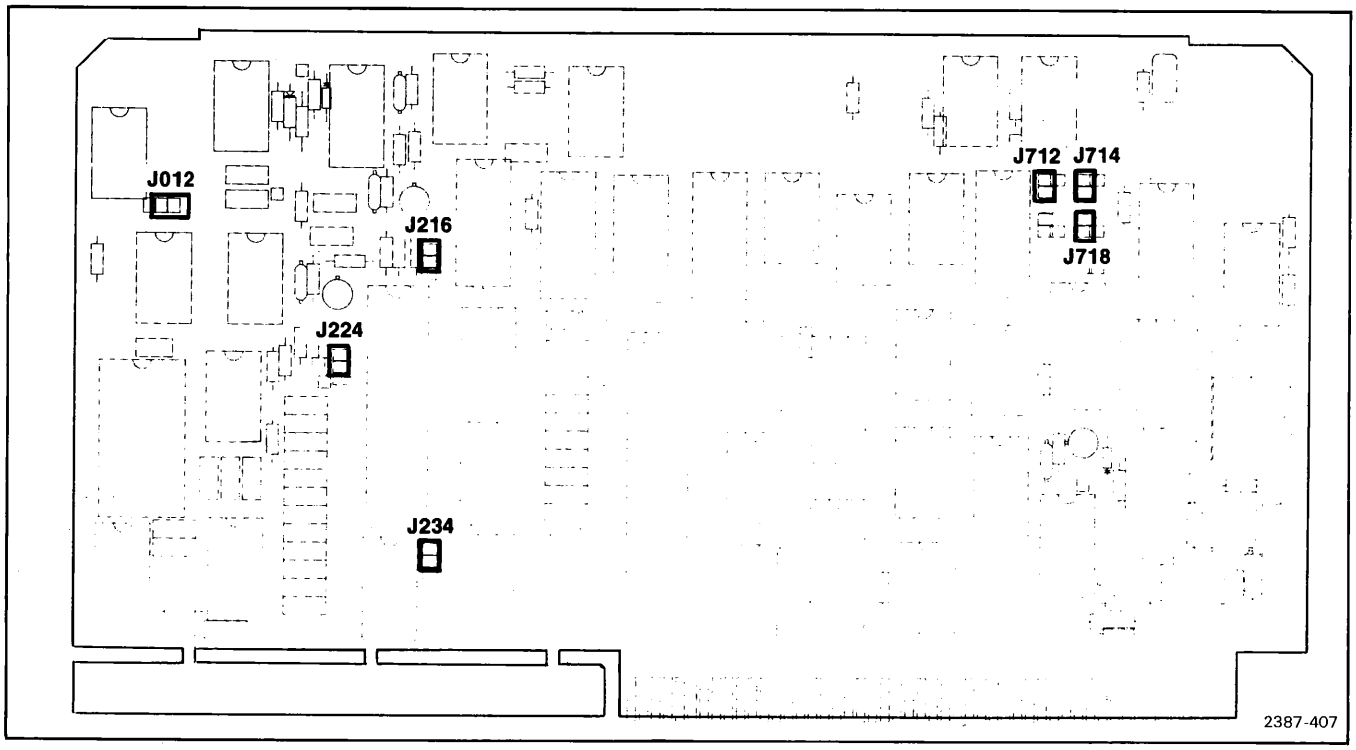


Fig. 4-9. Normal positions of jumpers J012, J216, J224, J234, J712, J714, and J718 on MPU Board (A54).

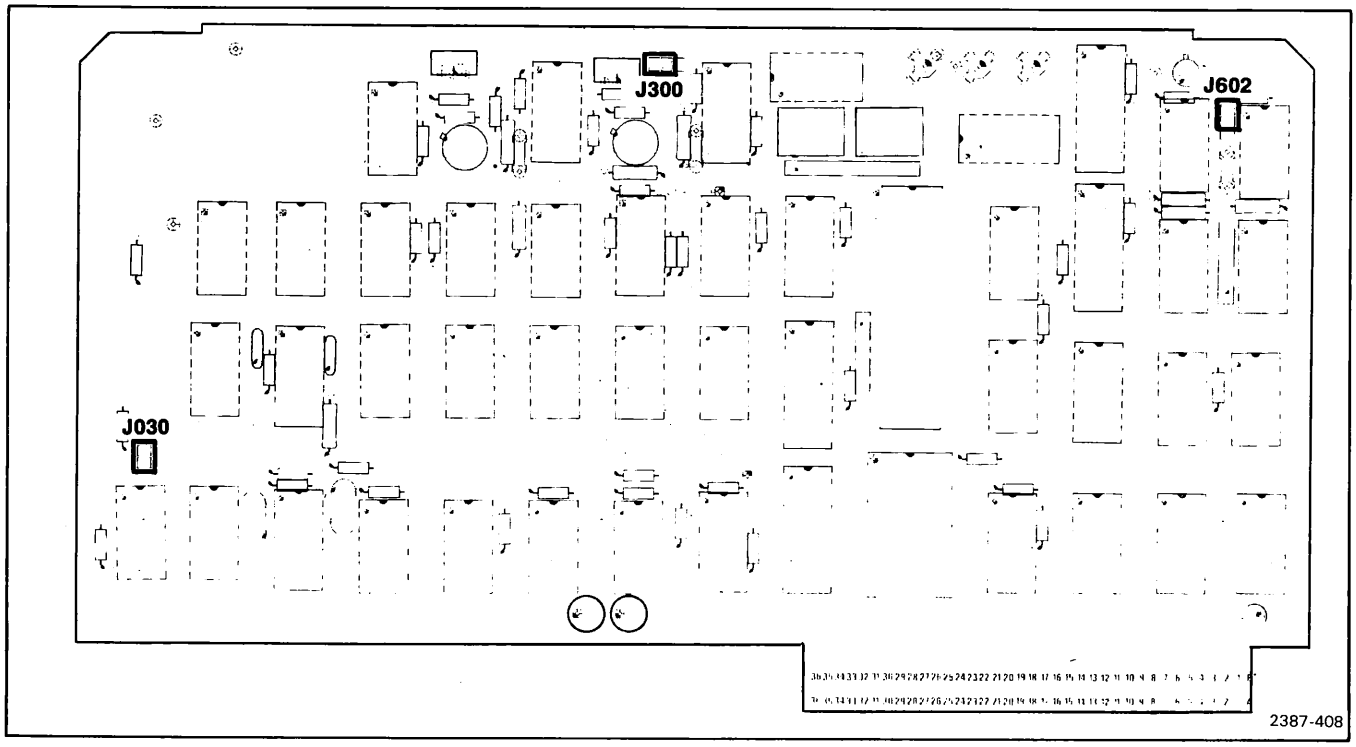


Fig. 4-10. Normal positions of jumpers J030, J300, and J602 on IEEE 488 Interface Board (A56).

PREVENTIVE MAINTENANCE

Preventive maintenance, consisting of cleaning, visual inspection, etc., performed on a regular basis, will improve the reliability of this instrument. Periodic checks of the semiconductor devices used in the 7612D are not recommended. See semiconductor-checking information given under Troubleshooting.

The severity of the environment to which this instrument is subjected determines the frequency of maintenance. A convenient time to perform preventive maintenance is preceding adjustment of the instrument.

VISUAL INSPECTION

The 7612D should be inspected occasionally for such defects as broken connections, improperly seated semiconductors, damaged circuit boards, and heat-damaged parts.

The corrective procedure for most visible defects is obvious. However, particular care must be taken if heat-damage components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

CLEANING

WARNING

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue cleaner, preferably isopropyl alcohol or a 20:1 solution of water and Kelite to wash the circuit boards. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

EXTERIOR

Loose dust may be removed with a soft cloth or a dry brush. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

INTERIOR

Dust on the interior of the unit should be removed occasionally because it is electrically conductive under high-humidity conditions. Cleaning the interior of the unit should precede calibration adjustments. Use low-velocity compressed air to blow off the accumulated dust. Hardened dirt can be removed with a soft, dry brush, cotton-tipped swab, or cloth dampend with a mild detergent and water solution.

LUBRICATION

There are no components in the 7612D that require regular lubrication.

SEMICONDUCTOR CHECKS

Periodic checks of the semiconductors in this instrument are not recommended. The best check of semiconductor performance is actual operation in the instrument. More details on checking semiconductor operation are given under Troubleshooting.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of other closely related circuits. The Performance Check procedure in this manual provides a quick and convenient means of checking instrument operation. In some cases, minor troubles may be revealed or corrected by adjustment.

ELECTRICAL ADJUSTMENT

To ensure accurate measurements, check the electrical adjustment of this instrument after each 1000 hours of operation, or every six months if used infrequently. In addition, replacement of components may necessitate adjustment of the affected circuits. Complete adjustment instructions are given in Section 5, Calibration. This procedure can be helpful in localizing certain troubles in the instrument, and in some cases, may correct them.

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting the 7612D. Information in other sections of this manual should be used in conjunction with the following data to aid in locating a defective component. An understanding of the circuit operation is helpful in locating troubles. See Section 3, Theory of Operation, for this information.

TROUBLESHOOTING AIDS

SCHEMATIC DIAGRAMS

Schematic diagrams are provided on foldout pages in section 8. The circuit number and electrical value of each component are shown on the diagrams. Power supply voltages are also shown. Components that are mounted on circuit boards are enclosed on the diagrams with a heavy black line.

CIRCUIT-BOARD ILLUSTRATIONS

Illustrations of circuit boards are shown opposite the schematic diagrams. Each board-mounted electrical component is identified by its circuit number.

MAIN INTERCONNECT (A68) CONNECTORS DIAGRAM

Figure 8-32 in the Diagrams and Circuit-Board Illustrations section, shows the pinout of the connectors on the Main Interconnect board. A table also lists all the signals routed through the Main Interconnect Board and their connections in alphabetical order.

COMPONENT-LOCATOR GRIDS

The schematic diagrams and circuit-board illustrations have component-locator grids. When used with the associated tables, these grids allow you to quickly locate a component on either the schematic or the circuit board.

COMPONENT AND WRITING COLOR CODE

Colored stripes or dots on resistors and capacitors signify electrical values, tolerances, etc., according to the EIA standard color code. Components not color coded usually have the value printed on the body.

The insulated wires used for interconnection in the 7612D are color coded to facilitate tracing wires from one point to another.

SEMICONDUCTOR LEAD CONFIGURATION

The lead configurations of the semiconductor devices used in this instrument are shown in Figure 4-11.

STATIC-SENSITIVE DEVICES

WARNING

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 4-2 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Table 4-2
RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes		Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs.	(Most Sensitive)	1
ECL		2
Schottky signal diodes		3
Schottky TTL		4
High-frequency bipolar transistors		5
JFETs		6
Linear microcircuits		7
Low-power Schottky TTL		8
TTL	(Least Sensitive)	9

[a]Voltage equivalent for levels:

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V(est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.

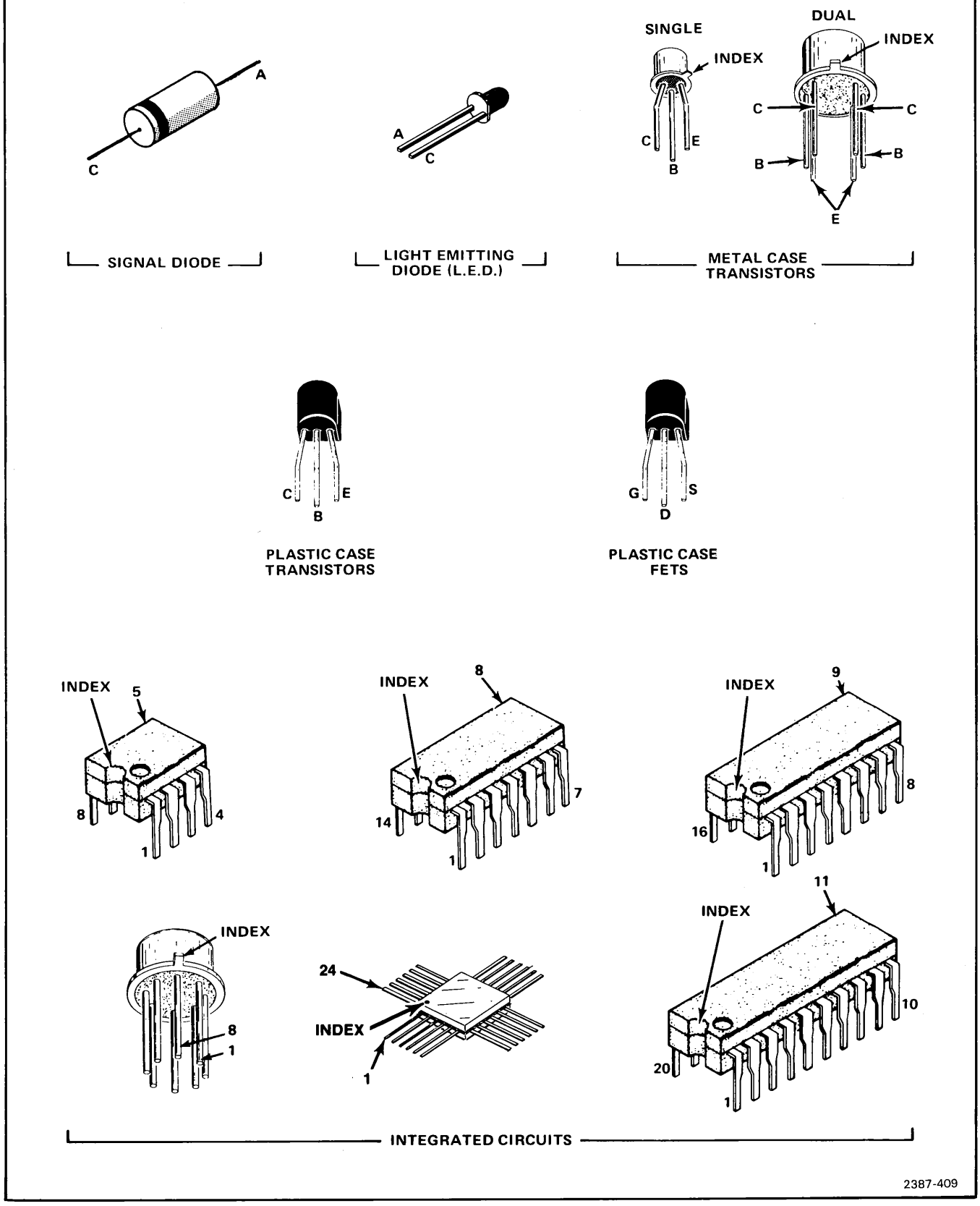


Fig. 4-11. Semiconductor lead configurations.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special antistatic suction-type desoldering tools.

MULTI-PIN CONNECTOR HOLDERS

The multi-pin connector holders are keyed with two triangles, one on the holder and one on the circuit board.

The two triangles identify pin 1 of the holder and the row of pins. When connecting a holder to its row of pins, orient the holder so that triangles align (see Fig. 4-12).

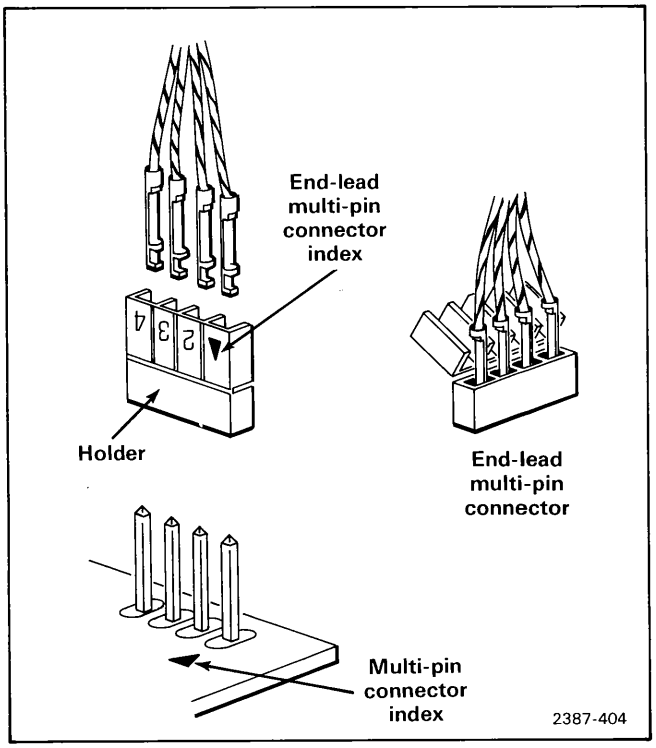


Fig. 4-12. Orientation of multi-pin connector holders.

TROUBLESHOOTING EQUIPMENT

The following equipment is useful for troubleshooting the 7612D.

1. SEMICONDUCTOR TESTER

Some means of testing the transistors, operational amplifiers, comparators, diodes, and FETs used in this instrument is helpful. A transistor-curve tracer such as the Tektronix Type 577/177 or 577/178 will give the most complete information.

2. MULTIMETER

A voltmeter is required for checking voltages within the circuits, and an ohmmeter for checking resistors and diodes. The voltmeter should have an input impedance of at least 10 MΩ, a range of at least 0 to 130 volts dc, and an accuracy of 0.1%. The ohmmeter should have a range of 0 to 20 MΩ.

3. TEST OSCILLOSCOPE

A test oscilloscope (with dc to 200 MHz bandwidth) is required to view waveforms at different points in the circuits. A Tektronix 7000-series oscilloscope equipped with a readout system, 7D13A Digital Multimeter, 7B-series time-base, and a 7A-series amplifier with a 10X probe will meet the needs of items 2 and 3.

4. 7612D CALIBRATION KIT

The Gray Code Ramp Generator in this kit is an invaluable aid for determining if a fault lies in the 7612D data memory or in the hybrid comparators, etc.

Extender boards and cables are also provided for accessing the 7612D plug-in boards during troubleshooting.

5. LOGIC ANALYZER

A logic analyzer such as the TEKTRONIX 7D01 Logic Analyzer is required to view many of the digital signals in the 6800 system. The TEKTRONIX DF2 Display Formatter enhances the 7D01's usefulness in troubleshooting IEEE 488 interface and bus problems.

7612D CHECKOUT SOFTWARE

Checkout software for the 7612D is available as an aid to troubleshoot the instrument. The software is provided in two versions—one designed to run under TEK SPS BASIC and one for 4050-series BASIC. Provided that the instrument is capable of communicating over the IEEE 488 bus, the software provides go/no-go testing of the command set used during normal operation of the 7612D. It is not intended to diagnose problems down to the chip level. When a fault is detected, an error message is printed to provide service personnel the maximum amount of information concerning the fault.

For a complete checkout, the software requires the use of programmable plug-in units in the 7612D. Refer to the checkout software manual, Tektronix Part 070-3466-00, for more information.

DIAGNOSING POWER-UP PROBLEMS

If jumper J718 on the MPU Board (A54) is in its normal position, a power-up error will cause the 7612D to stop and display an error message. Table 2-11, Internal Error Messages (Section 2, Operating and Programming), lists the possible messages and the errors that cause them.

Three of the error messages contain information, in their zero bits, about the error. To ascertain the information from the zero bit, use the diagnostic command FET H0. The responses to the FET H0 command for the following messages mean:

301	address of misplaced EPROM
302	address of bad RAM byte
304	last address of bad EPROM

If jumper J718 is set to the "continue" position the 7612D will not stop when it senses a power-up problem. For details, refer to the MPU(A54) discussion under Selecting Internal Jumpers in this section.

TROUBLESHOOTING TECHNIQUES

This troubleshooting procedure checks the simple trouble sources before proceeding with extensive troubleshooting. The first few checks ensure proper connection, operation, and adjustment. If the trouble is not located by these checks, the remaining steps aid in locating the component. When the defective component is located, it should be replaced using the replacement procedure given under Corrective Maintenance.

1. CHECK CONTROL SETTINGS

An incorrect setting of the 7612D controls can indicate a problem that does not exist. If there is any question about the correct function or operation of a control or front-panel connector, refer to the front-panel operating instructions and programming information provided in section 2.

2. CHECK ASSOCIATED EQUIPMENT

Before proceeding with troubleshooting, check that the other equipment used is operating correctly. If possible, substitute known good equipment for any equipment in question, and see if the problem persists. Check that any interconnecting cables are not defective.

3. VISUAL CHECK

Visually check the portion of the instrument in which the trouble is suspected. Many problems can be located by visual indications such as unsoldered connections, broken wires, damaged circuit boards, damaged components, or components bent
over and touching other parts or circuit board runs.

4. CHECK INSTRUMENT ADJUSTMENT

Check the adjustment of the unit or the affected circuit by performing the Calibration Procedure in Section 5. The apparent trouble may only be a result of mis-adjustment and may be corrected by calibration.

5. ISOLATE TROUBLE TO A CIRCUIT

To isolate trouble to a circuit, note the trouble symptom. The symptom often identifies the circuit in which the trouble is located. When trouble symptoms appear in more than one circuit, check the affected circuits by taking voltage readings. Incorrect operation of all circuits sometimes indicates trouble in the power supply.

If the power supply is suspected to be defective, connect the 7612D to a variable autotransformer. Then check each output voltage for correct regulation with a dc voltmeter (0.1% accuracy), and for correct ripple with an oscilloscope, while varying the input voltage through the regulating range (90-132 V_{ac} or 180-250 V_{ac}, see rear panel). Table 4-3 lists the test points, voltage tolerances, and typical ripple voltage for each output voltage.

The voltages and ripples listed in Table 4-3 were measured with a 7704A Oscilloscope that contained a 7B80 Time Base, a 7A22 Differential Amplifier with its HF −3 dB Point set to .1 MHz and its LF −3 dB Point set to DC, and used a P6106 Probe. When checking voltages on P100 the probe was grounded to the minus terminal of C300, the capacitor next to P100 on the Plug-In Interface Board. When checking the +5.1 V, −2 V, and −5.2 V, the probe was grounded to the COM Terminal on the Power Supply. After the defective circuit has been located, proceed with step 6 to locate the defective components.

TABLE 4-3
Power Supply Tolerances and Ripple Voltages

Power Supply	Test Point	Tolerance	Typical Ripple (peak-to-peak)
+130 V	P100 A22	+128.7 to 131.3	5 mV
+ 50 V	P100 A11	+49.75 to 50.25	5 mV
+ 15 V	P100 A12	+14.91 to +15.09	3 mV
+ 5.0 V	P100 A13	+4.95 to +5.05	3 mV
− 15 V	P100 A16	−14.955 to −15.045	3 mV
− 50 V	P100 A17	−49.95 to −50.05	4 mV
+5.1 V	+5.1 V Terminal	+5.0 to +5.2	50 mV
−2.0 V	−2.0 V on Power	+1.96 to +2.04	20 mV
−5.2 V	−5.2 V Supply	+5.195 to +5.205	10 mV

6. CHECK INDIVIDUAL COMPONENTS

The following methods are provided for checking the individual components. Components which are soldered in place are best checked by disconnecting one end to isolate the measurement from the effects of surrounding circuitry.

CAUTION

To avoid component damage, disconnect the power source before removing or replacing semiconductors.

NOTE

To locate intermittent or temperature sensitive components mounted on the circuit boards, Quick Freeze (Miller Stephenson, MS-240, Tektronix Part 006-0173-01) is recommended. Dry ice or dichloro-difluoromethane (Freon 11, or 12) may also be used.

TRANSISTORS

The best check of transistor operation is actual performance under operating conditions. Transistors that are soldered to the circuit board should first be checked in-circuit using a dynamic transistor tester; then a replacement can be substituted to further verify that the old transistor is bad. Socketed transistors can be checked immediately by substituting a known good component; however, be sure that circuit conditions are not such that a replacement might also be damaged. If substitute transistors are not available, check the old transistor out-of-circuit using a dynamic tester (such as the Tektronix Type 577/177). Static-type testers may be used, but because they do not check operation under simulated operating conditions, some defects may go unnoticed. Be sure the power is off before attempting to remove or replace any transistor.

INTEGRATED CIRCUITS

Analog ICs, such as comparators and operational amplifiers, can usually be checked in-circuit with a voltmeter or test oscilloscope. An understanding of the device and circuit operation is essential for this type of troubleshooting. (For example, an op-amp can be tested by measuring the input and output circuit voltages and comparing this ratio to the ratio of input and feedback resistors.) Analog ICs that are socketed can also be checked out-of-circuit using a dynamic tester such as the Tektronix 577/178.

Digital ICs are best checked in-circuit using a logic probe or voltmeter. Use care when checking voltages and waveforms around DIP (Dual-In-Line-Package) ICs so that adjacent leads are not shorted together. A convenient means of connecting a test probe to 14- and 16-pin ICs is with an IC test clip. This device also doubles as an extraction tool.

DIODES

A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter set to the R × 1k scale. The diode resistance should be very high in one direction and very low when the meter leads are reversed. A diode can also be tested with a dynamic tester (transistor curve tracer).

CAUTION

Do not use an ohmmeter scale that has a high internal current. High currents may damage the diodes under test.

RESISTORS

Check resistors with an ohmmeter. Resistor tolerance is given in the replaceable electrical parts list. Resistors normally do not need to be replaced unless the measured value varies widely from the specified value.

CAPACITORS

A leaky or shorted capacitor can be detected by checking resistance with an ohmmeter on the highest scale. Use an ohmmeter that will not exceed the voltage rating of the capacitor. (Be careful to observe correct polarity when checking electrolytic capacitors.) The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter, or by checking whether the capacitor passes ac signals.

REPAIR AND READJUST THE CIRCUIT

Replace the defective component or assembly. Be sure to check the performance of any circuit that has been repaired or that has had any electrical components replaced. Recalibration of the affected circuit may be necessary.

Corrective maintenance consists of component replacement and instrument repair. Special techniques required to replace components and assemblies are given here.

CORRECTIVE MAINTENANCE

OBTAINING REPLACEMENT PARTS

STANDARD PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix field office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source. Before you purchase a part from a source other than Tektronix, check the electrical parts list for the proper value, rating, tolerance, and description.

Order all special parts directly from your local Tektronix Field Office or representative.

ORDERING PARTS

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument Type.
2. Instrument Serial Number.
3. A description of the part (if electrical, include the full component number found in the Replaceable Electrical Parts list—section 8).
4. Tektronix Part Number.

SOLDERING TECHNIQUES

WARNING

Disconnect the instrument from the power source before soldering.

CIRCUIT BOARDS

The components mounted on the circuit boards can be replaced using normal circuit-board soldering techniques. Remember the following points when soldering on the circuit boards:

1. Use a pencil-type soldering iron with a wattage rating from 15 to 50 watts.
2. Apply heat from the soldering iron to the junction between the component and the circuit board.
3. Heat-shunt the lead to the component by using a pair of long-nose pliers.
4. Avoid excessive heating near the circuit board, as this could separate the circuit board wiring from the base material.
5. Use only 60-40 rosin core, electronic grade solder.
6. Clip off any excess lead length extending beyond the circuit board. Clean off any residual flux with a flux-removing solvent.

METAL TERMINALS

When soldering metal terminals use 60-40 tin-lead solder and a 15 to 50 watt soldering iron. Observe the following precautions when soldering metal terminals:

1. Apply only enough heat to make the solder flow freely.
2. Apply only enough solder to form a solid connection. Excess solder may impair the function of the part.
3. If a wire extends beyond the solder joint, clip off the excess.
4. Clean the flux from the solder joint with a flux-removing solvent.

POWER SUPPLY

Use only silver solder on the ceramic plate terminal ends of the black leads coming from the Line board (A80). There is a ceramic plate under each transistor pair Q011-Q012, and Q31-Q41 mounted on brackets below the front edge of the Line board.

MICROPROCESSOR OPERATING SYSTEM FIRMWARE

Operating systems for the 6800 MPU are contained in firmware. To determine which operating system is installed, query the 7612D with the ID? command. The response ends with FXX.YY where XX is the 6800 MPU firmware version number. The PROM locations are shown in Figure 4-13. The value of the XX suffix shown on the part numbers may vary with the version number.

6800 VERSION 1

The following part-numbered PROMs contain the 6800 MPU operating system, Version 1:

MPU MEMORY (A52)	U011	160-0456-01
	U013	160-0457-01
	U021	160-0455-01
	U031	160-0454-01
	U111	160-0452-01
	U211	160-0453-01
	U213	160-0450-01
	U221	160-0451-01
	U231	160-0448-01
	U401	160-0449-01
	U607	160-0447-01

TIME BASE BOARD (A20)

If CR702 is installed on the Time Base board in your instrument (see Fig. 8-11 in the diagrams section), then manufacturer's part number 10016 applies to the following ICs. If CR702 is not installed, use 10010 for the following ICs (also see area G1 of diagram 9):

Use 10016 (156-1038-XX) with CR702	U606 U616 U626 U700 U710 U720 U730	Use 10010 (156-0870-XX) without CR702

REMOVING AND REPLACING PARTS

POWER SUPPLY

How to Remove the Power Supply

1. Turn off the PRINCIPAL POWER SWITCH on the rear panel.
2. Disconnect the power cord.
3. Set the 7612D on its right side and remove the bottom and left side covers.
4. Remove six nuts from the power supply bottom terminal posts and disconnect leads.
5. Disconnect ribbon cable connector from J500 on the Main Interconnect board (A68).

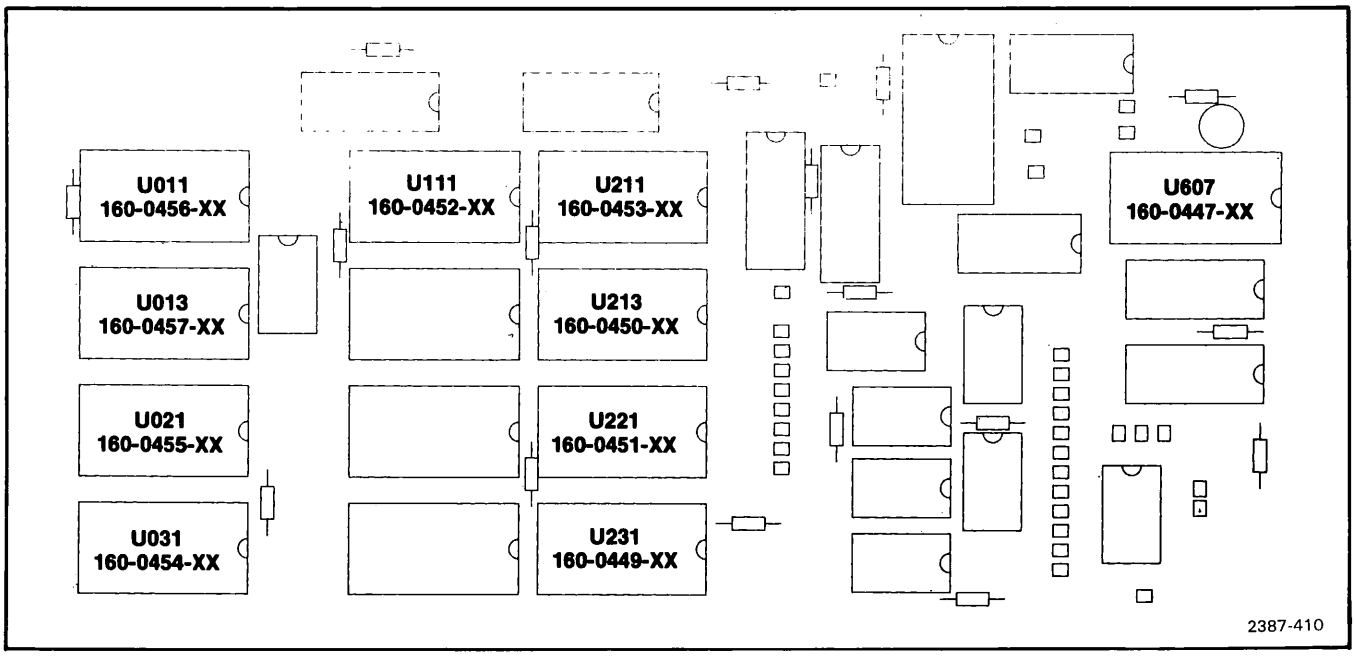


Fig. 4-13. Location of PROMs in the 6800 operating system.

6. Remove two screws from the side ribbon cable clamp on the power supply and remove clamp sections.

7. Remove ribbon cable connector P420.

8. Remove four screws at the corners of the power supply rear panel.

9. Slide the power supply out of the instrument chassis.

CAUTION

Allow several minutes for the input filter capacitors to discharge before removing the power supply covers.

How to Replace the Power Supply

1. Check that the PRINCIPAL POWER SWITCH is off.

2. Check that the power cord is disconnected.

3. The power supply loads may be checked for proper resistances before installing the power supply. Use a Triplett Model 630-NA or equivalent. Remove the plug-in units from the 7612D. Test points on the Main Interconnect board (A68) are shown in Figure 8-32 in the diagrams section. Connect the VOM to the points indicated in Table 4-4. The measurements in the Reverse column can be made by changing the ACV ± switch on the Triplett 630-NA to (−) . P420 connections are on the power supply end of the large ribbon cable connected to the Plug-In Interface board (A46). The J500, COM, −5.2 V, +5.1 V, and −2 V test points are located on the Main Interconnect board.

TABLE 4-4
Power Supply Load Resistances

Power Supply	Meter Range	Meter Leads		Approximate Reading	
		COM—	V-Ω-A	Normal	Reverse
−5.2 V	10X	COM	−5.2 V	16 Ω	30 Ω
+5.1 V	10X	COM	+5.1 V	14 Ω	16 Ω
−2 V	10X	COM	−2 V	26 Ω	26 Ω
PON	10X	COM	Pin 1, J500	90 Ω	42 Ω
HWF	10X k	COM	Pin 3, J500	85 kΩ	60 Ω (10X)
−5.2 SENS	10X	COM	Pin 4, J500	16 Ω	30 Ω
COM SENS	10X	COM	Pin 5, J500	0 Ω	0 Ω
−2 SENS	10X	COM	Pin 6, J500	26 Ω	26 Ω
	10X	COM	Pin 7, J500	open	open
	10X	COM	Pin 8, J500	open	open
+5.1 SENS	10X	COM	Pin 9, J500	14 Ω	16 Ω
		Top of C500 on Plug-In Interface Board			
GND SENS	10X	(A46)	A1, P420	0 Ω	0 Ω
"	"	"	A2, P420	0 Ω	0 Ω
"	"	"	A3, P420	0 Ω	0 Ω
"	"	"	A4, P420	0 Ω	0 Ω
"	"	"	A5, P420	0 Ω	0 Ω
"	"	"	A6, P420	0 Ω	0 Ω
"	"	"	A7, P420	0 Ω	0 Ω
"	"	"	A8, P420	0 Ω	0 Ω
"	"	"	A9, P420	0 Ω	0 Ω

TABLE 4-4 (cont)

Power Supply	Meter Range	Meter Leads		Approximate Reading	
		COM—	V-Ω-A	Normal	Reverse
"	"	"	A10, P420	0 Ω	0 Ω
+50 V	X1 k	"	A11, P420	9 kΩ	3.75 Ω
+15 V	10X	"	A12, P420	65 Ω	48 Ω
+5 V	10X	"	A13, P420	52 Ω	30 Ω
+5 V	10X	"	A14, P420	52 Ω	30 Ω
	10X	"	A15, P420	open	open
−15 V	10X	"	A16, P420	35 Ω	12 Ω
−50 V	X1 k	"	A17, P420	9 kΩ	3.7 kΩ
GND SENS	10X	"	A18, P420	0 Ω	0 Ω
	10X	"	A20, P420	open	open
+130 V	10X k	"	A22, P420	11 kΩ	5 kΩ
GND SENS	10X	"	B1, P420	0 Ω	0 Ω
GND SENS	10X	"	B1, P420	0 Ω	0 Ω
+50 VSENS	10X	"	B3, P420	38 Ω	48 Ω
+15 VSENS	10X	"	B4, P420	0 Ω	0 Ω
+5 VSENS	10X	"	B5, P420	50 Ω	30 Ω
GND SENS	10X	"	B6, P420	0 Ω	0 Ω
−15 VSENS	10X	"	B7, P420	35 Ω	110 Ω
−50 VSENS	X1 k	"	B8, P420	9 kΩ	3.7 kΩ
GND SENS	10X	"	B9, P420	0 Ω	0 Ω
GND SENS	10X	"	B10, P420	0 Ω	0 Ω
+50 V	10X	"	B11, P420	9 kΩ	3.7 kΩ
+15 V	10X	"	B12, P420	65 Ω	48 Ω
+5 V	10X	"	B13, P420	52 Ω	30 Ω
+5 V	10X	"	B14, P420	52 Ω	30 Ω
	10X	"	B15, P420	open	open
−15 V	10X	"	B16, P420	35 Ω	12 Ω
−50 V	X1 k	"	B17, P420	9 kΩ	3.7 kΩ
GND SENS	10X	"	B18, P420	0 Ω	0 Ω
	10X	"	B20, P420	open	open
+130 V	10X k	"	B22, P420	11 kΩ	5 kΩ

4. Insert the power supply into the 7612D chassis.

5. Connect the ribbon cable to J500 on the Main Interconnect board (A68).

6. Connect P420 to the connector on the side of the power supply. Install cable clamp sections and secure with two nuts.

7. Connect six leads to terminal posts on the bottom of the power supply in the same order as they were removed and secure with six nuts.

8. Reinstall four screws at the corners of the power-supply rear panel.

9. Connect the power cord.

10. Turn on the PRINCIPAL POWER SWITCH.

How to Remove the Power-Supply Rectifier Board

NOTE

The numbers in parentheses are index numbers from Figure 9-6, Power Supply, in the Replaceable Mechanical Parts section.

1. Set the Power Supply on its rear panel with the cover (6) facing up.

2. Remove the seven screws that fasten the cover to the Power Supply.

3. Lift the cover off the Power Supply. (Guide the two cable assemblies to prevent scratching them against edges of the Cover.)

4. Working through the access holes in the Control Board, remove the two screws that fasten the Control Board chassis (36) to the Line Power Board chassis.

5. Disconnect P020 and P060 from the back of the Control Board.

6. Remove the angle bracket (144) that is attached to the rear panel (146) next to the Control Board chassis.

7. Remove the two screws that fasten the Control Board chassis to the rear panel.

8. Remove the two flat-head screws that fasten the Control Board chassis to the Rectifier Board chassis.

9. Carefully pull the Control Board assembly directly out from the Power Supply to disconnect P040 where it connects to the Rectifier Board. Set the Control Board assembly aside.

10. Remove the seven flat-head screws that fasten the Rectifier Board chassis to the Rectifier Board.

11. Remove the two flat-head screws that fasten the Rectifier Board chassis to the Regulator Board chassis (19).

12. Remove the Rectifier Board chassis (55).

13. Remove the two screws that fasten the Rectifier Board to the two spacers.

14. Pull the Rectifier Board directly away from the Regulator Board to disconnect J450. You can swing the board outward slightly to clear the fan.

15. Disconnect P124 from J124 on the Line Power Board.

How to Install the Power-Supply Rectifier Board

1. Connect P124 to J124 on the Line Power Board.

2. Carefully position the Rectifier Board to align J450 with the pins of J450 on the Regulator Board.

3. Move the Rectifier Board toward the Regulator Board to fully engage J450.

4. Install the two screws that fasten the Rectifier Board to the spacers.

5. Attach the chassis (55) to the Rectifier Board with seven flat-head screws.

6. Fasten the Rectifier Board chassis (55) to the Regulator Board chassis (19) with two flat-head screws.

7. Position the Control Board assembly so that the pins of J040 align with J040 on the Rectifier Board, then move the Control Board assembly toward the Rectifier Board to fully engage J040.

8. Fasten the Control Board chassis (36) to the Rectifier Board chassis (55) with two flat-head screws.

9. Fasten the Control Board chassis (36) to the Rear Panel (146) with two screws.

10. Working through the access holes in the Control Board, fasten the Control Board chassis to the Line Power chassis (57) with two screws.

11. Install the angle bracket (144) on the Rear Panel with two screws.

12. Connect P020 and P060 from the Line Power Board to P020 and P060, respectively, on the Control Board.

13. Lower the Cover onto the Power Supply, and guide the two cable assemblies as follows:

    a. The eight-wire assembly should come out the back of the Cover because it will connect to J500 on the Main Interconnect Board.

    b. The green-yellow chassis-ground lead should be routed through the hole near the Regulator Board.

14. Fasten the Cover to the Power Supply with seven screws—four on the rear and three around the edges.

HIGH-VOLTAGE OSCILLATOR ASSEMBLY (A76)

How to Remove the HV Oscillator Assembly

1. Disconnect the power cord.

WARNING

Be certain power to the instrument is removed before proceeding.

2. Place the instrument on its left side.

3. Remove the top and right side covers.

4. Disconnect four cables from the rear edge of the Deflection Amplifier Board (A26).

5. Disconnect the crt HV cables from the HV Oscillator Assembly sockets marked A (UPPER CRT) and B (LOWER CRT).

6. Remove screws and square washers from the three cable clamp assemblies holding wiring harnesses to the top of the HV Oscillator Assembly.

7. Remove four screws from rear-panel corners of the HV Oscillator Asembly. Slide the assembly 1/2-inch out of the mainframe.

8. Remove screw and nut holding the bracket between the crt sockets and the HV Oscillator Assembly. Remove the bracket.

9. Slide the HV Oscillator Assembly out as far as the cables will allow.

10. Disconnect the crt socket connectors and eight coaxial cables from inside the rear panel of the assembly. Remove the HV Oscillator Assembly.

11. Remove four screws from the rear panel and remove the rear panel from the HV Oscillator Assembly.

How to Replace the HV Oscillator Assembly

1. Attach rear panel to HV Oscillator Assembly with four screws.

2. Install the assembly in the mainframe and slide forward until the eight coaxial cables are within reach of the rear-panel connectors.

3. Connect the coaxial cables to the rear-panel connectors.

4. Connect the crt socket connectors to the crt sockets.

5. Install bracket in place with screw and nut.

6. Slide HV Oscillator Assembly into place and install the four screws in the corners of the rear panel.

7. Secure the three cable clamp assemblies to the top of the HV Oscillator Assembly with screws and square washers.

8. Connect the crt HV cables to the HV Oscillator Assembly socket marked A (UPPER CRT) and B (LOWER CRT).

9. Connect the four cables from the HV Oscillator Assembly to the rear edge connectors of the Deflection Amplifier board.

10. Replace the right side and top covers.

ELECTRON-BOMBARDED SEMICONDUCTOR (EBS) TUBE(S)

How to Remove the EBS Tube(s)

1. Disconnect the ac power cord at the rear of the instrument.

WARNING

Be certain power to the instrument is disconnected before proceeding.

2. Set the 7612D on its left side. Remove the top, right-side, and bottom covers.

3. Remove the two screws holding the bottom of the rectangular crt shield housing to the bottom of the instrument.

4. Set the instrument in its normal horizontal operating position.

5. Remove four screws that hold the top shield plate to the mainframe chassis rails.

6. Remove two flat-head and two round-head screws holding plate to shield housing and lift plate off instrument to expose top of crt shield housing.

7. Remove eight screws from front panel and tilt front panel forward.

8. Disconnect four coaxial cables near center of front panel and lay the front panel down flat on its face.

9. Disconnect wires and cables connected to the Deflection Amplifier board (A26); the board is shown in Figure 8-12 in the Diagrams section. Be sure to disconnect six wires in the center of the board before removing the board. Remove eight nuts from board and remove board by pulling outward until it is clear of shield studs. Lift up until bottom of board is clear of chassis and remove. Use care to avoid bending the crt terminal board pins behind the board when removing the board.

10. Disconnect wires and cables connected to the Header Board on the front of the crts. Note their placement for reinstallation later.

11. Disconnect the pair of HV cables from the connectors marked A (UPPER CRT) and B (LOWER CRT) at the rear of the crt assembly.

12. Grasp the front- and rear-upper ends of the crt shield housing and carefully lift the entire crt assembly up and out of the instrument. Use extreme care when lifting the crt assembly to avoid bending the crt terminal prongs that protrude from the side of the shield housing. Lay the crt assembly on its left side on the top of the instrument with the crt base-pin socket connections intact.

13. Disconnect the crt base-pin socket cables and remove the crt assembly from the instrument.

14. Lay the crt assembly with its left side down and the Deflection Amplifier board support studs up.

CAUTION

Use a nonmagnetic screwdriver to remove shield mounting screws and shield fasteners to avoid magnetizing the shield. All shield mounting screws and shield fastener screws are nonmagnetic and should be saved to reinstall the crt assembly.

15. Remove four screws from the shield panel and lift off the panel. Disconnect four leads from side of the crts.

16. Remove two screws holding the crt terminal board bracket in place. Rotate the bracket to the left and remove.

17. Remove two corner brackets that are now loose.

18. Unsolder two black leads connected to ground lug on bracket between the crts.

19. Unsolder pair of leads from the upper (Channel A) crt cable assembly at the terminal lug on the bracket.

NOTE

To remove the channel A (upper) crt assembly only, skip steps 20, 21, 22, and 23.

20. Unsolder pair of leads from the lower (Channel B) crt cable assembly at the opposite solder lug.

21. Remove both pairs of leads from the crt assembly brackets.

22. Remove screws and nut holding terminal strip and ground lug and remove terminal strip.

23. Remove six screws holding lower crt assembly and lift it up and out of the shield housing.

24. Remove six screws holding upper crt assembly and lift assembly up and out of the shield housing.

25. Remove three spacers from each assembly for installation on replacement crt assemblies.

CAUTION

Before attempting to remove the header board assembly observe static-sensitive device precautions; connect a ground strap between your wrist and the rim of the crt to prevent damage to the crt target due to static charge build-up.

26. Remove four nuts holding the header board assembly to the crt base. Grasp header board assembly and pull straight away from crt neck pins.

27. Save the four spacer washers and the gasket.

28. Unsolder ground lead from shield and 100 k ohm resistor and solder lug from header board mounting screw lug.

How to Replace the EBS Tube(s)

1. Check that the ac power is disconnected from the rear of the instrument. The instrument should be on its left side with the top, right, and bottom covers removed.

2. Install the three mounting bracket spacers on the crt assembly; on the rear bracket of the upper assembly (Channel A) and on the front bracket of the lower assembly.

3. Solder the ground lead to the shield in the same position as the original. Solder the 100 k ohm resistor and solder lug assembly to the header board mounting screw lug.

4. Remove the anti-static foam block from the crt neck pins. Note—observe anti-static precautions stated in previous CAUTION.

5. Position the crt assembly so that the cables coming from the shield are pointing up. Install one spacer washer on each mounting stud, and install the metal gasket on the mounting board pins. The tab on the gasket should fit in the hole near the top mounting stud. Carefully align the header board assembly with the crt neck pins; the flat corner index of the black hypcon flange should be aligned with the left (top when mounted in instrument) header board mounting stud. Secure the header board in place with four nuts.

   Remember: **Use only nonmagnetic tools** when installing the crt assembly and shield housing.

6. Grasp the crt assembly at the header board and opposite bracket and carefully position in place within the shield housing.

7. Install three screws in the rear bracket. Install three screws in the front bracket; place the 100 k ohm resistor solder lug behind the upper bracket screw. Tighten all screws securely.

8. Install the terminal strip with ground lug and nylon nut. (Skip this step if installing the Channel A (upper) crt assembly only.)

9. Dress the leads from the crt shields through the unused mounting bracket holes and solder to the ground lug.

10. Dress the pair of crt leads (white with blue trace) through the mounting bracket openings and solder to the terminal strip solder lugs; one pair to each lug.

11. Replace the two corner brackets under each lip of the shield housing.

12. Replace the crt terminal board bracket by sliding under the corner brackets so that the lead connectors are over the crt connections. Secure the bracket with two screws.

13. Reconnect the crt terminal leads to the crt connections.

14. Replace the side panel on the shield housing and secure with four screws. Be sure the crt terminal openings are aligned with the crt terminals before installing the panel. Press the panel inward at the center to obtain a tight fit with the shield housing.

15. Lay the crt assembly on top of the instrument. Remove the crt socket pin protector and reconnect the crt socket cables to the crt sockets.

16. Grasp the front and rear upper ends of the crt shield housing and carefully set the assembly into the instrument. Use extreme care to avoid bending the crt terminal board prongs as the assembly is placed in the instrument.

17. Reconnect the pair of HV cables to the connectors marked A (UPPER CRT) and B (LOWER CRT) at the rear of the crt assembly.

18. Reconnect the wires and cables connected to the Header Boards on the front of the crts.

19. Install the Deflection Amplifier board (A26); Lift the top of the board up behind the upper mainframe rail until the bottom of the board clears the bottom rail and align with the shield housing mounting studs. Use care to avoid bending the crt terminal board prongs behind the board when positioning the board in place.

20. Reconnect the wires and cables to the Deflection Amplifier board and install the eight nuts and washers that hold it in place.

21. Reconnect four coaxial cables near center of front panel in the order that they were connected and position the front panel in place. Secure the front panel with eight screws.

22. Install shield housing plate on top of shield housing with four screws.

23. Install two flat-head and two round-head screws in chassis rails and housing plate. Do not tighten screws.

24. Lift the instrument up to a Vertical position on its left side. Install two screws in the bottom to secure the bottom of the shield housing.

25. Return the instrument to its normal horizontal position and tighten the screws on the top plate.

26. Replacement of the crt(s) will require that the instrument be readjusted. Refer to Section 5, Calibration.

CALIBRATION

This section contains procedures for checking the performance of, and adjusting, the 7612D. These procedures compare the performance of the 7612D with test equipment of certified accuracy to detect, correlate, or eliminate by adjustment, any variation from electrical specification. The procedures also verify that the controls operate correctly.

The Calibration section has two parts. Part I—Performance Check, verifies that the 7612D meets its applicable electrical specifications without making internal adjustments. Part II—Adjustment and Performance Check, is a complete calibration procedure that includes adjustments and performance checks and verifies that the controls operate correctly. The procedures of Parts I and II are written so that the entire instrument or any major circuit or part of a circuit can be checked or adjusted.

CAUTION

Because calibrating the 7612D Programmable Digitizer requires special equipment, we recommend that it be sent to one of the Tektronix Service Centers listed below for calibration when required.

The nonautomatic procedure contained herein has the following shortcomings:

a. It does not check effective number of bits.

b. The tests for aberrations and bandwidth interact, and are difficult to perform.

CALIFORNIA
Irvine 92714
17052 Jamboree Blvd. or
P.O. Box 19523
Irvine, 92713
Phone: (714) 556-8080
(213) 778-5225

Santa Clara 95050
3003 Bunker Hill Lane
Phone: (408) 496-0800

MARYLAND
Rockville 20850
2 Research Court
Phone: (301) 948-7151

MASSACHUSETTS
(Boston)
482 Bedford Street
Lexington 02173
Phone: (617) 861-6800

MICHIGAN
(Detroit)
24155 Drake Road
Farmington 48024
Phone: (313) 478-5200

MINNESOTA
St. Paul 55112
4660 Churchill Rd.
Phone: (612) 484-8571

NEW MEXICO
Albuquerque 87108
1258 Ortiz Drive, S.E.
Phone: (505) 265-5541
Southern N.M. Area: ENterprise 678
Southern Nevada Area: ENterprise 678

Service Centers in most EMC countries and Japan are also able to calibrate the 7612D.

Table 5-1, Calibration Procedure Electives, lists the choices available and gives instruction for performing complete or partial calibration procedures. For more detail, refer to Using These Procedures, which follows.

USING THESE PROCEDURES

NOTE

In these procedures, capital letters within the body of the text identify front-panel controls, indicators, and connectors on the 7612D (e.g., AUTO). Initial capitals identify all the associated test equipment and its controls, indicators, and connectors (e.g., Amplitude) used in the procedures. Initial capitals also identify internal adjustments of the 7612D (e.g., Offset).

These procedures are divided into subsections by major functional circuits (e.g., A. Power Supply, B. High-Voltage Oscillator, etc.). The order in which the subsections and procedures appear is the recommended sequence for a complete performance check or calibration of the instrument.

The first step in each subsection (A1, B1, C1, etc.) contains reference information and control settings that must be performed before proceeding.

The Setup Conditions provide equipment connection information and control settings for both this instrument and any associated test equipment. Also, the setup Conditions are written so that if desired, each subsection (A, B, C, etc.) or step (A2, A3, B2, B3, etc.) can be performed independently.

The terms CHECK, EXAMINE, ADJUST, or INTERACTION when used as the first word of an instruction are defined as follows:

1. **CHECK**—indicates that the instruction accomplishes an electrical specification check. Each electrical specification checked is listed in Table 5-2, Performance Check Summary (see the following Performance Check Summary discussion for more information).

2. **EXAMINE**—usually precedes an ADJUST instruction and indicates that the instruction determines whether adjustment is necessary. If no ADJUST instruction appears in the same step, the EXAMINE instruction concerns measurement limits that have no related adjustment. Measurement limits following the word EXAMINE are not to be interpreted as electrical specifications. They are provided as indicators of a properly functioning instrument and to aid in the adjustment process.

3. **ADJUST**—describes which adjustment to make and the desired result. We recommend that adjustments not be made if a previous CHECK or EXAMINE instruction indicates that no adjustment is necessary.

4. **INTERACTION**—indicates that the adjustment described in the preceding instruction interacts with other circuits. The nature of the interaction is described and reference is made to the step(s) affected.

PERFORMANCE CHECK SUMMARY

Table 5-2, Performance Check Summary, lists the electrical specifications that are checked in Part I and Part II of this section. Table 5-2 is intended to provide a convenient means for locating the procedures in Part I and Part II that check or adjust the instrument to meet the applicable electrical specifications. For example: if the Sweep Generator had been repaired, use Table 5-2 to locate the electrical specifications affected by the repair. Then note the title of the procedure in Part I or Part II in which those specifications are checked and/or adjusted. Use the index provided at the front of Part I and Part II to determine the page number of the desired procedures.

ADJUSTMENT INTERVAL

To maintain instrument accuracy, check performance every 1000 hours of operation, or every 6 months if used infrequently. Before complete adjustment, thoroughly clean and inspect this instrument as outlined in the Maintenance section.

TABLE 5-1
Calibration Procedure Electives

Electives	Procedures
Function Check	A functional check is accomplished by performing Part II—Adjustment and Performance Check.
Performance Check Only	Perform Part I—Performance Check.
Complete Calibration	Perform Part II—Adjustment and Performance Check.
Partial Procedures	Proceed to the desired step(s) (e.g., A2, A3, B2, B3, etc., as listed in the Index to Part I—Performance Check or Index to Part II—Adjustment and Performance Check). **NOTE** *When adjustments are made we recommend that the entire major functional circuit procedure be performed.*

TABLE 5-2
Performance Check Summary

Characteristic	Performance Requirement			Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
A/D CONVERTER PERFORMANCE					
Accuracy[1]	Signal Freq.	S/N Ratio	No. of EFF. Bits	See footnote 1.	See footnote 1.
	300 kHz 20 MHz 80 MHz	42.0 32.0 20.0	7.8 6.0 4.0		
Monotonicity	Monotonic at 300 kHz.			F2. Check Monotonicity.	J2. Check Channel A Monotonicity. J3. Check Channel B Monotonicity.
VERTICAL DEFLECTION SYSTEM					
Bandwidth	90 MHz −3 dB.			G7. Check Channel A Bandwidth. G8. Check Channel B Bandwidth.	K7. Check/Adjust Channel A Bandwidth. K8. Check/Adjust Channel B Bandwidth.
Aberrations response to 192 LSB positive step	+4% or −4%, total 4% p-p.			G9. Check Channel A Aberration. G10. Check Channel B Aberration.	K9. Check Channel A Aberration. K10. Check Channel B Aberration.
Low-Frequency Step Response	Less than ±1%, total of 1% p-p tilt or overshoot.			G11. Check Channel A Low-Frequency Step Response. G12. Check Channel B Low-Frequency Step Response.	K11. Check Channel A Low-Frequency Step Response. K12. Check Channel B Low-Frequency Step Response.
Channel Isolation	Greater than 20:1 at 75 MHz.			G6. Check Channel Isolation.	K6. Check Channel Isolation.
Deflection Factor	Compatible with all 7000-series plug-in units.			G3. Check Channel A Gain. G5. Check Channel B Gain.	K3. Check/Adjust Channel A Gain. K5. Check/Adjust Channel B Gain.
A AND B TIME BASES					
Clock					
Internal Rate	200 MHz ±.0035%.			A2. Check Internal Clock Accuracy.	E3. Check Clock Frequency.
External Clock In Frequency Range	Less than or equal to 200 MHz.			D2. Check External Clock Input.	H2. Check External Clock Input.
Rise and Fall Time	Less than or equal to 1 ns.			D2. Check External Clock Input.	H2. Check External Clock Input.
Pulse Width	2.5 ns minimum.			D2. Check External Clock Input.	H2. Check External Clock Input.
Time Measurement Accuracy	±.0035%			E2. Check Accuracy of Time Base A. E3. Check Accuracy of Time Base B.	12. Check Accuracy of Time Base A. 13. Check Accuracy of Time Base B.
Triggering Ambiguity [1]	±1 sample ambiguity in recognizing the trigger; 1 sample maximum recognition between channels.			See footnote 1.	See footnote 1.

[1]The procedure for verifying this characteristic requires special equipment and/or software. As such, it is not checked in the Performance Check Procedure given in the 7612D Service Manual. The characteristic can be checked at any designated Tektronix field service center.

TABLE 5-2 (cont)

Characteristic	Performance Requirement			Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
TRIGGERING					
Trigger Sensitivity to Repetitive Signals	Freq. Range	Minimum Signal Required			
Coupling:		Int	Ext	C2. Check Channel A Internal Trigger.	G2. Check/Adjust Channel A Internal Trigger.
AC	40 Hz-50 MHz	20 LSB		C3. Check Channel B Internal Trigger.	G3. Check/Adjust Channel B Internal Trigger.
			100 mV	C7. Check External Trigger.	G7. Check/Adjust External Trigger.
	50 MHz-100 MHz-	44 LSB		C2. Check Channel A Internal Trigger.	G2. Check/Adjust Channel A Internal Trigger.
				C3. Check Channel B Internal Trigger.	G3. Check/Adjust Channel B Internal Trigger.
			100 mV	C7. Check External Trigger.	G7. Check/Adjust External Trigger.
AC HF REJ	40 Hz-50 kHz	20 LBS		C4. Check Internal High-Frequency Reject.	G4. Check Internal High-Frequency Reject.
			100 mV	C8. Check External High-Frequency Reject.	G8. Check External High-Frequency Reject.
DC	Dc—50 MHz	20 LSB		C2. Check Channel A Internal Trigger.	G2. Check/Adjust Channel A Internal Trigger.
	50 MHz—100 MHz	44 LSB		C3. Check Channel B Internal Trigger.	G3. Check/Adjust Channel B Internal Trigger.
	Dc—50 MHz		50 mV	C7. Check External Trigger.	G7. Check/Adjust External Trigger.
	50 MHz—100 MHz		100 mV		
DC HF REJ	Dc—50 kHz	20 LSB		C4. Check Internal High-Frequency Reject.	G4. Check Internal High-Frequency Reject.
			100 mV	C8. Check External High-Frequency Reject.	G8. Check External High-Frequency Reject.
Range of LEVEL Control with 1 kHz Sine-Wave Input					
Internal	At least −128 to +128 LSBs.			C5. Check Internal Trigger Level Range.	G5. Check Internal Trigger Level Range.
External	At least −1.28 V to +1.28 V			C9. Check External Trigger Level Range.	G9. Check External Trigger Level Range.
IEEE 488 INTERFACE					
Data Connector	Conforms to IEEE Standard 488-1975.			Verified at the factory.	
X,Y,Z Analog Display Outputs of Waveform Data					
X and Y	1 V p-p, ±3%, into 100 kΩ or more: adjustable from 0.75 to 1.3 V.			B3. Check X Gain. B2. Check Y Gain.	F3. Check/Adjust X Gain. F2. Check/Adjust Y Gain.
Z	Zero V blanked, 1 V unblanked into 100 kΩ or more. Blanked between data points.			B4. Check Z Gain.	F4. Check Z Gain.

TABLE 5-2 (cont)

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
POWER SUPPLY			
Input Line Voltage Ranges			
115 V Nominal	90-132 V ac		
230 V Nominal	180-250 V ac		
Line Frequency	48-440 Hz	Does not normally require customer verification. Satisfactory operation verified at the factory.	
Power Consumption Maximum (including plug-in units)	400 W, 5 A at 60 Hz, 115 V line (fused t 8 A, fast-blow)		
Remote Control			
REMOTE ACTUATE INPUT	A TTL low (<0.8 V applied between center and outer conductors will turn the power supply on.	H2. Check REMOTE ACTUATE Input.	L2. Check REMOTE ACTUATE Input.
REMOTE ENABLE OUTPUT	Provides a TTL low (<0.8 V) between center and outer conductors about 150 ms after power-up. Maximum sink current is 16 mA.	H3. Check REMOTE ENABLE Output.	L3. Check REMOTE ENABLE Output.

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 5-3 is required for a complete Adjustment and Performance Check of the 7612D. If only a Performance Check is to be performed, the items for Adjustment are not required and are indicated by footnote 1. The remaining test equipment is common to both procedures.

The specifications for test equipment given in Table 5-3 are the minimum required to meet the performance requirements. Detailed operating instructions for test equipment are omitted in these procedures. Refer to the test equipment instruction manual if more information is needed.

SPECIAL FIXTURES

Special fixtures are used only where they facilitate instrument adjustment. These fixtures are available from Tektronix, Inc. Order by part number from Tektronix Field Offices or representatives.

TEST EQUIPMENT ALTERNATIVES

All of the listed test equipment is required to completely calibrate this instrument. However, complete checking or adjusting may not always be necessary or desirable. You may be satisfied with checking only selected characteristics, thereby reducing the amount of test equipment actually required. The calibration procedures in Part I and Part II are based on the first item of equipment given as an example. When other equipment is substituted, control settings or setups may need to be altered. If the exact item of equipment given as an example in Table 5-3 is not available, first check the Minimum Specifications column carefully to see if any other equipment might suffice. Then check the Purpose column to see why this item is used. If used for a performance check or adjustment that is of little or no importance for your measurement requirements, the item and corresponding step(s) can be deleted.

TABLE 5-3
Test Equipment

Description	Minimum Specification	Purpose	Recommended Equipment
1. Test Oscilloscope	Bandwidth, dc to 200 MHz; dual trace. Four plug-in compartments.	Observe waveforms while checking performance.	TEKTRONIX 7704A Oscilloscope System.
2. Amplifier (two needed)	Bandwidth, dc to 500 MHz; 10 mV maximum sensitivity; 50 Ω input.	Used to check Time Base and Monotonicity.	TEKTRONIX 7A19 Amplifier.
3. Amplifier (two needed)	Bandwidth, dc to 225 MHz; 5 mV maximum sensitivity; 1 megohm input.	Used in eight tests.	TEKTRONIX 7A16A Amplifier.
4. Programmable Amplifier (two needed)	Bandwidth, dc to 225 MHz; 5 mV maximum sensitivity; 1 megohm and 50 Ω input.	Used to check CRT Alignment, Bit Symmetry, Clock Buffer, and Trigger.	TEKTRONIX 7A16P Programmable Amplifier.
5. Differential Amplifier (two needed)	Sensitivity, 5 mV maximum; dc offset; selectable upper and lower −3 dB points.	Used to check Monotonicity.	TEKTRONIX 7A22 Differential Amplifier.
6. Time Base	Fastest sweep rate, 10 ns/div.; triggering to 400 MHz.	Provides sweep for test oscilloscope.	TEKTRONIX 7B80 Time Base.
7. Counter [1]	Frequency range, to 225 MHz; Resolution, 0.1 Hz maximum.	Used to check Clock Buffer, Time Base, and Time Measurement Accuracy.	TEKTRONIX 7D15 225 MHz Universal Counter/Timer.
8. Probe [1] (two needed)	Dc−300 MHz, 10X attenuation.	Used to check CRT Alignment.	TEKTRONNIX P6106.
9. Probe [1]	Dc−250 MHz, 10x attenuation.	Used to check High Voltage Oscillator, Bit Symmetry, Time Base, and Time Measurement Accuracy.	TEKTRONIX P6053B.
10. Test Leads for DMM[1]		Connect input to DMM.	Tektronix Part No. 030-0120-00.
11. Digital Multimeter	200 V range; 0.1% dc voltage accuracy.	Measure voltages in Power Supply, CRT Alignment, Clock Buffer, Vertical, Power Supply Remote Control, and External Connectors.	TEKTRONIX DM 501A Digital Multimeter.
12. Pulse Generator	Rep rate range, 10 Hz to 250 MHz; pulse width range, 2 ns to 50 ms; maximum amplitude, 5 V into 50 Ω.	Used to check Time Base.	TEKTRONIX PG 502 250 MHz Pulse Generator.
13. Function Generator	Frequency range, 0.1 Hz to 11 MHz; sine wave, triangle, and ramp outputs; up to 5 V output into 50 Ω.	Used to check CRT Alignment, Trigger, Monotonicity, and External Connectors.	TEKTRONIX FG 501A 2 MHz Function Generator.
14. Sine-Wave Generator	Frequency range, to 250 MHz; output to 5 V into 50 Ω.	Used to check Clock Buffer and Trigger.	TEKTRONIX SG 503 Leveled Sine Wave Generator.
15. Power Module Mainframe (TM 500-series)	Capable of housing and powering three TM 500-series test instruments.	Provides housing and power for items 11, 12, 13, 14.	TEKTRONIX TM 503, TM 504 or TM 506 Power Module.

[1]**Used for adjustment only; not used for performance check.**

TABLE 5-3 (cont)

Description	Minimum Specification	Purpose	Recommended Equipment
16. Display Monitor	Bandwidth—dc to 3 MHz. Deflection Factor—at least 100 mV/division. Input R and C—1 MΩ and 50 pf. Slew Rate—Half-scale in 1 μs. Write a spot in 9 μs.	Used in checking CRT Alignment, Clock Buffer, Trigger, and Monotonicity.	TEKTRONIX 624 Monitor or equivalent.
17. Coaxial Cable (five needed)	Impedance, 50 Ω; Length, 42 inches; Connectors, bnc male.	Used to connect signals.	Tektronix Part No. 012-0057-01.
18. Coaxial Cable	Impedance, 50 Ω; Length 36 inches; Connectors, bnc male.	Used with PG 502 to check Time Base.	Tektronix Part No. 012-0482-00.
19. Calibration Fixture	Provide gain and pulse signals.	Used to check XYZ Display and Vertical.	Tektronix Part No. 067-0587-02.
20. Adapter (two needed)	Bnc female (two) to bnc male (one).	Used to check CRT Alignment, Bit Symmetry, Trigger, and Vertical.	Tektronix Part No. 103-0030-00.
21. Adapter	Bnc female (one) to dual banana plug.	Used to check Power Supply Remote Control and External Connectors.	Tektronix Part No. 103-0090-00.
22. Dual-Input Coupler	Impedance, 50 Ω; connectors: bnc male, two; female, one.	Used to check Bit Symmetry and Clock Buffer.	Tektronnix Part No. 067-0525-01.
23. Attenuator	Attenuation, 10X; Impedance, 50 Ω; Connectors, bnc.	Used in Trigger check.	Tektronix Part No. 011-0059-02.
24. Shorting Cap	Connector, bnc male. Impedance, zero ohms.	Used to check continuity of External Connectors.	Tektronix Part No. 200-0678-00.
25. Time Mark Generator	Markers, 0.1 μS; amplitude 1 V into 50 Ω.	Used to check Time-Measurement Accuracy.	TEKTRONIX TG 501 Time Mark Generator.

PART I—PERFORMANCE CHECK

The following procedure (Part I—Performance Check) verifies electrical specifications without making internal adjustments. All tolerances given are as specified in the Specification tables (Section 1) in this manual.

Part II—Adjustment and Performance Check provides the information necessary to: (1) verify that the instrument meets the electrical specifications, (2) verify that the controls function properly, and (3) perform all internal adjustments.

See Table 5-1, Calibration Procedure Electives, at the beginning of this section, for information on performing a Partial Part I—Performance Check procedure.

INDEX TO PART I— PERFORMANCE CHECK

PERFORMANCE CHECK INITIAL SETUP PROCEDURE

NOTE

The performance of the 7612D can be checked at any ambient temperature from 0° C to +40° C unless otherwise stated.

1. Before starting the performance check, thoroughly clean and inspect the 7612D. Correct any problems before continuing.

2. Check that the Line Voltage Selector is set for the nominal line voltage available, and connect a suitable power cord to the power input connector. If the nominal line voltage is not within the two ranges of the Line Voltage Selector, use a variable autotransformer to provide the desired voltage. Be sure the safety-earth ground path is intact so that the 7612D chassis is connected directly to ground via the power cord.

3. Set the rear-panel PRINCIPAL POWER SWITCH to ON.

4. Turn the 7612D on by pressing the front-panel ON/OFF button. (It will light when power is applied to the instrument.) Allow at least 30 minutes warmup before proceeding.

5. Power-up conditions for the programmable parameters are:

   RECORD LENGTH 2048
   NO OF RECORDS 1
   BREAKPOINT LOCATION 0000
   SAMPLE INTERVAL 5E-9
   SAMPLES 00
   TRIGGER FUNCTIONS
   SELECT L
   SOURCE . . . . . INT
   SLOPE . . . . . +
   COUPLING . . . . . AC
   HF REJ . . . . . OFF
   TRIGGER LEVEL 00
   INSTRUMENT FUNCTION
   PROGRAM . . . . . CHANNEL A
   CLK . . . . . INT

6. Turn off power when removing or installing plug-in units, then allow a short time for the 7612D to stabilize when it is turned on.

7. The 7612D front and rear-panel controls and connectors are spelled and capitalized in this procedure as they appear on the instrument. Internal adjustments are initial capitalized as they appear in the diagrams section.

8. The display monitor may remain connected throughout the procedure.

9. Be sure the test oscilloscope is operating correctly at all times. Check and adjust the test oscilloscope front-panel gain and sweep calibration and the compensation of all probes before beginning and at any point in the procedure where the plug-in units or probes are changed.

A. INTERNAL CLOCK ACCURACY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

4. Programmable Amplifier, 7A16P
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cables, 42 inch (four needed)
25. Time-Mark Generator, TG 501

A1. INTERNAL CLOCK ACCURACY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

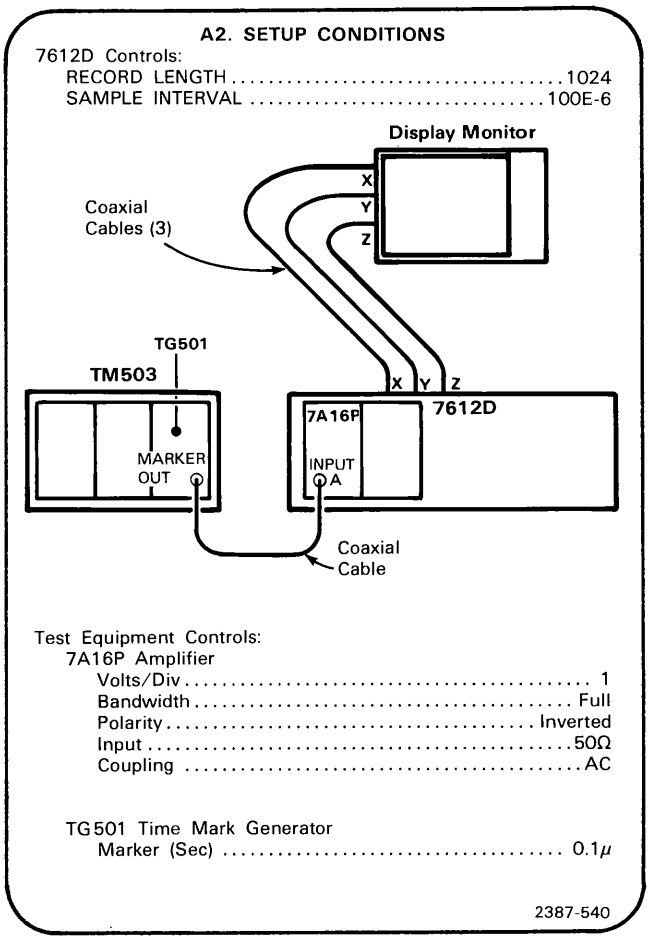
b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

A2. CHECK INTERNAL CLOCK ACCURACY

NOTE

First perform step A1, then proceed.



a. Press the 7612D ARM A button.

b. **CHECK**—that the monitor display contains 17 or fewer time marks.

B. XYZ DISPLAY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A
6. Time Base, 7B80
17. Coaxial Cable (42 inch)
19. Calibration Fixture

B1. XYZ DISPLAY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I— Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

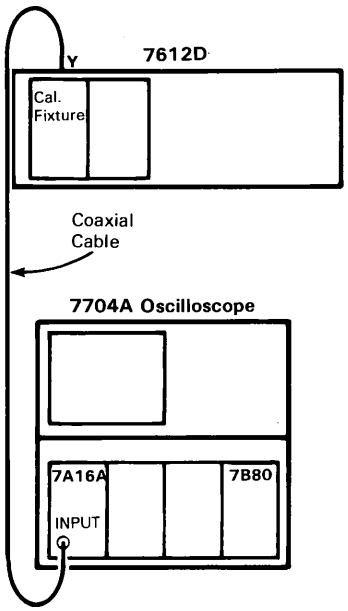
B2. CHECK Y GAIN

NOTE

First perform step B1, then proceed.

B2. SETUP CONDITIONS

7612D Controls:
- ON/OFF ..... OFF



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode

7A16A Amplifier
- Volts/Div 0.2
- Coupling ..... DC
- Polarity ..... +Up

7B80 Time Base
- Time/Div ..... 2 ms
- Triggering
  - Mode ..... Norm
  - Coupling ..... AC
  - Source ..... Int
  - Slope ..... +
  - Level ..... Centered

Calibration Fixture
- Rep Rate ..... 1 kHz
- Position ..... Centered
- Test ..... Vert or Horiz Gain

2387-541

a. Turn on the 7612D.

b. Press the 7612D SAMPLE INTERVAL button.

c. Use the DECREMENT/INCREMENT buttons to set the A Sample Interval to 20E-6.

d. Press the 7612D COPY button. This programs Channel B with the Sample Interval (20E-6) from Channel A.

e. Press the 7612D ARM A button.

f. Observe the display on the test oscilloscope. If necessary, adjust the time base Variable Time/Div to provide a stable display.

g. Leave the 7612D turned on, and move the Calibration Fixture from Channel A to Channel B.

h. Press the PROGRAM CHANNEL B button.

i. Press the TRIGGER SELECT R button.

j. Press the ARM B button.

k. Observe the display on the test oscilloscope. If necessary, adjust the Variable Time/Div to provide a stable display.

l. **CHECK**—that the distance between the top and bottom stairsteps is 5.0 ±0.15 (4.85 to 5.15) divisions. See Figure 5-1.

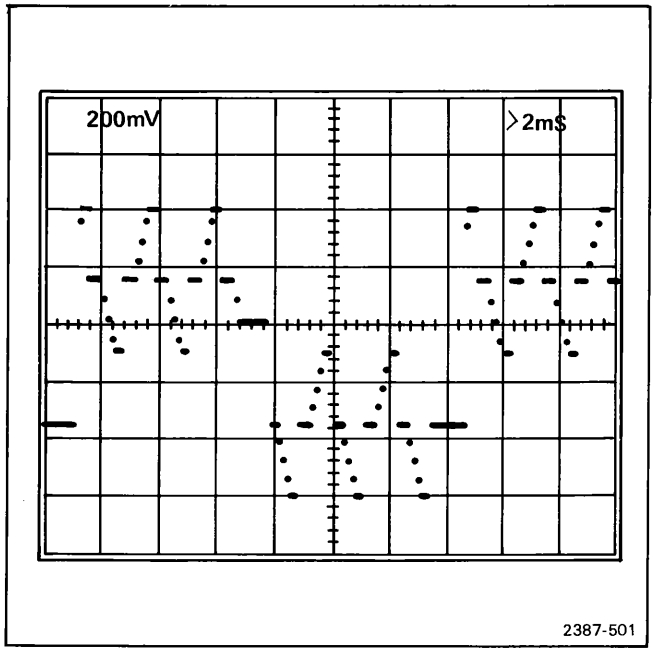


Fig. 5-1. Display of staircase waveforms for checking Y gain.

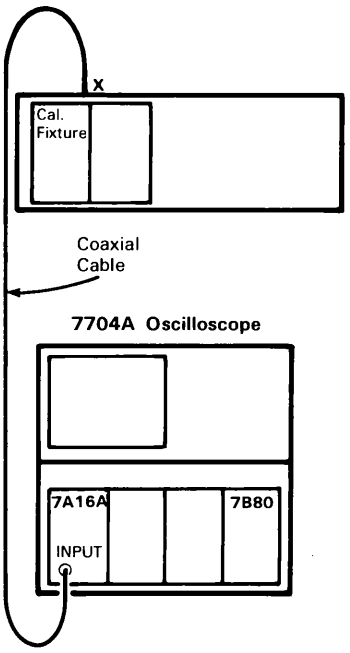
B3. CHECK X GAIN

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B3. SETUP CONDITIONS

7612D Controls:
Make no changes



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode

7A16A Amplifier
- Volts/Div 0.2
- Coupling ..... DC
- Polarity ..... +Up

7B80 Time Base
- Time/Div ..... 2 ms
- Triggering
  - Mode ..... Norm
  - Coupling ..... AC
  - Source ..... Int
  - Slope ..... –
  - Level ..... Centered

Calibration Fixture
- Rep Rate 1kHz
- Position ..... Centered
- Test ..... Vert or Horiz Gain

2387-542

a. Observe the test oscilloscope display. If necessary, adjust the Variable Time/Div to provide a stable display.

b. **CHECK**—that the amplitude of the ramp displayed on the test oscilloscope is between 4.85 and 5.15 divisions (5.0 ±0.15 div). See Figure 5-2.

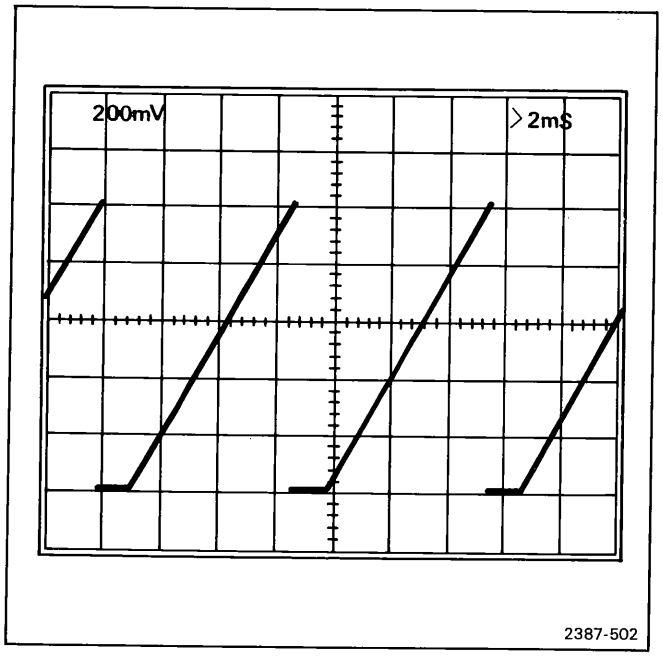


Fig. 5-2. Display of ramp waveform for checking X gain.

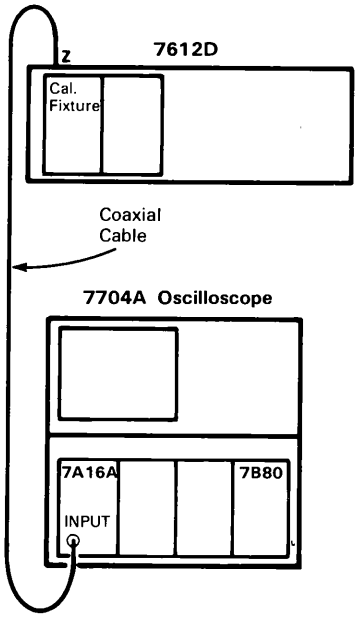
B4. CHECK Z GAIN

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B4. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7704 Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Soruce ..... Vert Mode

7A16A Amplifier
- Volts/Div 0.5
- Coupling ..... DC
- Bandwidth ..... 20 MHz
- Polarity ..... +Up

7B80 Time Base
- Time/Div 2μs
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... Int
  - Slope ..... +
  - Level ..... Centered

2387-543

a. **CHECK**—that the amplitude of the unblanking pulse is at least one volt (two divisions).

C. TRIGGER

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
4. Programmable Amplifier, 7A16P (two needed)
6. Time Base, 7B80
13. Function Generator, FG 501A
14. Sine-Wave Generator, SG 503
15. Power Module Mainframe, TM 503
17. Coaxial Cable, 42 inch (four needed)
20. Adapter, bnc T
23. Attenuator, 10X

C1. TRIGGER PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

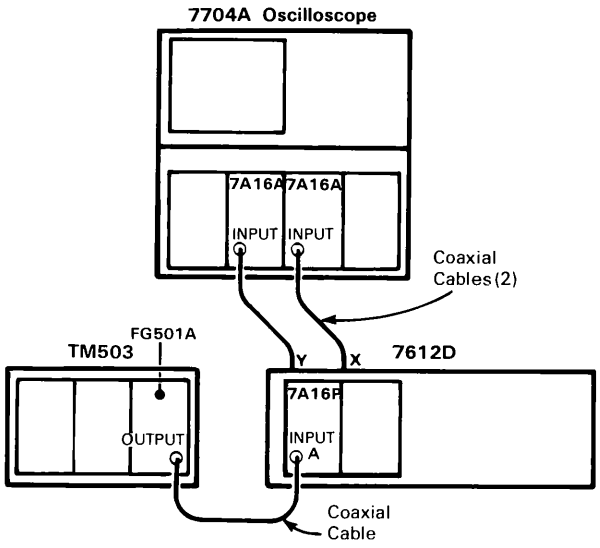
C2. CHECK CHANNEL A INTERNAL TRIGGER

NOTE

First perform step C1, then proceed.

C2. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6



Test Equipment Controls:

7A16P
- Volts/Div 0.2
- Input 50Ω
- Coupling ..... AC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

FG501A Function Generator
- Frequency Hz 5
- Multiplier ..... 10^4
- Function ..... ~(sine wave)
- Offset ..... Pressed in
- Amplitude ..... Min

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifiers
- Volts/Div 0.1
- Coupling ..... DC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

2387-544A

a. Find the upper and lower limiting points of the Channel A amplifier as follows:

1. While observing the test oscilloscope display, repeatedly press the ARM A button and advance the FG 501A Amplitude control until the amplitude of the sine wave displayed on the oscilloscope will increase no more. The sine wave will then appear clipped on its tops and bottoms.
2. Set the Right Vertical 7A16A to 50 mV/Div.
3. Release the Right Vertical 7A16A Variable Volts/Div control.
4. Use the Right Vertical 7A16A Variable Volts/Div and Position controls to set the top and bottom of the waveform to the top and bottom graticule lines. The display will be eight divisions high.

b. Set the 7A16P, in the 7612D, to 2 V/Div.

c. Repeatedly press the ARM A button while adjusting the FG 501A Amplitude control to produce a display of three minor divisions on the test oscilloscope. (If the 7612D will not trigger at this low amplitude, slightly adjust the 7A16P Position control until it triggers again.)

d. **CHECK**—for a triggered XY display (L TRIGGERED light on) on the test oscilloscope in the following eight Trigger settings:

COUPLING	SLOPE	HF REJ
1. AC	+	On
2. AC	+	Off
3. AC	−	On
4. AC	−	Off
5. DC	+	On
6. DC	+	Off
7. DC	−	On
8. DC	−	Off

e. Set the FG 501A to 40 Hz.

f. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude control as needed to cause a display of three minor divisions on the test oscilloscope.

g. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the following eight Trigger settings:

COUPLING	SLOPE	HF REJ
1. AC	+	On
2. AC	+	Off
3. AC	−	On
4. AC	−	Off
5. DC	+	On
6. DC	+	Off
7. DC	−	On
8. DC	−	Off

Set 7A16P Position and Trigger Level as necessary to verify triggering.

h. Connect the signal cable to the SG 503 Leveled Sine Wave Generator, and set the SG 503 as follows:

Frequency Range 25-50
Frequency Variable . . . . . To cause a readout of 50.0 on the Frequency MHz readout.
Amplitude Multiplier . . . . . X .1
Output Amplitude Volts P-P . . . Minimum

i. While repeatedly pressing the ARM A button, set the SG 503 Output Amplitude control to produce a display of 1.18 major divisions on the oscilloscope display.

j. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the four following Trigger settings:

SLOPE	COUPLING	HF REJ
+	AC	Off
+	DC	Off
−	AC	Off
−	DC	Off

k. Set the SG 503 to 100 MHz.

l. Set the 7612D SAMPLE INTERVAL to 100E-9.

m. Repeatedly press the ARM A button and check that the XY display on the oscilloscope is 1.18 major divisions in amplitude. If necessary, adjust the SG 503 Output Amplitude for the desired amplitude.

n. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the following four Trigger settings:

SLOPE	COUPLING	HF REJ
+	AC	Off
+	DC	Off
−	AC	Off
−	DC	Off

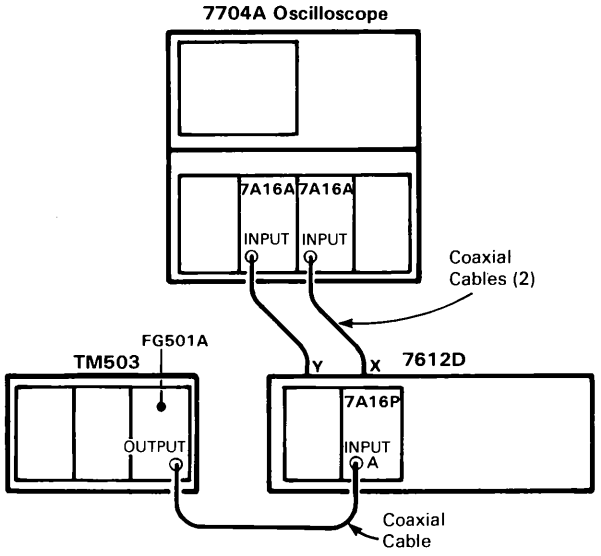
C3. CHECK CHANNEL B INTERNAL TRIGGER

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C3. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6
INSTRUMENT FUNCTION
PROGRAM ..... CHAN E
TRIGGER FUNCTIONS
SELECT ..... R



Test Equipment Controls:

7A16P
Volts/Div 0.2
Input 50Ω
Coupling ..... AC
Bandwidth ..... Full
Polarity ..... +Up
Position ..... Centered

FG501A Function Generator
Frequency Hz 5
Multiplier ..... 10^4
Function ..... ∿(sine wave)
Offset ..... Pressed in
Amplitude ..... Min

7704A Oscilloscope
Vertical Mode ..... Right
Horizontal Mode ..... A

7A16A Amplifiers
Volts/Div 0.1
Coupling ..... DC
Bandwidth ..... Full
Polarity ..... +Up
Position ..... Centered

2387-545A

a. Find the upper and lower limiting points of the Channel B amplifier as follows:

1. While observing the test oscilloscope display, repeatedly press the ARM B button and advance the FG 501A Amplitude control until the amplitude of the sine wave displayed on the oscilloscope will increase no more. The sine wave will then appear clipped on its tops and bottoms.

2. Set the Right Vertical 7A16A to 50 mV/Div.

3. Release the Right Vertical 7A16A Variable Volts/Div control.

4. Use the Right Vertical 7A16A Variable Volts/Div and Position controls to set the top and bottom of the waveform to the top and bottom graticule lines. The display will be eight divisions high.

b. Set the 7A16P, in the 7612D, to 2 V/Div.

c. Repeatedly press the ARM A button while adjusting the FG 501A Amplitude control to produce a display of three minor divisions on the test oscilloscope. (If the 7612D will not trigger at this low amplitude, slightly adjust the 7A16P Position control until it triggers again.)

d. **CHECK**—for a triggered (XY display (R TRIGGERED light on) on the test oscilloscope in the following eight Trigger settings:

	SLOPE	COUPLING	HF REJ
1.	+	AC	On
2.	+	AC	Off
3.	+	DC	On
4.	+	DC	Off
5.	−	AC	On
6.	−	AC	Off
7.	−	DC	On
8.	−	DC	Off

e. Set the FG 501A to 40 Hz.

f. While repeatedly pressing the ARM B button, adjust the FG 501A Amplitude control as needed to cause a display of three minor divisions on the test oscilloscope.

g. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the following eight Trigger settings:

	SLOPE	COUPLING	HF REJ
1.	+	AC	On
2.	+	AC	Off
3.	+	DC	On
4.	+	DC	Off
5.	−	AC	On
6.	−	AC	Off
7.	−	DC	On
8.	−	DC	Off

Set 7A16P Position and TRIGGER LEVEL as necessary to verify triggering.

h. Connect the signal cable to the SG 503 Leveled Sine Wave Generator, and set the SG 503 as follows:

Frequency Range 25-50
Frequency Variable . . . . . To cause a readout of 50.0 on the Frequency MHz readout.
Amplitude Multiplier X1
Output Amplitude Volts P-P . . . Minimum

i. While repeatedly pressing the ARM B button, set the SG 503 Output Amplitude control to produce a display of 1.18 major divisions on the oscilloscope display.

j. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the four following Trigger settings:

SLOPE	COUPLING	HF REJ
+	AC	Off
+	DC	Off
−	AC	Off
−	DC	Off

k. Set the SG 503 to 100 MHz.

l. Set the 7612D SAMPLE INTERVAL to 100E-9.

m. Repeatedly press the ARM B button and check that the XY display on the oscilloscope is 1.18 major divisions in amplitude. If necessary, adjust the SG 503 Output Amplifier for the desired amplitude.

n. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the following four Trigger settings:

SLOPE	COUPLING	HF REJ
+	AC	Off
+	DC	Off
−	AC	Off
−	DC	Off

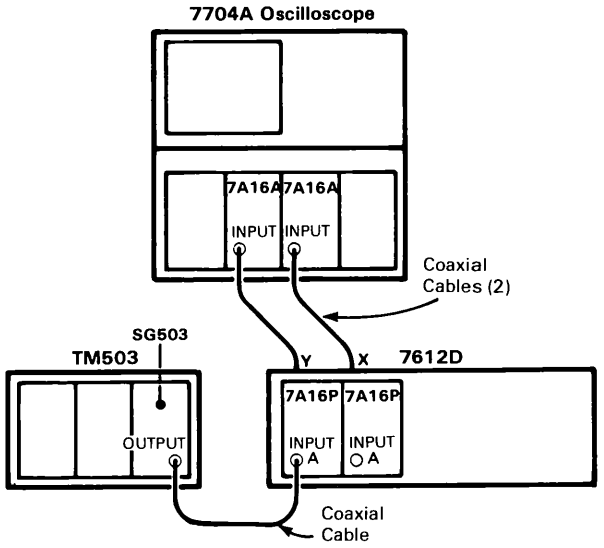
C4. CHECK INTERNAL HIGH-FREQUENCY REJECT

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C4. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6



Test Equipment Controls:

7A16P Amplifiers
Volts/Div 0.5
Input 50Ω
Coupling . . . . . AC
Bandwidth . . . . . Full

SG503 Leveled Sine Wave Generator
Frequency Range (MHz) 25-50
Frequency Variable . . . . . To produce an output of 50 MHz.
Amplitude Multiplier X1

7704A Oscilloscope
Vertical Mode . . . . . Right
Horizontal Mode . . . . . A

7A16A Amplifiers
Volts/Div 0.1
Coupling . . . . . DC
Bandwidth . . . . . Full
Polarity . . . . . +Up
Position . . . . . Centered

2387-546A

a. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude control for a two-major-division display on the test oscilloscope.

b. Set the 7612D to HF REJ mode.

c. **CHECK**—that the trigger circuit does not operate (L TRIGGERED light is off) in the four following trigger modes (the 7612D may trigger when switching modes and need to be re-armed):

	SLOPE	COUPLING	HF REJ
1.	+	AC	On
2.	+	DC	On
3.	−	AC	On
4.	−	DC	On

d. Press the 7612D COPY button.

e. Connect the SG 503 signal to the 7612D CHANNEL B input and press the PROGRAM CHANNEL B button.

f. Repeat steps a, b, and c, using the ARM B button.

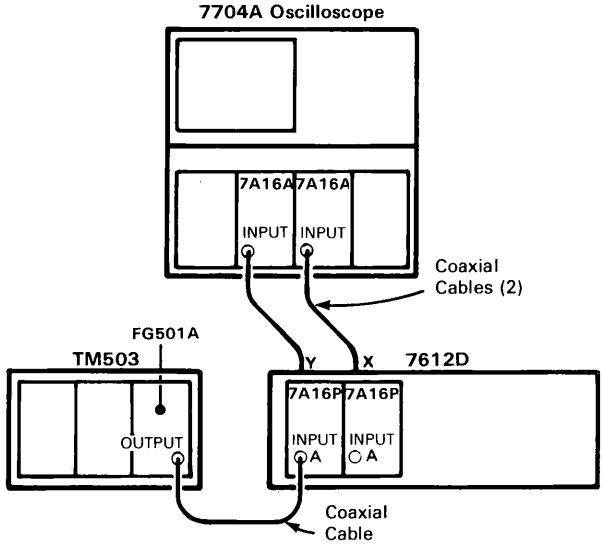
C5. CHECK INTERNAL TRIGGER LEVEL RANGE

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C5. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 6E-6



Test Equipment Controls:

7A16P Amplifiers
- Volts/Div 5
- Input 50Ω
- Coupling ..... AC
- Bandwidth ..... Full

FG501A Function Generator
- Frequency HZ 1
- Multiplier ..... 10^3
- Function ..... ~(sine wave)
- Offset ..... Pressed in
- Amplitude ..... Centered

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifiers
- Volts/Div 0.1
- Coupling ..... DC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

2387-547A

a. While repeatedly pressing the ARM A button, set the FG 501A Amplitude so that the oscilloscope display begins to clip.

b. Repeatedly press the ARM A button and adjust the 7A16P Position control so that the displayed waveform is clipped equally at its top and bottom.

c. Continue pressing the ARM A button, and adjust the FG 501A Amplitude control so that the displayed waveform amplitude is just short of the clipping points.

d. **CHECK**—the oscilloscope for a triggered XY display (7612D L TRIGGERED light on) that varies, while changing the 7612D TRIGGER LEVEL and pressing the ARM A button, from a base level (00) to a maximum positive level, then back to the base level and on to a maximum negative level. Figure 5-3 shows the desired display.

e. Connect the FG 501A output to the 7612D CHANNEL B input.

f. Press the COPY button, then press PROGRAM CHANNEL B.

g. Repeat parts a through d, using the ARM B button.

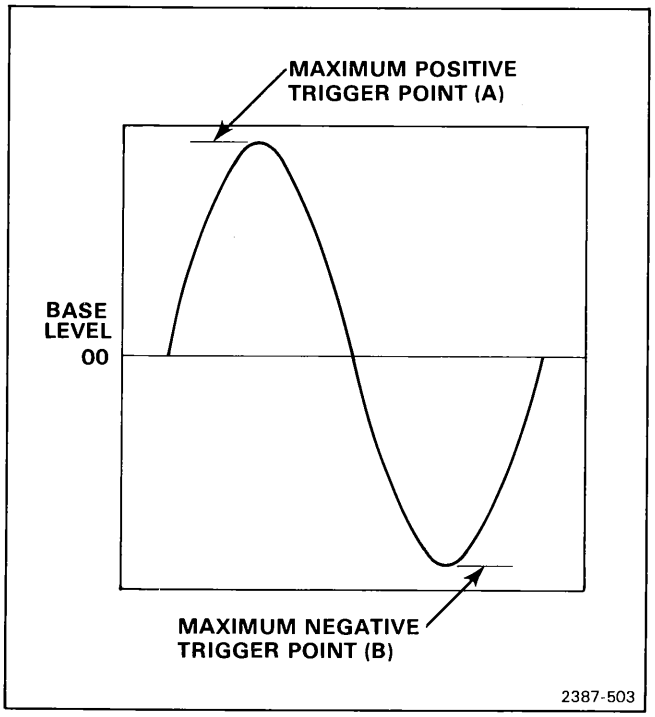
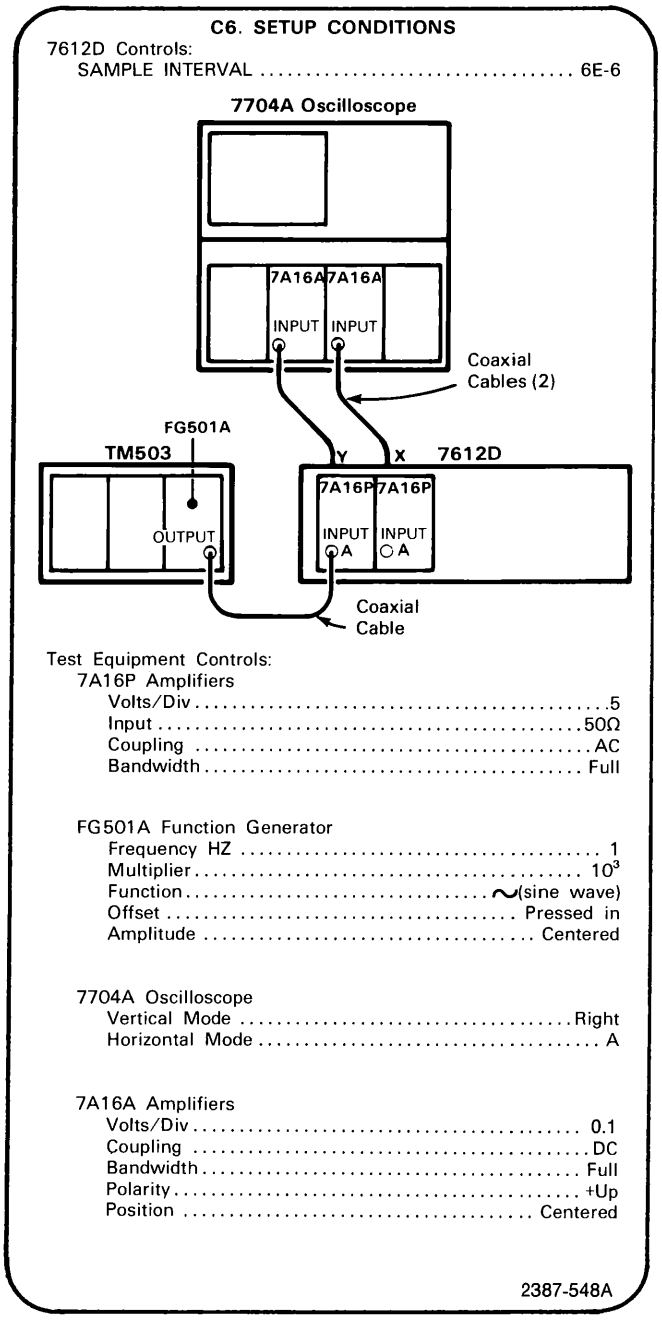


Fig. 5-3. XY display showing maximum positive and negative trigger points.

C6. CHECK MANUAL TRIGGER

NOTE

If the preceding step was not performed, first perform step C1, then proceed.



a. Increase the left 7A16D Volts/Div until the L TRIGGERED light goes out. If necessary, reduce the amplitude of the input signal.

b. Press the ARM A button; observe that the ARM A button lights and stays lit.

c. **CHECK**—that pressing the MAN TRIG button causes the L TRIGGERED button to light momentarily, that a triggered XY display appears on the test oscilloscope, and that the ARM A button is now extinguished.

d. Press COPY, then press PROGRAM CHANNEL B.

e. Connect the FG 501A output signal to the 7612D CHANNEL B input.

f. Repeat parts a through c for the CHANNEL B, using the R TRIGGERED light and the ARM B button.

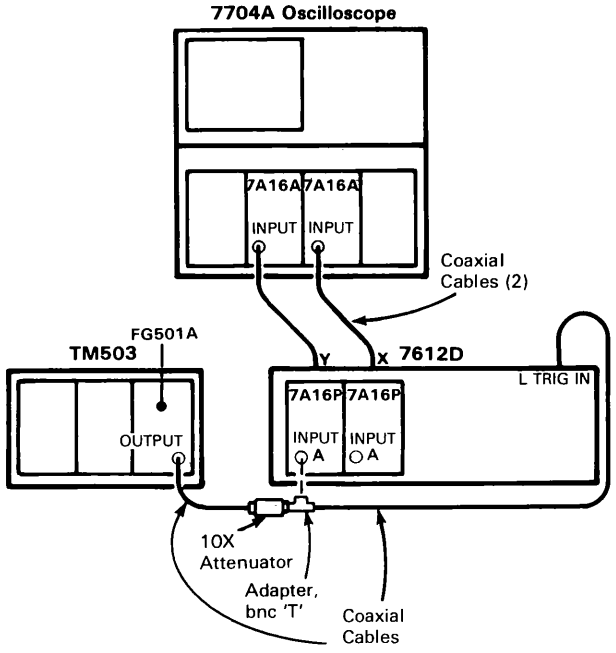
C7. CHECK EXTERNAL TRIGGER

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C7. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 100E-9
- TRIGGER FUNCTIONS
  - SOURCE ..... EXT



Test Equipment Controls:

7A16P Amplifiers
- Volts/Div ..... 50 mV
- Input ..... 1 MΩ
- Coupling ..... AC
- Bandwidth ..... Full

FG 501A Function Generator
- Frequency Hz 5
- Multiplier ..... 10^4
- Function ..... ~(sine wave)
- Offset ..... Press in
- Amplitude ..... Minimum

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifier (both)
- Volts/Div 0.1
- Coupling ..... DC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

2387-549A

a. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude control for an XY display amplitude of one major division on the 7704A.

b. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the following eight trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	AC	Off
3. +	DC	On
4. +	DC	Off
5. −	AC	On
6. −	AC	Off
7. −	DC	On
8. −	DC	Off

Set the vertical Position and TRIGGER LEVEL controls as necessary to verify triggering.

c. Change the FG 501A to 40 Hz.

d. Set the 7612D SAMPLE INTERVAL to 100E-6.

e. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude for an XY display of one major division on the 7704A.

f. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the eight following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	AC	Off
3. +	DC	On
4. +	DC	Off
5. −	AC	On
6. −	AC	Off
7. −	DC	On
8. −	DC	Off

Set the vertical Position and TRIGGER LEVEL controls as necessary for stable triggering.

g. Change the 7612D to:

SAMPLE INTERVAL 100E-9
HF REJ . . . . . Off

h. Connect the SG 503 in place of the FG 501A and set it to 50 MHz.

i. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude to cause a one-major-division XY display on the 7704A.

j. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the four following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

Set Vertical Position and TRIGGER LEVEL as necessary for stable triggering.

k. Change the SG 503 to 100 MHz.

l. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude to cause a two-major-division XY display on the 7704A.

m. Set the 7612D SAMPLE INTERVAL to 30E-9. Set the Vertical position and TRIGGER LEVEL as necessary for stable triggering.

n. **CHECK**—for a triggered XY display (L TRIGGERED Light on) in the four following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

o. Move the bnc "T" adapter from the CHANNEL A vertical input to the CHANNEL B vertical input, and move the coaxial cable from the L TRIG IN to the R TRIG IN connector.

p. Connect the FG 501A in place of the SG 503.

q. Set the 7612D to:

TRIGGERING LEVEL 00
PROGRAM . . . . . CHANNEL B
SAMPLE INTERVAL 100E-9

r. Set the FG 501A to 50 kHz.

s. While repeatedly pressing the ARM B button, adjust the FG 501A Amplitude to cause a one-major-division XY display on the 7704A.

t. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the eight following Trigger modes:

	SLOPE	COUPLING	HF REJ
1.	+	AC	On
2.	+	AC	Off
3.	+	DC	On
4.	+	DC	Off
5.	−	AC	On
6.	−	DC	Off
7.	−	AC	On
8.	−	DC	Off

Set the vertical Position and TRIGGER LEVEL as necessary for stable triggering.

u. Repeat parts c through n, using the R TRIGGER light and the ARM B button.

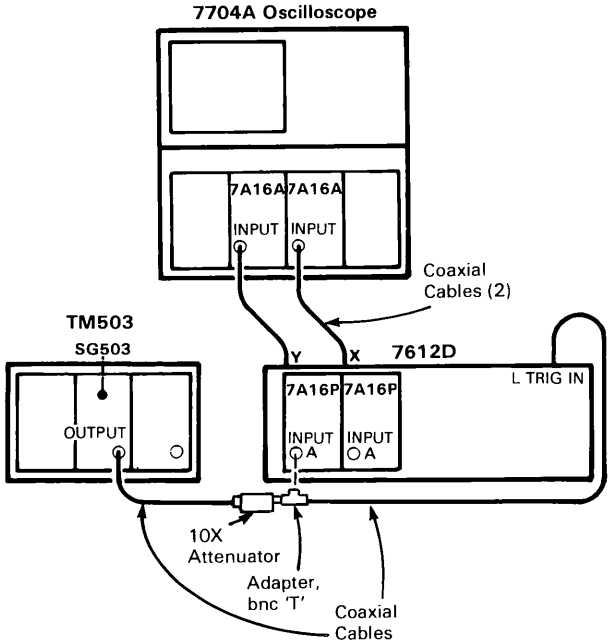
C8. CHECK EXTERNAL HIGH-FREQUENCY REJECT

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C8. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 100E-9
- TRIGGER FUNCTIONS
  - SOURCE ..... EXT



Test Equipment Controls:

7A16P Amplifiers
- Volts/Div ..... 50 mV
- Input ..... 1 MΩ
- Coupling ..... AC
- Bandwidth ..... Full

SG503 Leveled Sine Wave Generator
- Frequency Range (MHz) 25-50
- Frequency Variable ..... To cause a readout of 50.0 on Frequency MHz readout.
- Amplitude Multiplier X1
- Output Amplitude Volts P-P 2.0

7704A Osciloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifiers
- Volts/Div 0.1
- Coupling ..... DC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

2387-550A

a. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude to cause a three-major-division XY display on the 7704A.

b. Set the 7612D HF REJ to on (lighted).

c. **CHECK**—that the trigger circuit will not operate (L TRIGGERED light stays off) in the four following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	DC	On
3. −	AC	On
4. −	DC	On

d. Move the SG 503 inputs to the CHANNEL B and R TRIG IN connectors.

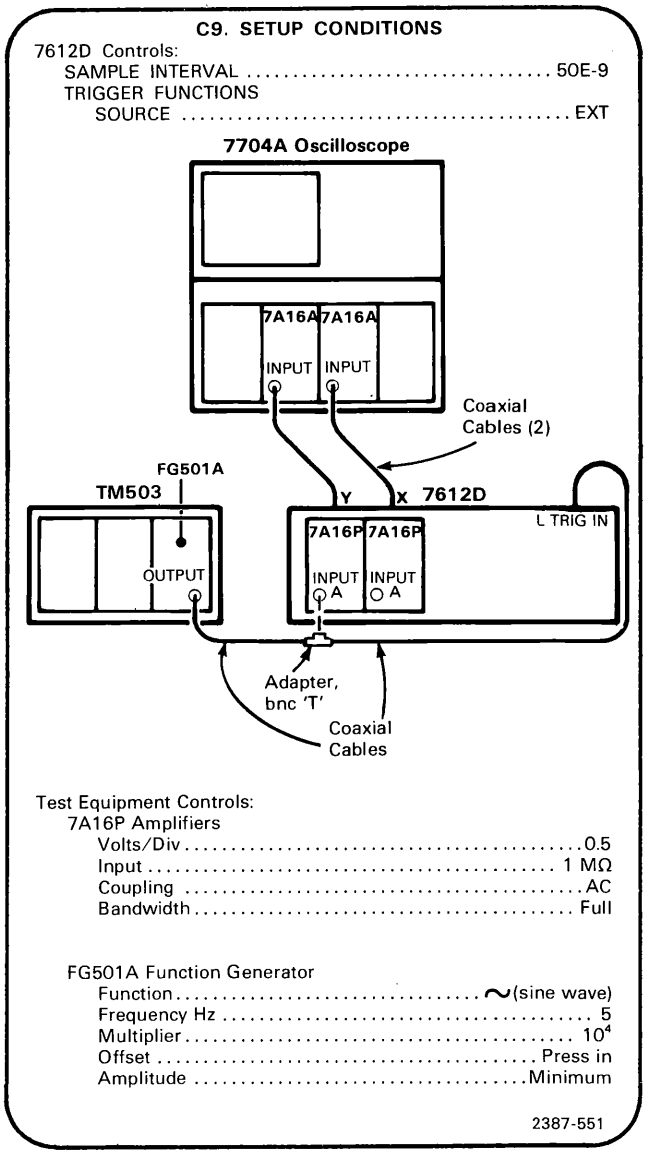
e. Press the COPY button, then press the PROGRAM CHANNEL B button.

f. **CHECK**—that the trigger circuit will not operate (R TRIGGER light stays off) in the four Trigger modes listed in part c.

C9. CHECK EXTERNAL TRIGGER LEVEL RANGE

NOTE

If the preceding step was not performed, first perform step C1, then proceed.



a. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude control to cause a 5.12-major-division XY display on the 7704A.

b. **CHECK**—the 7704A for a triggered XY display (7612D L TRIGGERED light on) that varies, while changing the 7612D TRIGGER LEVEL and pressing the ARM A button, from a base level (00) to a maximum positive level, then back to the base level and on to a maximum negative level. See Figure 5-4.

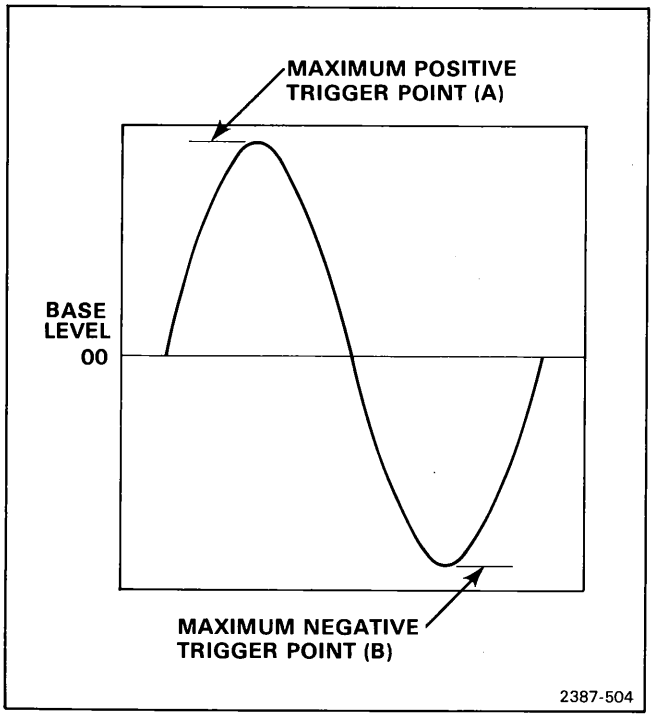


Fig. 5-4. XYZ display showing maximum positive and negative trigger points.

c. Disconnect the inputs from the CHANNEL A and L TRIG IN connectors, and connect them to the CHANNEL B input and rear-panel R TRIG IN connectors, respectively.

d. Press the 7612D COPY button, then press PROGRAM CHANNEL B.

e. Repeat parts a and b, using the ARM B button and the R TRIGGERED light.

D. TIME BASE

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
2. Amplifier, 7A19
4. Programmable Amplifier, 7A16P
6. Time Base, 7B80
12. Pulse Generator, PG 502
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cables, 42 inch (four needed)
18. Coaxial Cable, 36 inch

D1. TIME BASE PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

D2. CHECK EXTERNAL CLOCK INPUT

NOTE

First perform step D1, then proceed.

[insert D2. Setup Conditions]

a. Disconnect the PG 502 signal from the 7A19 in the test oscilloscope.

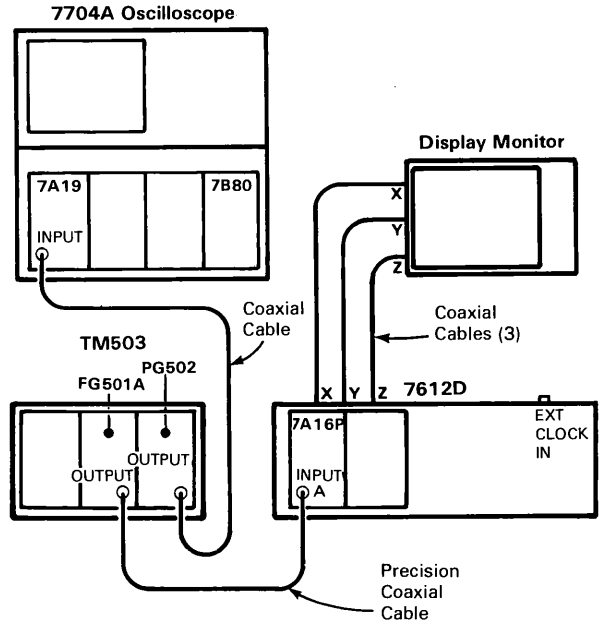
b. Connect the output of the PG 502 to the 7612D EXT CLK IN connector.

c. Press the ARM A button.

d. **CHECK**—that the monitor displays 10 triangle waves.

D2. SETUP CONDITIONS

7612D Controls:
- INSTRUMENT FUNCTION
  - CLK ..... EXT
- SAMPLE INTERVAL ..... 1E+0 (MULTIPLIER)



Test Equipment Controls:
- 7A16P Amplifier
  - Volts/Div 1
  - Bandwidth ..... Full
  - Polarity ..... Inverted
  - Input 50Ω
  - Coupling ..... AC
- 7704A Oscilloscope
  - Vertical Mode ..... Left
  - Horizontal Mode ..... B
  - B Trigger Source ..... Vert Mode
  - Intensity, Focus, Readout ..... As needed
- 7B80 Time Base
  - Time/Div ..... 5 ns
  - Mag X1
  - Triggering
    - Mode ..... P-P Auto
    - Coupling ..... AC
    - Source ..... Int
- PG502 Pulse Generator
  - Pulse Duration ..... Sq. Wave (Int Period)
    - Variable ..... X1 (ccw)
  - Period ..... ≤4 ns
    - Variable ..... For 200 MHz waveform (5 ns period) on test oscilloscope
  - Output (Volts)
    - Low level ..... +0.3 V
    - High level ..... -1.4 V
- FG501A Function Generator
  - Frequency Hz 10
  - Function ..... ∿ (triangle wave)
  - Multiplier ..... 10^5
  - Amplitude ..... 2 V (monitor display will be two divisions high)

2387-552A

E. TIME-MEASUREMENT ACCURACY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

4. Programmable Amplifier, 7A16P
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cables, 42 inch (four needed)

E1. TIME-MEASUREMENT ACCURACY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

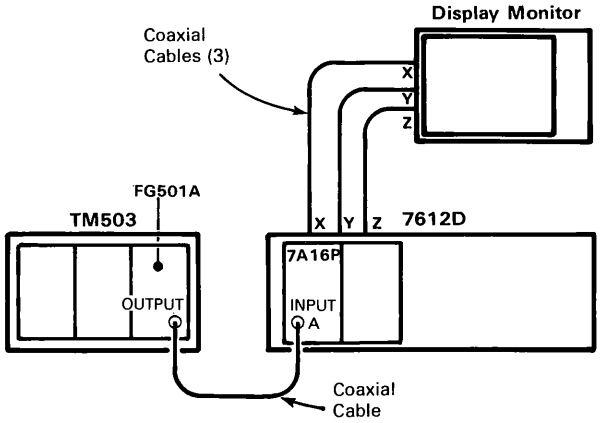
E2. CHECK ACCURACY OF TIME BASE A

NOTE

First perform step E1, then proceed.

E2. SETUP CONDITIONS

7612D Controls:
- RECORD LENGTH 1024
- TRIGGER FUNCTION
  - SLOPE ..... –
  - COUPLING ..... DC



Test Equipment Controls:

7A16P Amplifier
- Volts/Div 1
- Bandwidth ..... Full
- Polarity ..... +Up
- Input
  - Coupling ..... DC
  - Impedance 50Ω

FG501A Function Generator
- Frequency Hz 2
- Multiplier ..... 10^5
- Function ..... ⎍ (square wave)
- Amplitude ..... 2 V (monitor display will be two divisions high)

2387-553

a. While repeatedly pressing the ARM A button, adjust the FG 501A Frequency Hz control so that one complete square wave is displayed on the monitor.

b. Press the 7612D SAMPLE INTERVAL button.

c. Use the INCREMENT > button to set the sample interval to 10E-9.

d. Press the ARM A button.

e. **CHECK**—that the monitor displays two complete square waves.

f. Change the FG 501A Frequency Hz to 100 kHz.

g. Repeatedly press the ARM A button and adjust the FG 501A Frequency Hz so that one complete square wave is displayed on the monitor.

h. Press the SAMPLE INTERVAL button.

i. Use the INCREMENT > button to set the sample interval to 20E-9.

j. **CHECK**—that the monitor displays two complete square waves.

k. Repeat the procedure given in parts h, i, and j to check the time-measurement accuracies of the other sample intervals. Table 5-4 gives the sample intervals, input frequencies, and number of pulses the monitor should display.

TABLE 5-4
Inputs and Output to Check Time Measurement Accuracy

Sample Interval	Input Frequency	Pulses in Monitor Display
10E-9	100 kHz	1
20E-9	100 kHz	2
30E-9	100 kHz	3
40E-9	100 kHz	4
50E-9	100 kHz	5
60E-9	100 kHz	6
70E-9	100 kHz	7
80E-9	100 kHz	8
90E-9	100 kHz	9
100E-9	10 kHz	1
200E-9	10 kHz	2
300E-9	10 kHz	3
400E-9	10 kHz	4
500E-9	10 kHz	5
600E-9	10 kHz	6
700E-9	10 kHz	7
800E-9	10 kHz	8
900E-9	10 kHz	9
1E-6	1 kHz	1
2E-6	1 kHz	2
3E-6	1 kHz	3
4E-6	1 kHz	4
5E-6	1 kHz	5
6E-6	1 kHz	6
7E-6	1 kHz	7
8E-6	1 kHz	8
9E-6	1 kHz	9
10E-6	100 Hz	1
20E-6	100 Hz	2
30E-6	100 Hz	3
40E-6	100 Hz	4
50E-6	100 Hz	5
60E-6	100 Hz	6
70E-6	100 Hz	7
80E-6	100 Hz	8
90E-6	100 Hz	9
100E-6	10 Hz	1
200E-6	10 Hz	2
300E-6	10 Hz	3
400E-6	10 Hz	4
500E-6	10 Hz	5
600E-6	10 Hz	6
700E-6	10 Hz	7
800E-6	10 Hz	8
900E-6	10 Hz	9
1E-3	1 Hz	1
2E-3	1 Hz	2
3E-3	1 Hz	3
4E-3	1 Hz	4
5E-3	1 Hz	5
6E-3	1 Hz	6
7E-3	1 Hz	7
8E-3	1 Hz	8
9E-3	1 Hz	9
10E-3	0.1 Hz	1
20E-3	0.1 Hz	2
30E-3	0.1 Hz	3
40E-3	0.1 Hz	4
50E-3	0.1 Hz	5
60E-3	0.1 Hz	6
70E-3	0.1 Hz	7
80E-3	0.1 Hz	8
90E-3	0.1 Hz	9
100E-3	0.01 Hz	1
200E-3	0.01 Hz	2
300E-3	0.01 Hz	3
400E-3	0.01 Hz	4
500E-3	0.01 Hz	5
600E-3	0.01 Hz	6
700E-3	0.01 Hz	7
800E-3	0.01 Hz	8
900E-3	0.01 Hz	9
1E-0	0.001 Hz	1

TABLE 5-4 (cont)

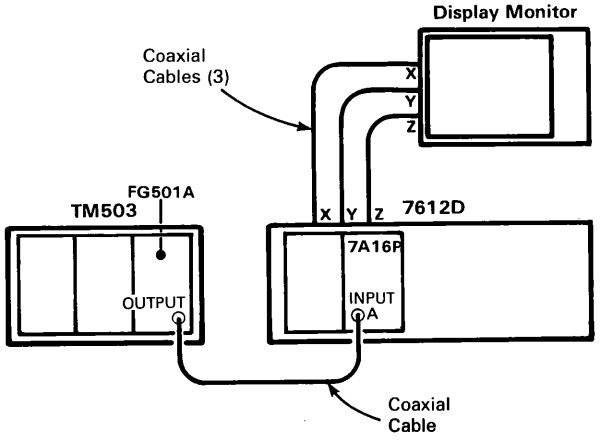
E3. CHECK ACCURACY OF TIME BASE B

NOTE

If the preceding step was not performed, first perform step E1, then proceed.

E3. SETUP CONDITIONS

7612D Controls:
- RECORD LENGTH 1024
- TRIGGER FUNCTIONS
  - SELECT ..... R
  - COUPLING ..... DC
- INSTRUMENT FUNCTION
  - PROGRAM ..... CHANNEL B



Test Equipment Controls:
- 7A16P Amplifier
  - Volts/Div 1
  - Bandwidth ..... Full
  - Polarity ..... +Up
  - Input
    - Coupling ..... DC
    - Impedance 50Ω
- FG501A Function Generator
  - Frequency Hz 2
  - Multiplier ..... 10^5
  - Function ..... ⎍ (square wave)
  - Amplitude ..... 2 V (monitor display will be two divisions high)

2387-554

a. While repeatedly pressing the ARM B button, adjust the FG 501A Frequency Hz control so that one complete square wave is displayed on the monitor.

b. Press the 7612D SAMPLE INTERVAL button.

c. Use the INCREMENT > button to set the sample interval to 10E-9.

d. Press the ARM B button.

e. **CHECK**—that the monitor displays two complete square waves.

f. Change the FG 501A Frequency Hz to 100 kHz.

g. Repeatedly press the ARM B button and adjust the FG 501A Frequency Hz so that one complete square wave is displayed on the monitor.

h. Press the SAMPLE INTERVAL button.

i. Use the INCREMENT > button to set the sample interval to 20E-9.

j. **CHECK**—that the monitor displays two complete square waves.

k. Repeat the procedure given in parts h, i, and j to check the time-measurement accuracies of the other sample intervals. Table 5-4 (see part k of Step E2. CHECK ACCURACY OF TIME BASE A) gives the sample intervals, input frequencies, and number of pulses the monitor should display.

F. MONOTONICITY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
2. Amplifier, 7A19 (two needed)
3. Differential Amplifier, 7A22 (two needed)
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cables, 42 inch (four needed)

F1. MONOTONICITY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

F2. CHECK CHANNEL A MONOTONICITY

NOTE

First perform step F1, then proceed.

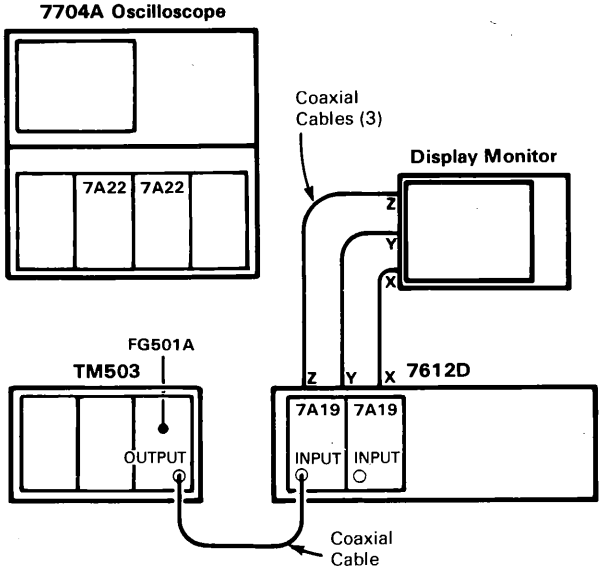
a. Connect and set the equipment as shown in F2. SETUP CONDITIONS.

b. While repeatedly pressing the ARM A button, increase the FG 501A Output Amplitude until the waveform display on the monitor reaches, and goes slightly past, either top or bottom of the display area.

c. Continue pressing the ARM A button and use the Channel A 7A19 Position control to center the waveform in the monitor's display area.

F2. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 20E-9
- PROGRAM ..... CHANNEL A
- TRIGGER FUNCTIONS
  - SELECT L
  - SLOPE ..... -
  - HF REJ ..... on



Test Equipment Controls:

7A16P Amplifiers
- Volts/Div 0.2
- Coupling ..... DC
- Polarity ..... +Up
- Position ..... Centered

FG501A Function Generator
- Frequency Hz 3
- Multiplier ..... 10^5
- Function .....
- Offset ..... Pressed in

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A22 Differential Amplifiers

	Right Vert	A Horiz
Volts/Div	2 mV	5 mV
HF -3 dB Point	0.3 MHz	0.3 MHz
LF -3 dB Point	DC Offset	DC Offset
Coupling		
+ Input	DC	DC
- Input	Gnd	Gnd

Display Monitor
- Intensity ..... For visible display

2387-555

d. Continue pressing the ARM A button and adjust the FG 501A Amplitude control until the waveform blanks equally at the top and bottom of the ramp. See Figure 5-5.

e. Set the 7704A as follows:

A Intensity ..... Visible display

f. Disconnect the X and Y cables from the monitor and connect the them to the + inputs of the test oscilloscope's A Horiz and Right Vert 7A22's, respectively.

g. Set both 7A22 Offset controls to obtain a waveform display similar to that shown in Figure 5-6a.

h. **CHECK**—that the ramp steps ascend progressively (see Fig. 5-6a) as you rotate the left and right 7A22 Offset controls with no decrease in step levels (see Fig. 5-6b) across the entire ramp.

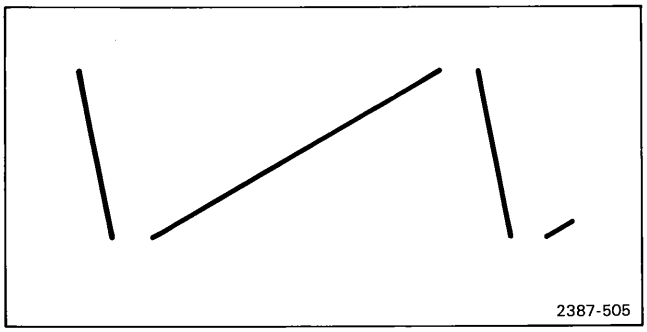


Fig. 5-5. Ramp blanked equally at top and bottom.

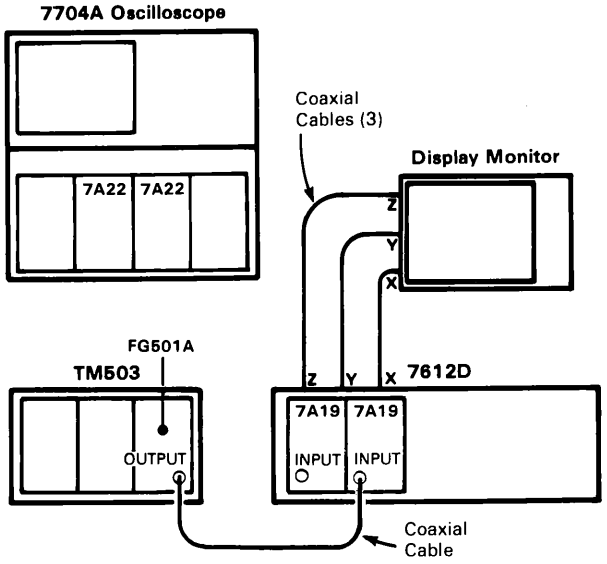
F3. CHECK CHANNEL B MONOTONICITY

NOTE

If the preceding step was not performed, first perform step F1, then proceed.

F3. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 20E-9
- PROGRAM ..... CHANNEL B
- TRIGGER FUNCTIONS
  - SELECT ..... R
  - SLOPE .....
  - HF REJ ..... on



Test Equipment Controls:

7A16P Amplifiers
- Volts/Div 2
- Coupling ..... DC
- Polarity ..... +Up
- Position ..... Centered

FG501A Function Generator
- Frequency Hz 3
- Multiplier ..... 10^5
- Function .....
- Offset ..... Pressed in

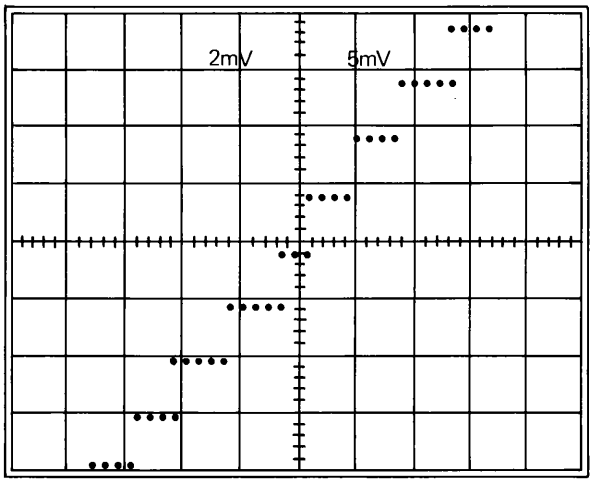
7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A22 Differential Amplifiers

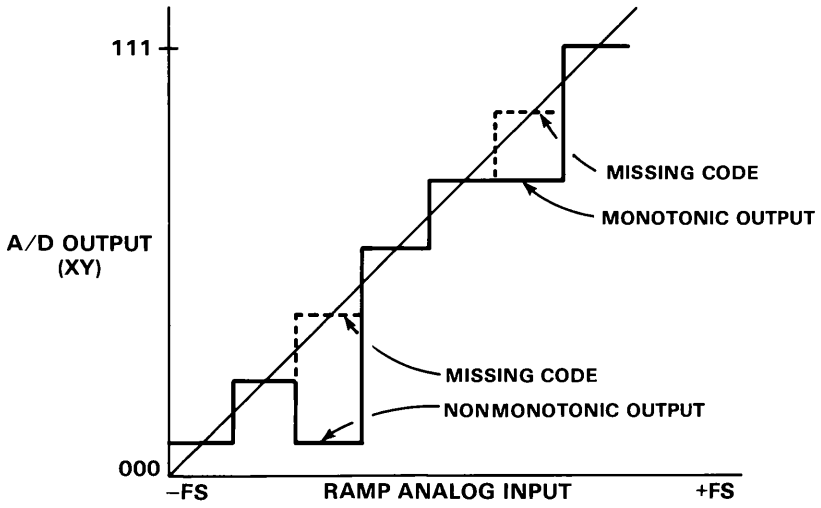
	Right Vert	A Horiz
Volts/Div	2 mV	5 mV
HF -3 dB Point	0.3 MHz	0.3 MHz
LF -3 dB Point	DC Offset	DC Offset
Coupling		
+ Input	DC	DC
- Input	Gnd	Gnd

Display Monitor
- Intensity ..... For visible display

2387-556



a. Monotonic XY output display.



b. Nonmonotonic output.

2387-506

Fig. 5-6. Monotonic and nonmonotonic outputs.

a. While repeatedly pressing the ARM B button, increase the FG 501A Amplitude until the waveform displayed on the monitor reaches, and goes slightly past, either top or bottom of the display area.

b. Continue pressing the ARM B button and use the Channel B 7A19 Position control to center the waveform in the monitor's display area.

c. Continue pressing the ARM B button and adjust the FG 501A Amplitude control until the waveform blanks equally at top and bottom of the ramp. See Figure 5-5 in step F2.

d. Disconnect the X and Y cables from the monitor and connect them to the + inputs of the test oscilloscope's A Horiz and Right Vertical 7A22s respectively.

e. Set both 7A22 Offset controls to obtain a waveform display similar to that shown in Figure 5-6a in step F2.

f. **CHECK**—that the ramp steps ascend progressively (see Fig. 5-6a) as you rotate the left and right 7A22 Offset controls with no decrease in step levels (see Fig. 5-6b) across the entire ramp.

G. VERTICAL

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
6. Time Base, 7B80
14. Sine-Wave Generator, SG 503
15. Power Module Mainframe, TM 503
17. Coaxial Cable, 42 inch (three needed)
18. Coaxial Cable, 36 inch
19. Calibration Fixture

G1. VERTICAL PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

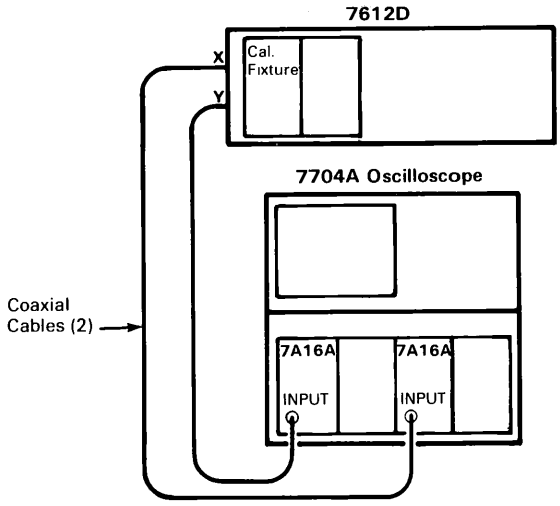
G2. CHECK CHANNEL A CENTERING

NOTE

First perform step G1, then proceed.

G2. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

Calibration Fixture
Test ..... Vert or Horiz Com Mode

7704A Oscilloscope
Test ..... Aux In
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Polarity	+Up	+Up
Position	9 o'clock	Centered

2387-557A

a. Connect the output of the SG 503 to the aux in connector on the calibration fixture with a coaxial cable.

b. Set the SG 503 as follows:

Frequency . . . . . 50 kHz
Output Amplitude . . . . . 600 mV
Amplitude Multiplier X1

c. While repeatedly pressing the 7612D ARM A button, adjust the left vertical 7A16A position and variable volts/div controls to obtain a clipped sine-wave display eight divisions high (Fig. 5-9a shows the desired waveform).

d. Disconnect the signal from the calibration fixture.

e. Set the calibration fixture to vert or horiz com mode.

f. Press ARM A.

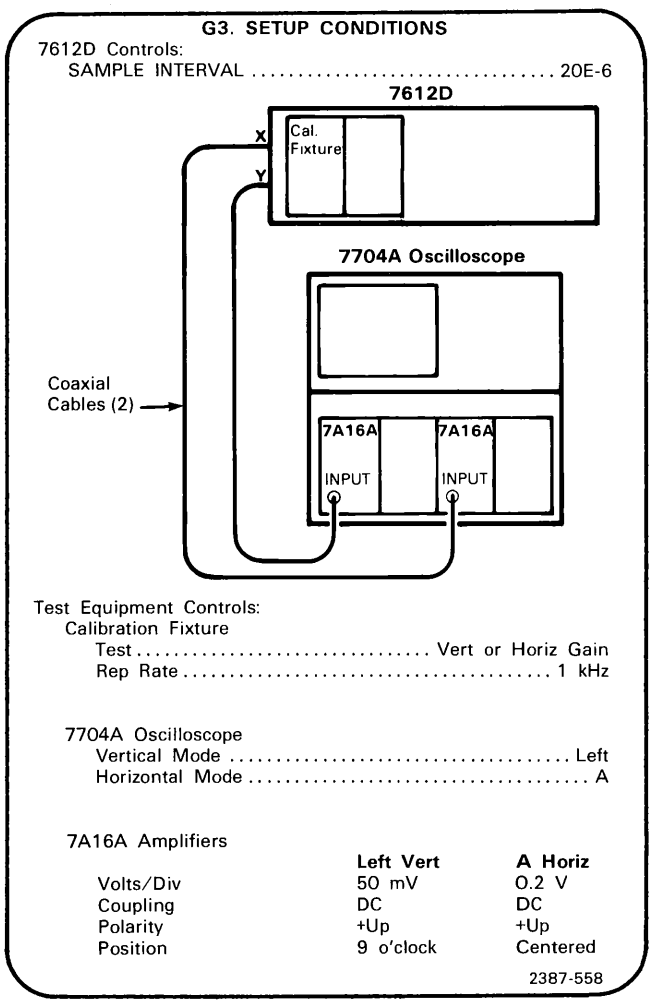
g. Press MAN TRIG.

h. **CHECK**—that the trace on the test oscilloscope is at graticule center +0.75 minor divisions (+5 LSBs).

G3. CHECK CHANNEL A GAIN

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. Press the SAMPLE INTERVAL button.

b. Use the DECREMENT/INCREMENT controls to set the A SAMPLE INTERVAL to 20E-6.

c. Press the COPY button.

d. Press the ARM A button.

e. Use the left vertical 7A16A Position control to set the bottom of the staircase waveform to the bottom graticule line.

f. Move the left vertical 7A16 Variable Volts/Div control to set the top staircase step at the top graticule line. See Figure 5-7.

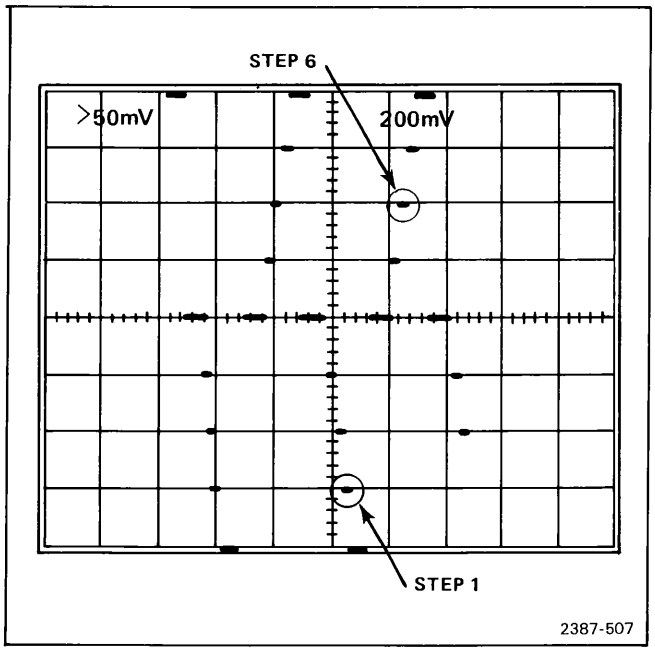


Fig. 5-7. Display of staircase waveform with its top and bottom steps set to the top and bottom graticule lines.

g. Observe that the longest lines are at the center graticule line on the test oscilloscope.

h. If the longest lines do not align with the center graticule line, repeatedly press the ARM A button while adjusting the calibration fixture Position control to bring the longest lines to the center graticule line.

i. **CHECK**—that each of the marks from −3 divisions to +3 divisions aligns with the appropriate graticule line (see Fig. 5-7).

j. Use the left 7A16A Position control to align the first stairstep with the first graticule line (see Fig. 5-7).

k. **CHECK**—that the sixth step aligns with the sixth graticule line, + or −0.1 division (see Fig. 5-7).

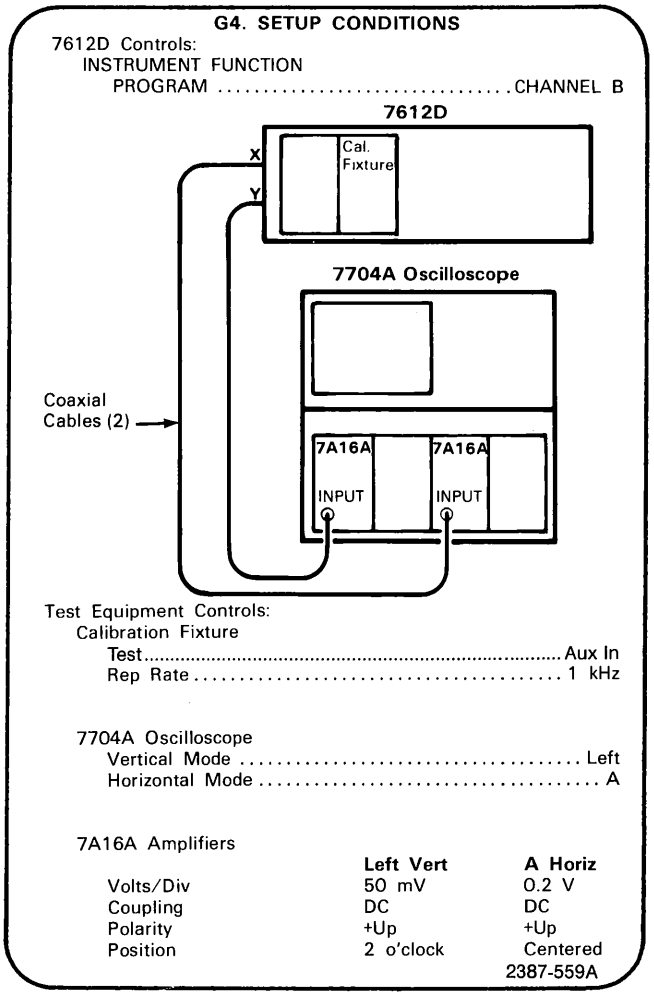
NOTE

This CHECK will verify that the gain is within ±2% of specified value.

G4. CHECK CHANNEL B CENTERING

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. Connect the output of the SG 503 to the aux in connector on the calibration fixture with a coaxial cable.

b. Set the SG 503 as follows:

Frequency ..... 50 kHz
Output Amplitude ..... 600 mV
Amplitude Multiplier X1

c. While repeatedly pressing the 7612D ARM B button, adjust the left vetical 7A16A position and variable volts/div controls to obtain a clipped sine-wave display eight divisions high (Fig. 5-9a shows the desired waveform).

d. Disconnect the signal from the calibration fixture.

e. Set the calibration fixture to vert or horiz com mode.

f. Press the ARM B button.

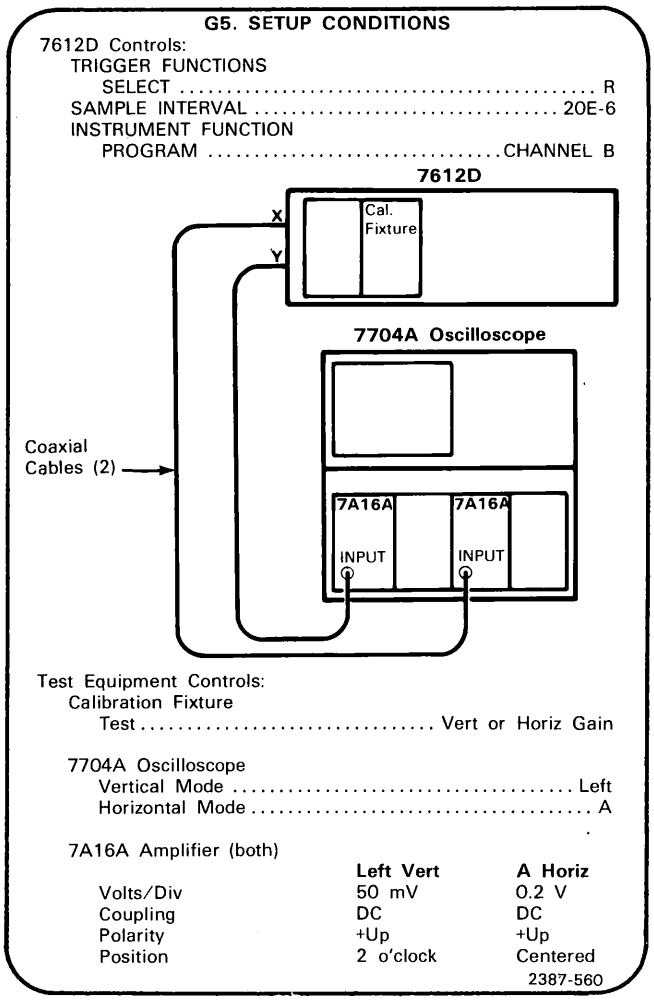
g. Press the MAN TRIG button.

h. **CHECK**—that the trace on the test oscilloscope is at graticule center + or −0.75 minor divisions (+ or − five LBSs)

G5. CHECK CHANNEL B GAIN

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. Press the SAMPLE INTERVAL button.

b. Press the PROGRAM CHANNEL B button.

c. Use the DECREMENT/INCREMENT controls to set the B SAMPLE INTERVAL to 20E-6.

d. Press the ARM B button.

e. Use the 7A16A Position control to set the top of the staircase waveform to the top graticule line.

f. Move the 7A16A Variable Volts/Div control to set the bottom staircase step at the bottom graticule line. See Figure 5-8.

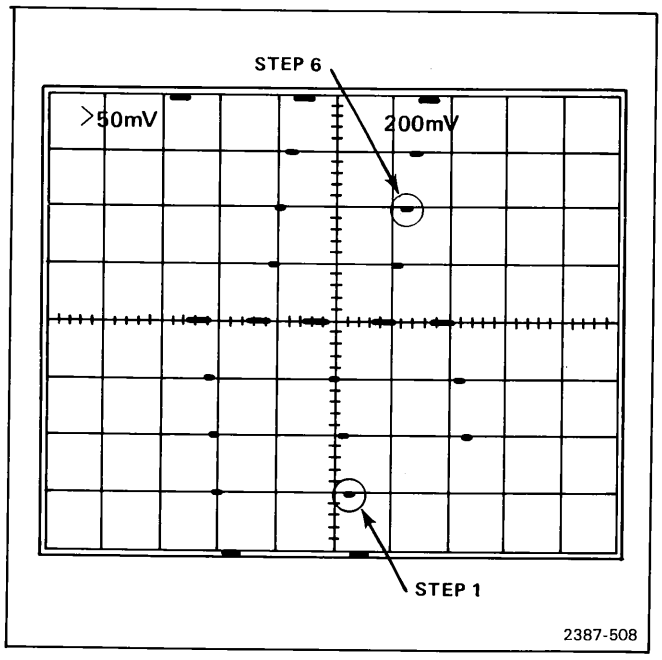


Fig. 5-8. Display of staircase waveform with its top and bottom steps set to the top and bottom graticule lines.

g. Observe that the longest lines are at the center graticule line on the test oscilloscope.

h. If the longest lines do not align with the center graticule line, repeatedly press the ARM B button while adjusting the calibration fixture Position control to bring the longest lines to the center graticule line.

i. **CHECK**—that each of the marks from −3 divisions to +3 divisions aligns with the appropriate graticule line.

j. Use the 7A16A Position control to align the first stairstep with the first graticule line (see Fig. 5-8).

k. **CHECK**—that the sixth step aligns with the sixth graticule line, + or − 0.1 division (see Fig. 5-8).

NOTE

This CHECK will verify that the gain is within ±2% of specified value.

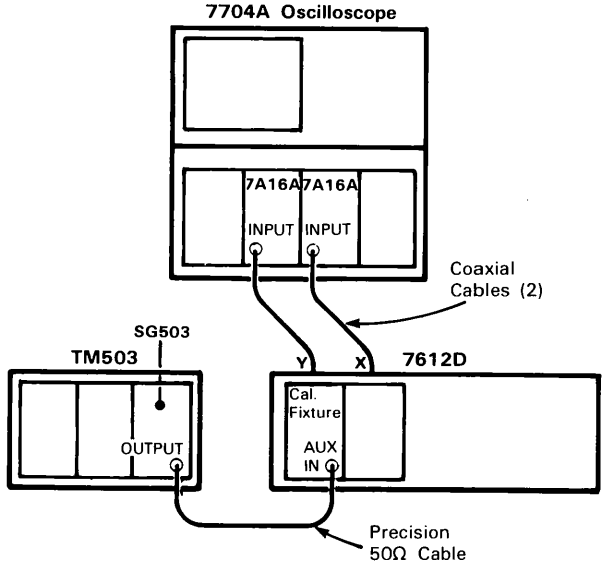
G6. CHECK CHANNEL ISOLATION

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G6. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 50E-9



Test Equipment Controls:

Calibration Fixture
- Test ..... Vert or Horiz Freq Resp
- Position ..... Centered
- Amplitude ..... Fully clockwise

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifiers
- Volts/Div ..... 50 mV
- Coupling ..... DC
- Polarity ..... +Up
- Bandwidth ..... Full

SG503 Leveled Sine Wave Generator
- Frequency Range MHz ..... Ref ≈ .05
- Frequency Variable ..... To cause Frequency MHz to read .050
- Amplitude Multiplier X1
- Outputs Amplitude
  - Volts P-P 0.6

2387-561

a. While repeatedly pressing the 7612D ARM A button, adjust the right vertical 7A16A Position and Variable Volts/Div to obtain a clipped sine-wave display as shown in Figure 5-9a. The display should be eight divisions high.

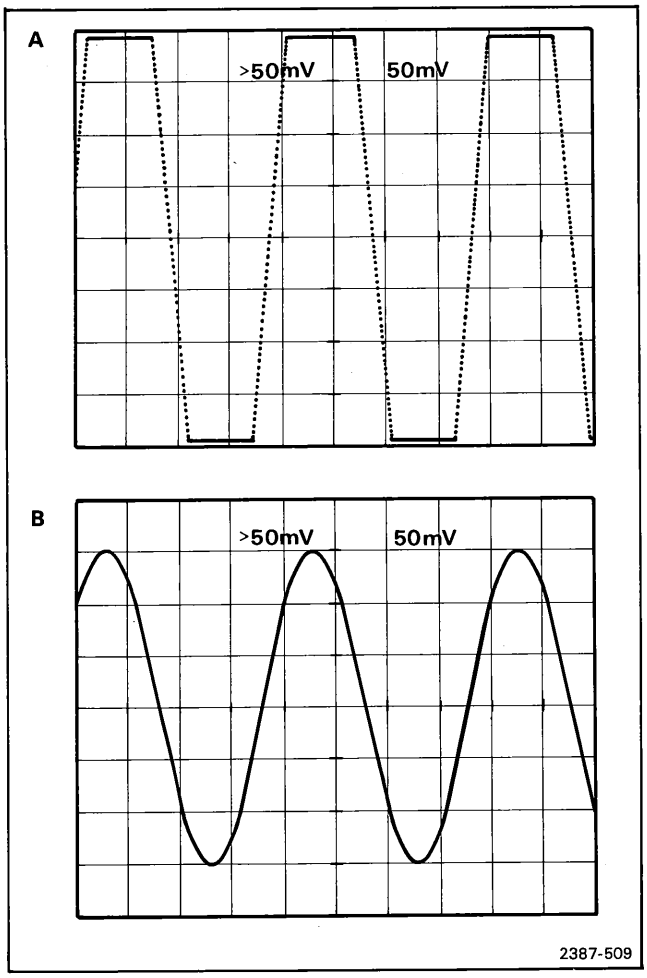


Fig. 5-9. Vertical setup waveforms.

b. Repeatedly press the 7612D ARM A button and adjust the calibration fixture Amplitude and, if necessary, Position control(s) to obtain a centered six-division display as shown in Figure 5-9b.

c. Set the SG 503 to 75 MHz.

d. Set the 7612D SAMPLE INTERVAL to 200E-9.

e. Press the 7612D ARM A button, and adjust the right vertical 7A16A Position control to bring the 7612D's Channel B trace on screen. (The Channel B trace will be below the sine-wave display on Channel A.)

f. **CHECK**—that the amplitude of the Channel B signal is 1.5 minor divisions or less.

g. Turn off the 7612D.

h. Set the SG 503 to 50 kHz.

i. Move the calibration fixture from Channel A to Channel B.

j. Turn the 7612D on, and set it as follows:

INSTRUMENT FUNCTION
PROGRAM . . . . . CHANNEL B
TRIGGER FUNCTIONS
SELECT . . . . . R
SAMPLE INTERVAL. 50E-9

k. Set the calibration fixture Amplitude control fully clockwise.

l. While repeatedly pressing the 7612D ARM B button, adjust the right vertical 7A16A Position and Variable Volts/Div controls to obtain a clipped sine-wave display as shown in Figure 5-9a. The display should be eight divisions high.

m. Repeatedly press the 7612D ARM B button and adjust the calibration fixture Amplitude and, if necessary, Position control(s) to obtain a centered six-division display as shown in Figure 5-9b.

n. Set the SG 503 to 75 MHz.

o. Set the 7612D SAMPLE INTERVAL to 200E-9.

p. Press the 7612D ARM B button and adjust the right vertical 7A16A Position control to bring the 7612D's Channel A trace on screen. (The Channel A trace will be above the sine-wave display on Channel B.)

q. **CHECK**—that the amplitude of the Channel A signal is 1.5 minor divisions or less.

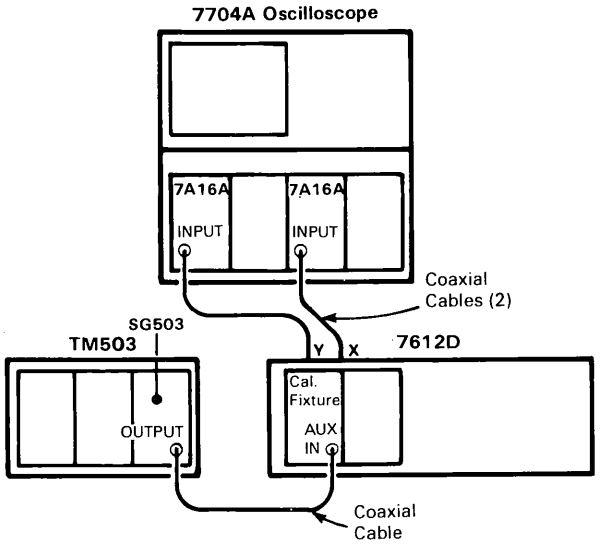
G7. CHECK CHANNEL A BANDWIDTH

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G7. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 2E-6



Test Fixture Controls:
Calibration Fixture
Test ..... Vert or Horiz Freq Resp
Position ..... Centered

SG503 Leveled Sine Wave Generator
Frequency Range (MHz) ..... Ref ≈.05
Amplitude Multiplier X.1
Output Amplitude Volts P-P .....Turn clockwise from zero until cw leveled indicator on Calibration Fixture Lights, then advance the Output Amplitude Volts P-P 0.1 V.

7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	+Up

2387-562

a. Press the ARM A button.

b. Use the Position control on the left vertical 7A16A to center the display on the test oscilloscope.

c. Use the Variable Volts/Div control on the left vertical 7A16A to set the display for six divisions of amplitude; then re-center the display with the Position control.

d. Set the SG 503 Frequency to 20.0 MHz, press the ARM A button, and check that the CW Leveled indicator on the calibration fixture is lit.

e. **CHECK**—for at least 4.2 vertical divisions of signal.

f. Set the SG 503 Frequency to 40.0 MHz, check that the CW Leveled indicator is lit, and press the ARM A button.

g. **CHECK**—for at least 4.2 vertical divisions of signal.

h. Set the SG 503 Frequency to 60.0 MHz, check that the CW Leveled indicator is lit, and press the ARM A button.

i. **CHECK**—for at least 4.2 vertical divisions of signal.

j. Set the SG 503 Frequency to 80.0 MHz, check that the CW Leveled Indicator is lit, and press the ARM A button.

k. **CHECK**—for at least 4.2 vertical divisions of signal.

l. Set the SG 503 Frequency to 90.0 MHz, check that the CW Leveled Indicator is lit, and press the ARM A button.

m. **CHECK**—for at least 4.2 vertical divisions of signal.

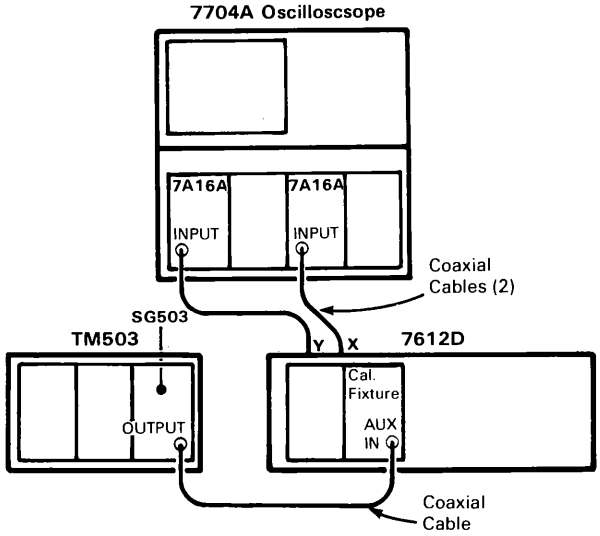
G8. CHECK CHANNEL B BANDWIDTH

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G8. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 2E-6



Test Fixture Controls:
Calibration Fixture
Test ..... Vert or Horiz Freq Resp
Position ..... Centered

SG503 Leveled Sine Wave Generator
Frequency Range (MHz) ..... Ref ≈.05
Amplitude Multiplier X.1
Output Amplitude Volts P-P .....Turn clockwise from zero until CW leveled indicator on Calibration Fixture lights, then advance the Output Amplitude Volts P-P 0.1 V.

7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	+Up

2387-563

a. Press the ARM B button.

b. Use the Position control on the left vertical 7A16A to center the display on the test oscilloscope.

c. Use the Variable Volts/Div Control on the left vertical 7A16A to set the display to be six divisions in amplitude; then re-center the display with the Position control.

d. Set the SG 503 Frequency to 20.0 MHz, press the ARM B button, and check that the CW Leveled indicator on the calibration fixture is lit.

e. **CHECK**—for at least 4.2 vertical divisions of signal.

f. Set the SG 503 Frequency to 40.0 MHz, check that the CW Leveled indicator is lit, and press the ARM B button.

g. **CHECK**—for at least 4.2 vertical divisions of signal.

h. Set the SG 503 Frequency to 60.0 MHz, check that the CW Leveled indicator is lit, and press the ARM B button.

i. **CHECK**—for at least 4.2 vertical divisions of signal.

j. Set the SG 503 Frequency to 80.0 MHz, check that the CW Leveled Indicator is lit, and press the ARM B button.

k. **CHECK**—for at least 4.2 vertical divisions of signal.

l. Set the SG 503 Frequency to 90.0 MHz, check that the CW Leveled Indicator is lit, and press the ARM B button.

m. **CHECK**—for at least 4.2 vertical divisions of signal.

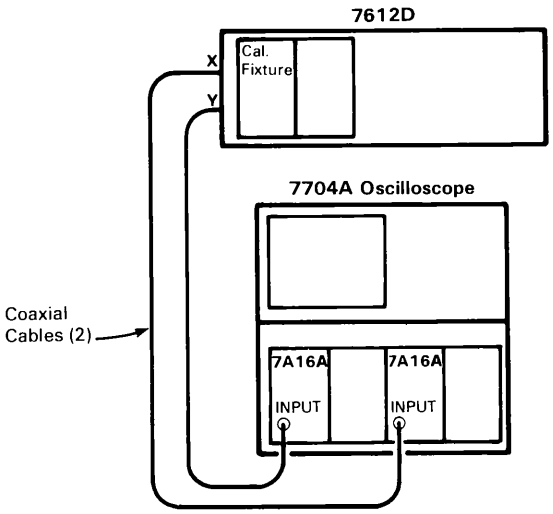
G9. CHECK CHANNEL A ABERRATION

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G9. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 5E-9



Test Equipment Controls:
7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	+Up

Calibration Fixture
Test ..... Vert or Horiz + Step Resp
Rep Rate ..... 1 MHz
Position, Amplitude ..... To produce six-division square wave centered on 7704A display. Press ARM A repeatedly while setting Position and Amplitude.

2387-564A

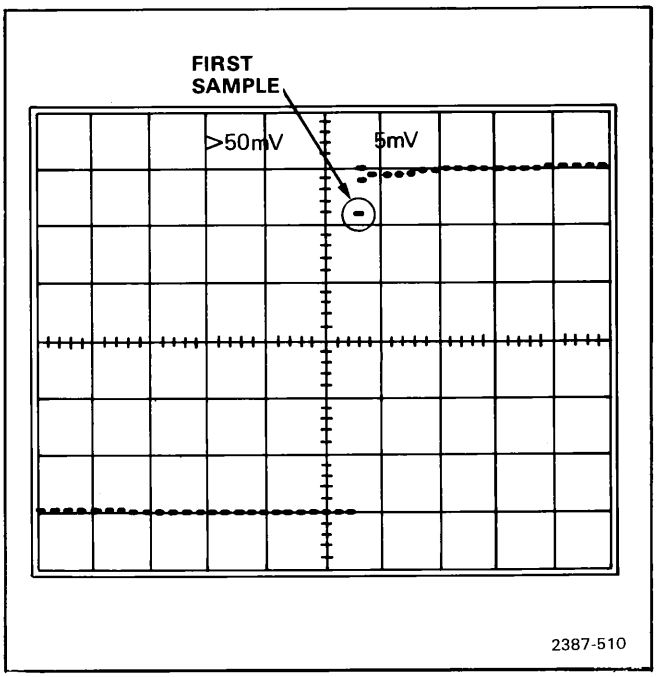


Fig. 5-10. Aberration waveform showing undershoot on front cover.

a. Change the A Horiz 7A16A Volts/Div to 10 mV and center the waveform front corner to obtain a display similar to that shown in Figure 5-10.

b. Press ARM A repeatedly to display samples of the aberrations on the waveform front corner.

NOTE

Figure 5-10 is an example of a waveform that is just withing the −4% undershoot tolerance. The first sample dot is ignored in Figure 5-10.

c. **CHECK**—that the front corner overshoot and undershoot does not exceed +1.2, −1.2 minor vertical graticule divisions (+4, −4%).

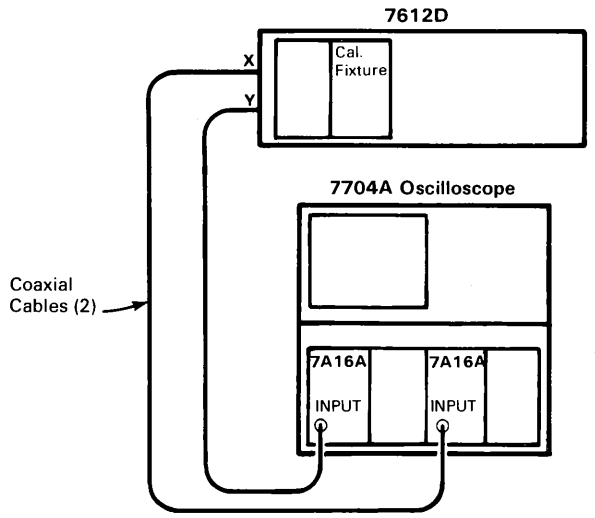
G10. CHECK CHANNEL B ABERRATION

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G10. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7704A Oscilloscope

Vertical Mode	Left
Horizontal Mode	A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	+Up

Calibration Fixture

Test	Vert or Horiz + Step Resp
Rep Rate	1 MHz
Position, Amplitude	To produce six-division square wave centered on 7704A display. Press ARM A repeatedly while setting Position and Amplitude.

2387-565

a. Change the A Horiz 7A16A Volts/Div to 10 mV and center the waveform front corner to obtain a display similar to that shown in Figure 5-10 in step G9.

b. Press the ARM B button repeatedly to display samples of the aberrations on the waveform front corner.

NOTE

Figure 5-10 is an example of a waveform that is just within the −4% undershoot tolerance. The first dot is ignored in Figure 5-10.

c. **CHECK**—that the front corner undershoot does not exceed +1.2 or −1.2 minor graticule divisions (±4%).

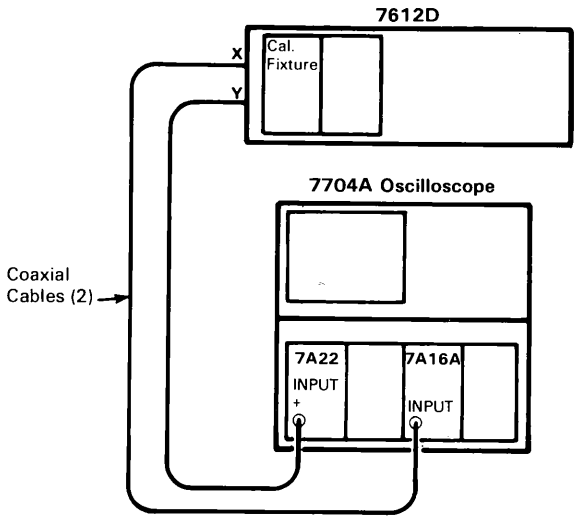
G11. CHECK CHANNEL A LOW-FREQUENCY STEP RESPONSE

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G11. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... A

7A22 Differential Amplifier
- Volts/Div ..... 50 mV
- HF -3 dB Point ..... 1 MHz
- LF -3 dB Point ..... DC
- Coupling ..... DC

7A16A Amplifier
- Volts/Div ..... 0.1 V
- Polarity ..... +Up
- Coupling ..... DC
- Bandwidth ..... Full

Calibration Fixture
- Test ..... Vert or Horiz Step Resp
- Rep Rate ..... 10 Hz
- Position } ..... To produce a five-division display centered on the 7704A display. Press ARM A repeatedly while adjusting Position and Amplitude.
- Amplitude }

2387-566

a. Set the 7A22 Volts/Div to 5 mV and the LF −3 dB Point to DC Offset.

b. Set the 7A22 Coarse and Fine Offset to view the top of the pulse.

c. **CHECK**—for not over one-half major division (1%) of tilt.

d. Change the calibration fixture Rep Rate to 100 Hz and the 7612D SAMPLING INTERVAL to 10E-6. Press ARM A.

e. **CHECK**—for not over one-half major division of tilt.

f. Change the calibration fixture Rep Rate to 1 kHz and the 7612D SAMPLE INTERVAL to 1E-6. Press ARM A.

g. **CHECK**—for not over one-half major division of tilt.

h. Change the calibration fixture Rep Rate to 10 kHz and the 7612D SAMPLING INTERVAL to 100E-9. Press ARM A.

i. **CHECK**—for not over one-half major division of tilt.

j. Change the calibration fixture Rep Rate to 100 kHz and the 7612D SAMPLING INTERVAL to 10E-9. Press ARM A.

k. **CHECK**—for not over one-half major division of tilt.

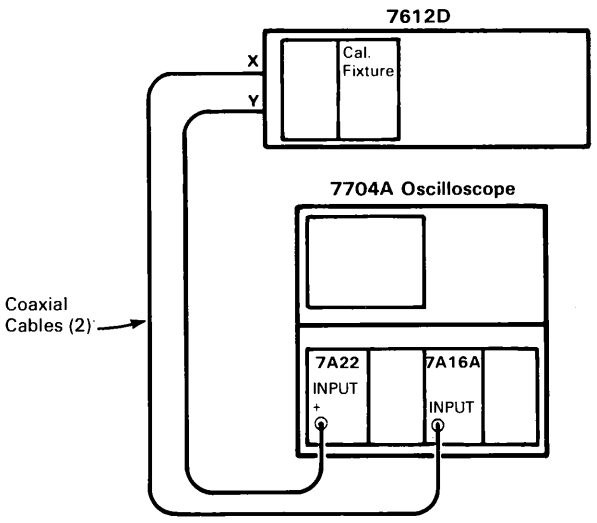
G12. CHECK CHANNEL B LOW-FREQUENCY STEP RESPONSE

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G12. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 100E-6
- TRIGGER FUNCTIONS
  - SELECT ..... R
- INSTRUMENT FUNCTION
  - PROGRAM ..... CHANNEL B



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... A

7A22 Differential Amplifier
- Volts/Div ..... 50 mV
- HF -3 dB Point ..... 1 MHz
- LF -3 dB Point ..... DC
- Coupling ..... DC

7A16A Amplifier
- Volts/Div ..... 0.1 V
- Polarity ..... +Up
- Coupling ..... DC
- Bandwidth ..... Full

Calibration Fixture
- Test ..... Vert or Horiz Step Resp
- Rep Rate ..... 10 Hz
- Position, Amplitude ..... To produce a five-division display centered on the 7704A display. Press ARM B repeatedly while adjusting Position and Amplitude.

2387-567

a. Move the calibration fixture from CHANNEL A to CHANNEL B of the 7612D.

b. Press PROGRAM CHANNEL B and SELECT R buttons.

c. Set the 7A22 Volts/Div to 5 mV and set its LF—3 dB Point to DC Offset.

d. Set the 7A22 Coarse and Fine Offset controls to bring the top of the pulse on the oscilloscope screen.

e. Press the ARM B button.

f. **CHECK**—for not over one-half major division of tilt.

g. Change the calibration fixture Rep Rate to 100 Hz and the 7612D SAMPLING INTERVAL to 10E-6. Press the ARM B button.

h. **CHECK**—for not over one-half major division of tilt.

i. Change the calibration fixture Rep Rate to 1 kHz and the 7612D SAMPLING INTERVAL to 1E-6. Press the ARM B button.

j. **CHECK**—for not over one-half major division of tilt.

k. Change the calibration fixture Rep Rate to 10 kHz and the 7612D SAMPLING INTERVAL to 100E-9. Press the ARM B button.

l. **CHECK**—for not over one-half major division of tilt.

m. Change the calibration fixture Rep Rate to 100 kHz and the 7612D SAMPLING INTERVAL to 10E-9. Press the ARM B button.

n. **CHECK**—for not over one-half major division of tilt.

o. Disconnect the test oscilloscope and remove the calibration fixture.

H. POWER SUPPLY REMOTE CONTROL

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
11. Digital Multimeter, DM 501A
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
17. Coaxial Cables, 42 inch (four needed)
20. Adapter, bnc "T" (two needed)
21. Adapter, bnc female to dual banana plug

H1. POWER SUPPLY REMOTE CONTROL PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

H2. CHECK REMOTE ACTUATE INPUT

NOTE

First perform step H1, then proceed.

a. Connect and set the equipment as shown in H2. SETUP CONDITIONS.

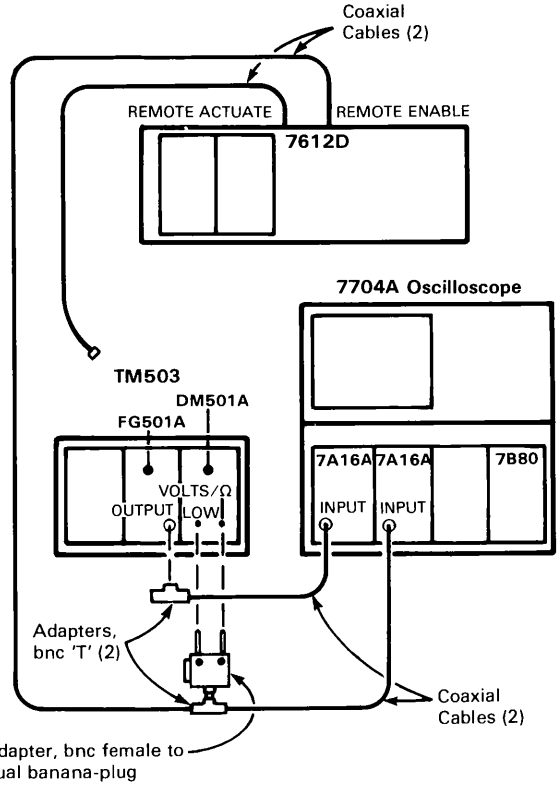
b. Set the FG 501A Frequency Multiplier to 10^{-1}.

c. Set the 7704A Vertical Mode to Chop.

d. Set the input coupling switches on both 7A16A Amplifiers to GND.

H2. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- Trigger Source ..... Left Vert

7A16A Amplifiers

	Left	Right
Volts/Div	1	5
Coupling	DC	DC

7B80 Time Base
- Time/Div ..... 5 mS
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... Int

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^2
- Function ..... ⌐ (square wave)
- Amplitude ..... To produce square wave of 1.6 V p-p
- Offset ..... To set negative excursion of square wave to +0.5 V. Result should be square wave between +0.5 V and +2.1 Vdc.

DM501A Digital Multimeter
- kΩ ..... pressed in
- Input ..... Ext
- Range ..... 2 kΩ

In this test the DM501A acts as a current source for a pull-up on the 7612D REMOTE ENABLE input. Any current source of less than 16 mA will work. For example, a 1 kΩ resistor connected to the +5 V will provide 5 mA.

2387-568

e. Set both oscilloscope traces to graticule center.

f. Set both 7A16A input coupling switches to DC.

g. Set the time base to Norm triggering and 50 ms/div.

h. Connect the coaxial cable from the 7612D REMOTE ACTUATE connector to the bnc T on the FG 501A output.

i. **CHECK**—that the 7612D powers on, then off at the FG 501A frequency (about five seconds on, five seconds off).

H3. CHECK REMOTE ENABLE OUTPUT

NOTE

If the preceding step was not performed, first perform step H1, then proceed.

a. Connect and set the equipment as shown in H3. SETUP CONDITIONS.

b. Set the FG 501A Multiplier to 10^{-1}.

c. Set the input coupling switches on both 7A16A Amplifiers to GND.

d. Set both oscilloscope traces to graticule center.

e. Set both 7A16A input coupling switches to DC.

f. Set the time base to Norm trigger mode and 50 mV/div.

g. Connect the coaxial cable from the FG 501A output to the 7612D REMOTE ACTUATE input.

h. **CHECK**—that the REMOTE ENABLE waveform (on the right 7A16A) switches high between 150 ms and 250 ms after the ACTUATE waveform switches high. Because the time base is triggered by the left vertical (REMOTE ACTUATE) signal, its transition will not be visible. (For best triggering, the time base trigger slope should be set to +, and the trigger level should be just on the + side of zero.) Figure 5-11 shows the test oscilloscope display.

i. **CHECK**—that the low part of the REMOTE ENABLE waveform is within 0.8 V of the ground reference level.

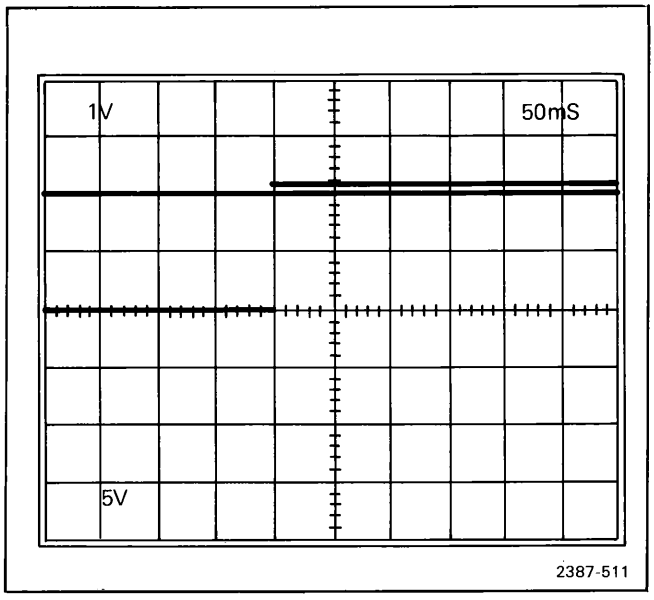
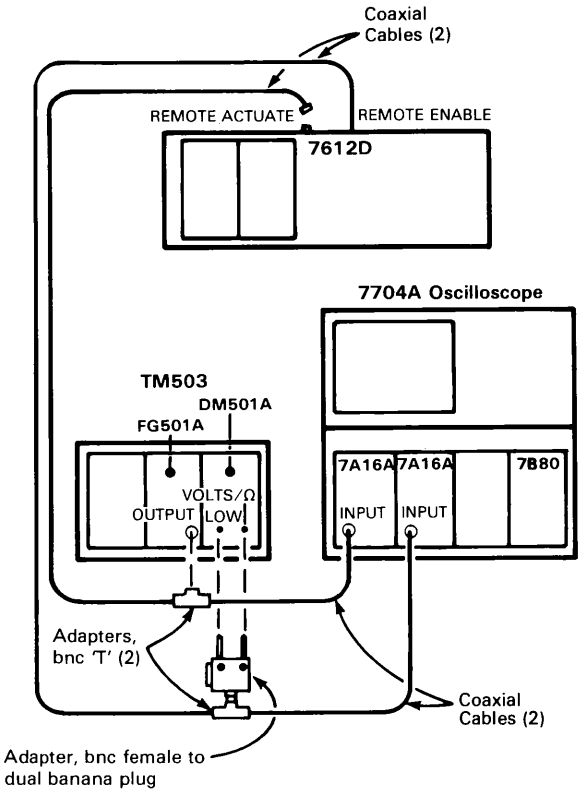


Fig. 5-11. The REMOTE ENABLE output check display.

H3. SETUP CONDITIONS

7612D Controls:
Make no changes to control settings.



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Chop
- Horizontal Mode ..... B
- Trigger Source ..... Left Vert

7A16A Amplifiers

	Left	Right
Volts/Div	1	5
Coupling	DC	DC

7B80 Time Base
- Time/Div ..... 5 mS
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... Int

FG501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^2
- Function ..... (square wave)
- Amplitude ..... To produce square wave of 1.6 V p-p.
- Offset ..... To set negative excursion of square wave to +0.5 V. Result should be square wave between +0.5 V and −2.1 Vdc.

DM501A Digital Multimeter
- kΩ ..... pressed in
- Input ..... Ext
- Range ..... 2 kΩ

In this test the DM501A acts as a current source for a pull-up on the 7612D REMOTE ENABLE input. Any current source of less than 16 mA will work. For example, a 1 kΩ resistor connected to +5 V will provide 5 mA.

2387-569

I. EXTERNAL CONNECTORS

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

11. Digital Multimeter, DM 501A
15. Power Module Mainframe, TM 503
17. Coaxial Cable, 42 inch
24. Shorting Cap

I1. EXTERNAL CONNECTORS PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure, which appears at the beginning of Part I—Performance Check.

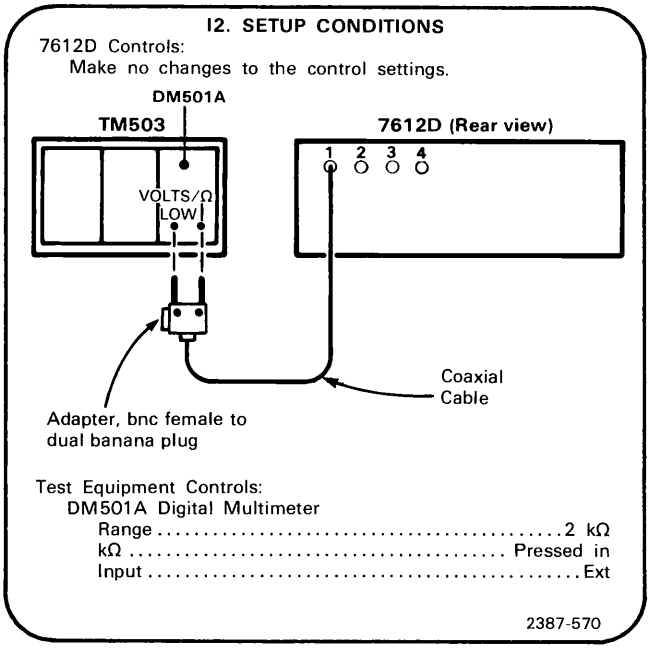
b. Leave the programmable parameters in their power-up conditions, as listed in the Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

I2. CHECK CONTINUITY BETWEEN FRONT- AND REAR-PANEL CONNECTORS

NOTE

First perform step I1, then proceed.



a. Put the shorting cap on bnc connector no. 1 on the 7612D front panel.

b. **CHECK**—that the digital multimeter indicates continuity.

c. Repeat parts a and b for bnc connectors 2, 3, and 4.

PART II—ADJUSTMENT AND PERFORMANCE CHECK

The following procedure (Part II—Adjustment and Performance Check) provides the information necessary to: (1) verify that the instrument meets the electrical specifications, (2) verify that the controls function properly, and (3) perform all internal adjustments.

Part I—Performance Check verifies electrical specifications without making internal adjustments. All tolerances given are as specified in the Specification tables (section 1) in this manual).

See Table 5-1, Calibration Procedure Electives, at the beginning of this section, for information on performing a Partial Part I—Performance Check procedure.

INDEX TO PART II—ADJUSTMENT AND PERFORMANCE CHECK

ADJUSTMENT AND PERFORMANCE CHECK
INITIAL SETUP PROCEDURE

NOTE

The performance of the 7612D can be checked at any ambient temperature from 0° C to +40° C unless otherwise stated. Adjustments must be performed at an ambient temperature from +20° C to +30° C for specified accuracies.

1. Before starting calibration, thoroughly clean and inspect the 7612D. Correct any problems before continuing.

2. Check that the Line Voltage Selector is set for the nominal line voltage available, and connect a suitable power cord to the power input connector. If the nominal line voltage is not within the two ranges of the Line Voltage Selector, use a variable autotransformer to provide the desired voltage. Be sure the safety-earth ground path is intact so that the 7612D chassis is connected directly to ground via the power cord.

3. Set the rear-panel PRINCIPAL POWER SWITCH to ON.

4. Turn the 7612D on by pressing the front-panel ON/OFF button. (It will light when power is applied to the instrument.) Allow at least 30 minutes warmup before proceeding.

5. Power-up conditions for the programmable parameters are:

RECORD LENGTH 2048
NO OF RECORDS 1
BREAKPOINT LOCATION 0000
SAMPLE INTERVAL 5E-9
SAMPLES 00
TRIGGER FUNCTIONS
  SELECT L
  SOURCE . . . . . INT
  SLOPE . . . . . +
  COUPLING . . . . . AC
  HF REJ . . . . . OFF
TRIGGER LEVEL 00
INSTRUMENT FUNCTION
  PROGRAM . . . . . CHANNEL A
  CLK . . . . . INT

6. Remove the 7612D covers only as necessary and replace them as soon as possible. With the covers off, air is not routed through the instrument properly, causing some parts to overheat.

7. Turn off power when removing or installing plug-in units, then allow a short time for the 7612D to stabilize when it is turned on.

8. The 7612D front and rear-panel controls and connectors are spelled and capitalized in this procedure as they appear on the instrument. Internal adjustments are initial capitalized as they appear in the diagrams section.

9. The display monitor may remain connected throughout the procedure.

10. Be sure the test oscilloscope is operating correctly at all times. Check and adjust the test oscilloscope front-panel gain and sweep calibration and the compensation of all probes before beginning and at any point in the procedure where the plug-in units or probes are changed.

A. POWER SUPPLY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

10. Test Leads for DMM
11. Digital Multimeter, DM 501A
15. Power Module Mainframe, TM 503

A1. POWER SUPPLY PRELIMINARY SETUP

a. Remove the bottom and left side covers.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up condition, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS A page in Section 8, Diagrams and Circuit Board Illustrations.

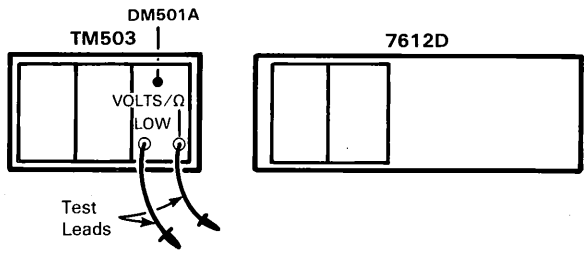
A2. CHECK/ADJUST −5.2 V

NOTE

First perform step A1, then proceed.

A2. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:
DM 501A Digital Multimeter
Volts ..... DC
Input ..... EXT
Range ..... 20 V

2387-571

a. Connect the multimeter leads to J500 on bottom of the A68 Main Interconnect Board as follows:

Low ..... Pin 5 (common)
Volts/Ω ..... Pin 4 (−5.2 V)

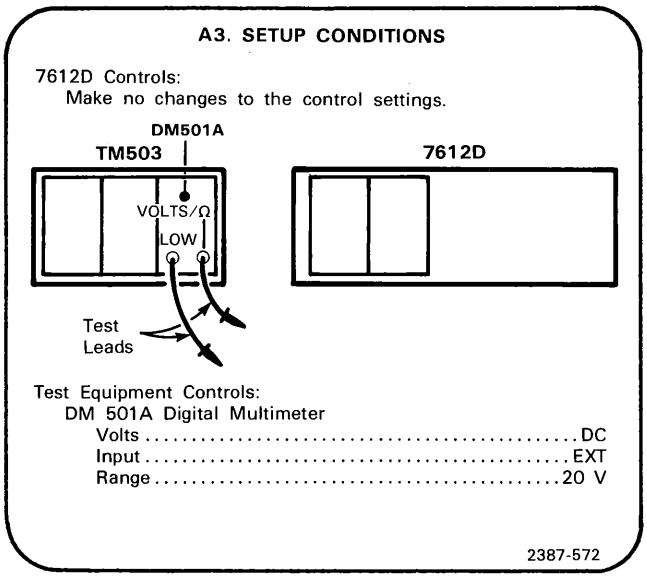
b. **CHECK**—that the digital multimeter reads −5.252 to −5.148 V.

c. **ADJUST**—5.2 V (R521), on the A82 Control Board for −5.2 V. Access to R521 is through a hole in the bottom of the LV Power Supply.

A3. CHECK/ADJUST −50 V

NOTE

If the preceding step was not performed, first perform step A1, then proceed.



a. Connect the digital multimeter Low lead to the mainframe chassis. Connect the Volts/Ω lead to pin A17 or B17 of P100 on the A46 Plug-In Interface Board.

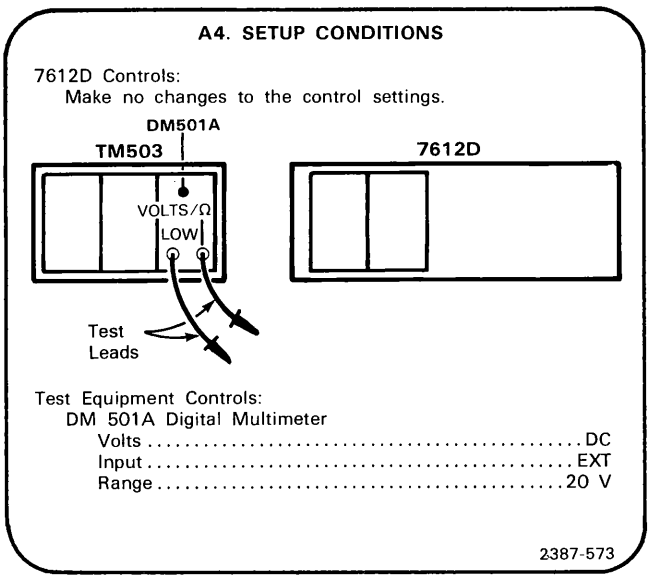
b. **CHECK**—that the digital multimeter reads −50.05 to −49.95 V.

c. **ADJUST**—50 V (R255), on the A88 Regulator Board for −50 V. Access to R255 is through a hole in the bottom of the LV Power Supply.

A4. CHECK OTHER POWER-SUPPLY VOLTAGES

NOTE

If the preceding step was not performed, first perform step A1, then proceed.



a. Connect the digital multimeter Low lead to the mainframe chassis. Connect the Volts/Ω lead to the connector and pin of the A46 Plug-In Interface Board indicated in Table 5-5.

b. **CHECK**—that each voltage listed in Table 5-5 is within its listed tolerance.

c. Connect the digital multimeter Low lead to J500, pin 5 on bottom of the A68 Main Interconnect board.

d. **CHECK**—that each voltage listed in Table 5-6 is within its listed tolerance.

e. Disconnect meter leads.

f. Replace the covers on the bottom and left side of the 7612D.

TABLE 5-5
Test Points and Tolerances of Supplies for Analog Circuits

Meter Range	Volts/Ω Meter Lead	Reading	Tolerance
200 VDC	J100, A22 or B22	+130 VDC	+128.7 to +131.3 V
200 VDC	J100, B3	+ 50 VDC	+49.75 to +50.25 V
20 VDC	J100, B4	+ 15 VDC	+14.91 to +15.09 V
20 VDC	J100, B5	+5 VDC	+4.95 to +5.05 V
20 VDC	J100, B7	−15 VDC	−15.045 to −14.955 V

TABLE 5-6
Test Points and Tolerances of Supplies for Digital Circuits

Meter Range	Volts/Ω Meter Lead	Reading	Tolerance
20 VDC	J500, Pin 9	+5.1 VDC	+4.998 to +5.202 V
20 VDC	J500, Pin 6	−2 VDC	−2.04 to −1.96 V

B. HIGH-VOLTAGE OSCILLATOR

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A
6. Time Base, 7B80
9. Probe, P6053B

B1. HIGH-VOLTAGE OSCILLATOR PRELIMINARY SETUP

a. Remove the 7612D right side cover.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS B page in Section 8, Diagrams and Circuit Board Illustrations.

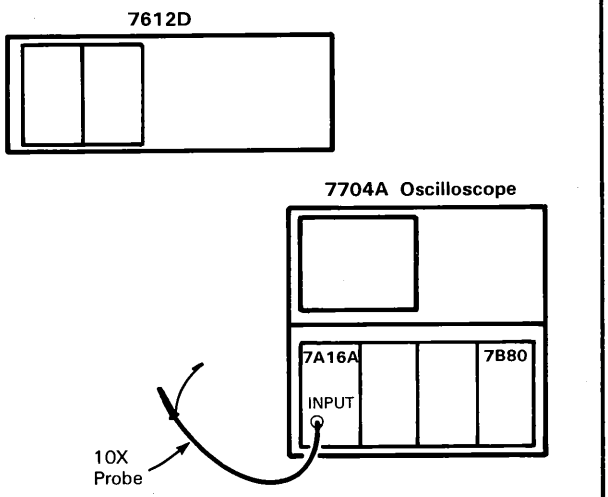
B2. CHECK OUTPUT OF HIGH-VOLTAGE OSCILLATOR

NOTE

First perform step B1, then proceed.

B2. SETUP CONDITIONS

7612D Controls:
ON/OFF ..... OFF



Test Equipment Controls:
7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... R

7A16A Amplifier
Volts/Div 10
Coupling ..... DC
Bandwidth ..... Full

7B80 Time Base
Time/Div ..... 10 μs
Triggering
Mode ..... P-P Auto
Source ..... Int
Coupling ..... AC

2387-574

a. Connect the 10X probe to J948 pin 1 on the A26 Deflection Amplifier Board. Connect the probe ground lead to TP924.

b. Establish a ground reference level on the test oscilloscope display.

c. Turn on the 7612D.

d. **CHECK**—for a flattened sine wave between -0.7 V and +15 V on the test oscilloscope.

e. **CHECK**—that after about 10 seconds, the display increases to between ground and about +40 V.

f. **CHECK**—that the period of the waveform is about 23 μs.

g. Turn the 7612D off.

h. Connect the probe to J948 pin 3 and repeat steps b through g.

i. Replace the 7612D right side cover.

C. CRT ALIGNMENT

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
4. Programmable Amplifier, 7A16P (two needed)
6. Time Base, 7B80
8. Probe, P6106 (two needed)
10. Test Leads for DMM
11. Digital Multimeter, DM 501A
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cables (four needed)
20. Adapter, bnc T

C1. CRT ALIGNMENT PRELIMINARY SETUP

a. Remove the 7612D right side cover.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS C page in Section 8, Diagrams and Circuit Board Illustrations.

C2. ADJUST CHANNEL A ANODE CURRENT

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

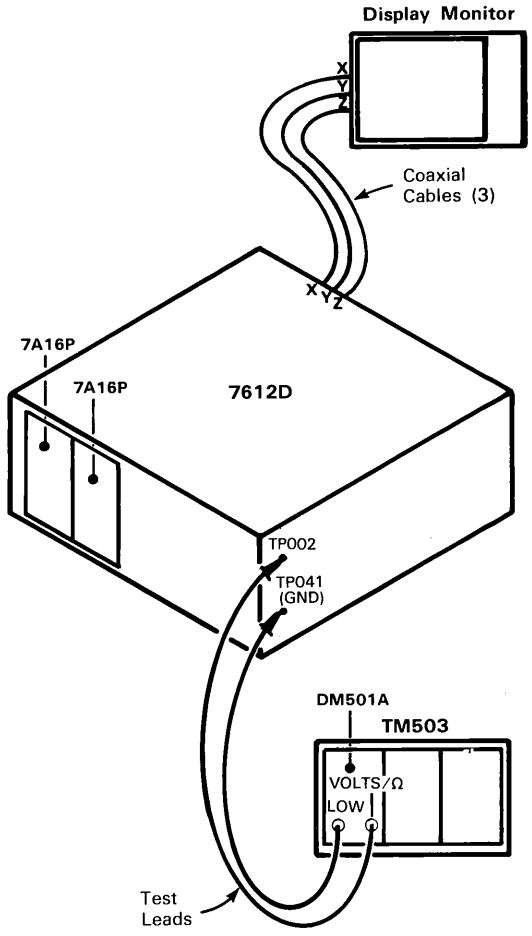
a. Connect and set the equipment as shown in C2. SETUP CONDITIONS.

b. **ADJUST**—AXAL (R010) for a minimum reading on the DMM.

c. **ADJUST**—AYAL (R110) for a maximum reading on the DMM.

C2. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:
7A16P Amplifier (both) ..... In power-up condition

DM 501A Digital Multimeter
Volts ..... DC
Input ..... Ext
Range ..... 2 V

2387-575

C3. ADJUST CHANNEL A X POSITION

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

a. Connect and set the equipment as shown in C3. SETUP CONDITIONS.

b. Press the 7612D SAMPLE INTERVAL button.

c. Use the DECREMENT/INCREMENT buttons to set the Sample Interval to 2E-6.

d. Press the 7612D ARM A button.

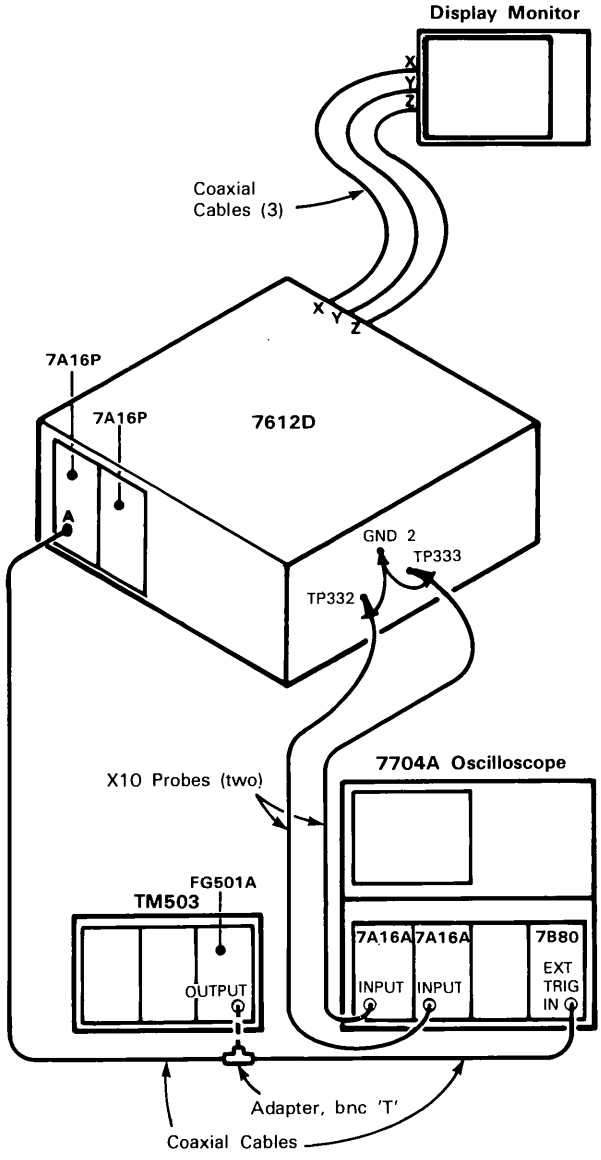
e. Adjust the function generator Amplitude control while continually pressing the ARM A button so that the display on the monitor is slightly clipped at the positive and negative peaks of the display. You may need to change the setting of the 7A16P Position control to center the monitor display.

f. Use the Position controls of the 7A16A amplifiers in the test oscilloscope to superimpose the two waveforms. Set the bottoms of the waveforms at the same level.

g. **ADJUST**—"A" X Pos control (R210) for equal amplitude waveforms on the test oscilloscope display.

C3. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7A16P Amplifier (left)
- Position ..... Mid-range
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... 20 MHz

7704A Oscilloscope
- Vertical Mode ..... Alt
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier (both)
- Position ..... Mid-range
- Volts/Div ..... 5 mV
- Coupling ..... DC
- Bandwidth ..... 20 MHz

7B80 Time Base
- Time/Div ..... 0.1 ms
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC HF Rej.
  - Source ..... Ext
- Mag ..... X1 (pressed in)

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^3
- Function ..... Triangle
- Amplitude ..... 9 o'clock
- Offset ..... Pressed in

2387-576

C4. CHECK/ADJUST CHANNEL A BEAM CURRENT

NOTE

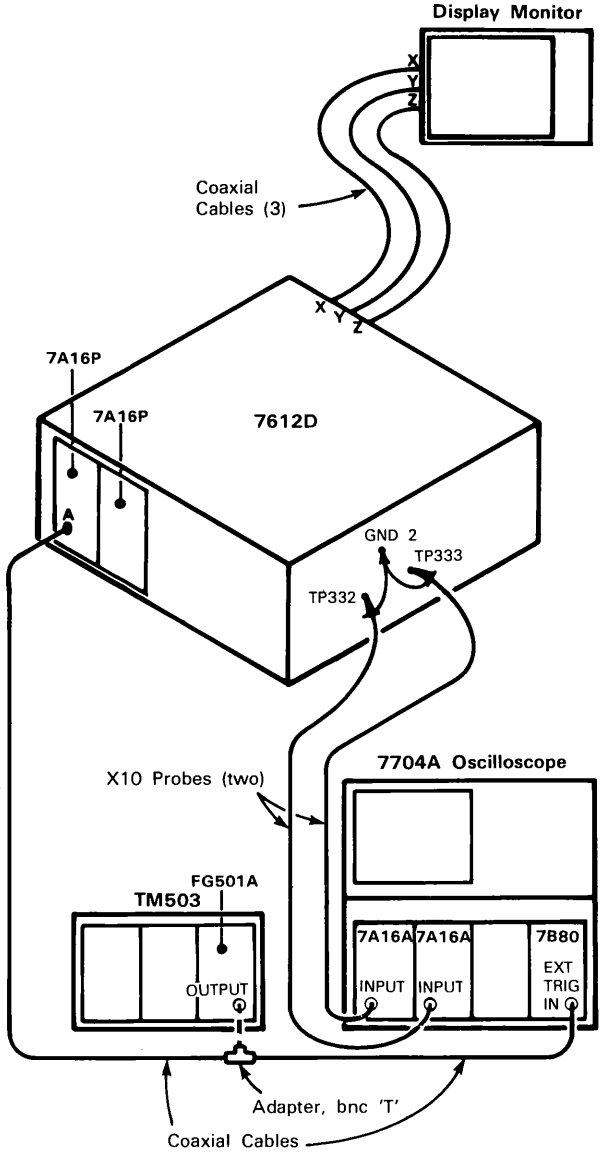
If the preceding step was not performed, first perform step C1, then proceed.

a. **CHECK**—for a display of 4.0 ±1/2 divisions (200 mV ±25 mV) on the test oscilloscope.

b. **ADJUST**—IBA (R306) for a display of 4 divisions (200 mV) on the test oscilloscope display.

C4. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7A16P Amplifier (left)
- Position ..... Mid-range
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... 20 MHz

7704A Oscilloscope
- Vertical Mode ..... Alt
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier (both)
- Position ..... Mid-range
- Volts/Div ..... 5 mV
- Coupling ..... DC
- Bandwidth ..... 20 MHz

7B80 Time Base
- Time/Div ..... 0.1 ms
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC HF Rej.
  - Source ..... Ext
- Mag ..... X1 (pressed in)

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^3
- Function ..... Triangle
- Amplitude ..... 9 o'clock
- Offset ..... Pressed in

2387-577

C5. ADJUST CHANNEL A ROTATION

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

a. Connect and set the equipment as shown in C5. SETUP CONDITIONS.

b. Verify that the two waveforms on the test oscilloscope are superimposed. If necessary, adjust the two 7A16A Position controls.

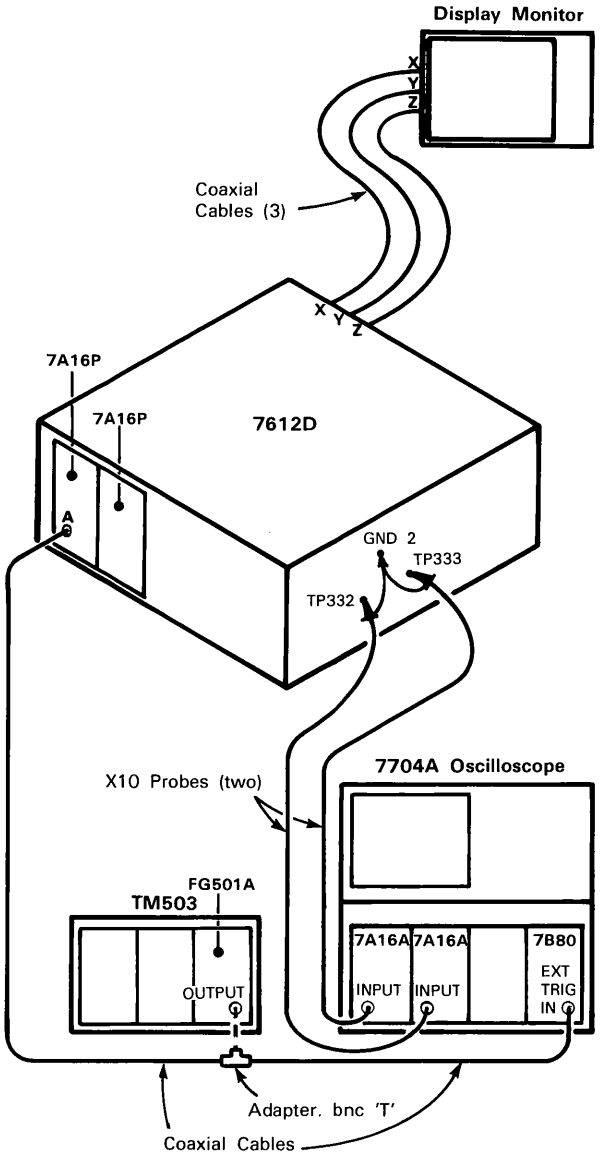
c. Set the Mag control on the 7B80 Time Base to X10.

d. Set the Time/Div to 0.1 ms.

e. **ADJUST**—A ROT (R310) for matching overlapped rising and falling edges. Figure 5-12 shows a typical display when R310 is correctly adjusted.

C5. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7A16P Amplifier (left)
- Position ..... Mid-range
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... 20 MHz

7704A Oscilloscope
- Vertical Mode ..... Alt
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier (both)
- Position ..... Mid-range
- Volts/Div ..... 5 mV
- Coupling ..... DC
- Bandwidth ..... 20 MHz

7B80 Time Base
- Time/Div ..... 0.1 ms
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC HF Rej.
  - Source ..... Ext
- Mag ..... X1 (pressed in)

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^3
- Function ..... Triangle
- Amplitude ..... 9 o'clock
- Offset ..... Pressed in

2387-578

C6. ADJUST CHANNEL A FOCUS

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

a. Connect and set the equipment as shown in C6. SETUP CONDITIONS.

b. Turn the 7612D power off.

c. Remove the nine front-panel retaining screws (eight on front and one in the right side of the plug-in compartment) and lay the front panel flat on the bench.

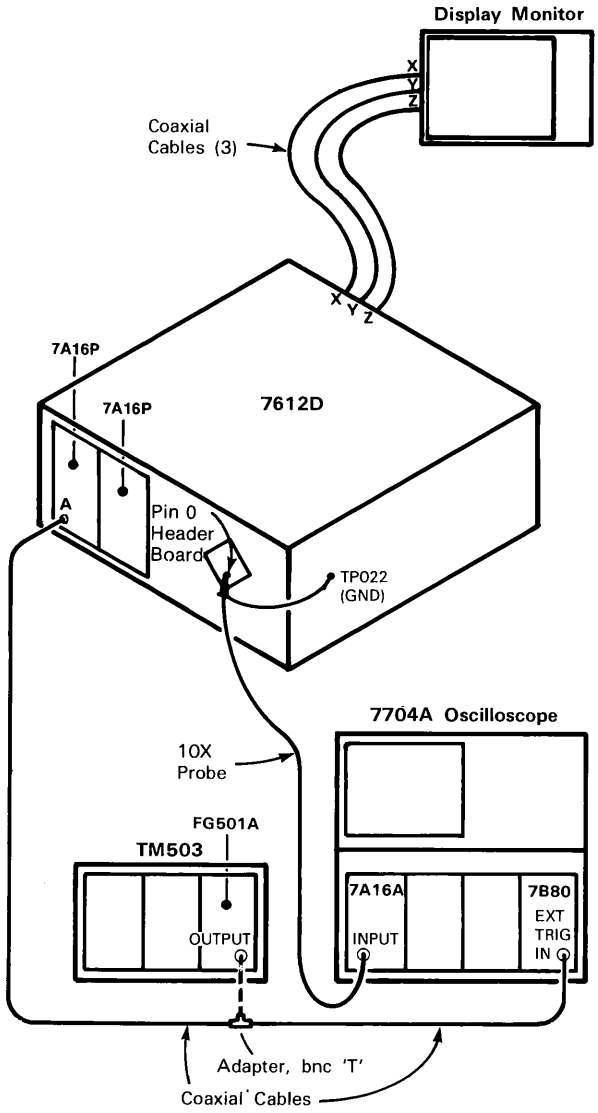
d. Turn the 7612D power on, and set the two 7A16P amplifiers as listed in C6. Setup Conditions.

e. Clip the probe tip to pin 7 on the top A14 Header Board assembly.

f. **ADJUST**—"A" Y Focus (R5006 on top of the high-voltage supply) for maximum amplitude of the envelope displayed on the 7704A Oscilloscope.

C6. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7A16P Amplifiers (both)
- Position ..... Centered
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... 20 MHz

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier
- Position ..... Centered
- Volts/Div ..... 5 mV
- Coupling ..... AC
- Bandwidth ..... 20 MHz

7B80 Time Base
- Time/Div ..... 0.1 ms
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC HF Rej
  - Source ..... EXT
- Mag ..... X1 (pressed in)

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^3
- Function ..... Triangle
- Amplitude ..... 9 o'clock
- Offset ..... Pressed in

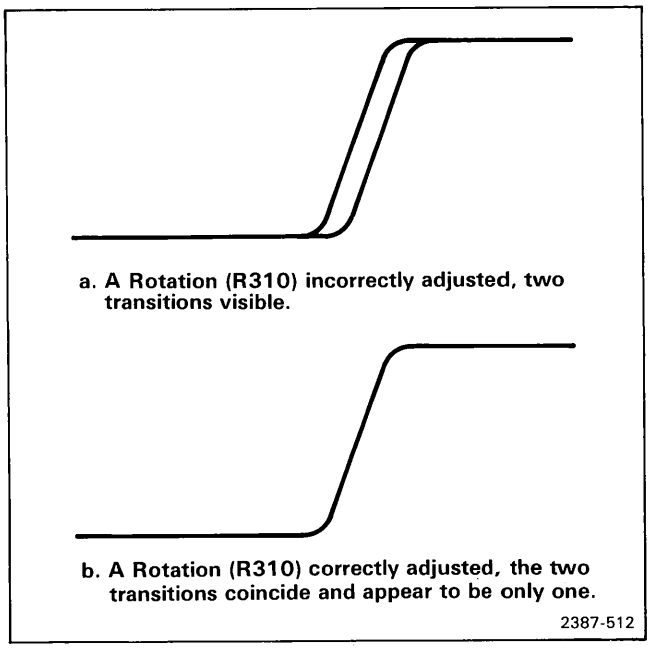
2387-579

g. **INTERACTION**—repeat steps C2 through C6 until negligible change is seen as you perform the adjustments. This compensates for interaction of the adjustments.

h. Perform steps C2 through C6 for the channel B EBS tube. Use the test points and adjustments listed in Table 5-7, Channel B CRT Alignment Test Points and Adjustments.

TABLE 5-7
Channel B CRT Alignment Test Points and Adjustments

Step	Test Point/Adjustment
C2	TP040, TP041
C2a	BXAL (R042)
C2b	BYAL (R139)
C3	TP330, TP331
C3g	BXPOS (R239)
C4	TP330, TP331
C4b	IBB (R440)
C5	TP330, TP331
C5d	B ROT (R338)
C6	Pin 7 on bottom of Header Board
C6e	"B" Y Focus (R of 5007) on top of the high-voltage supply



a. A Rotation (R310) incorrectly adjusted, two transitions visible.

b. A Rotation (R310) correctly adjusted, the two transitions coincide and appear to be only one.

2387-512

Fig. 5-12. Effect of A Rotation control on waveform at TP332 and TP333 (or B Rotation on waveform at TP330 & TP331).

D. BIT SYMMETRY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
4. Programmable Amplifier, 7A16P
6. Time Base, 7B80
9. Probe, P6053B (two needed)
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cable, 42 inch (five needed)
20. Adapter, bnc T

D1. BIT SYMMETRY PRELIMINARY SETUP

a. Remove the 7612D top cover.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS D page in Section 8, Diagrams and Circuit Board Illustrations.

D2. CHECK/ADJUST CHANNEL A BIT SYMMETRY

NOTE

First perform step d1, then proceed.

a. Connect and set the equipment as shown in D2. SETUP CONDITIONS.

b. Observe the display on the monitor.

c. While repeatedly pressing the 7612D ARM A button, vary the FG 501A Amplitude control so that the monitor display just fits its display area.

d. Adjust the Position control on the 7612D channel A amplifier, if necessary, to center the display on the monitor.

e. Increase the amplitude of the FG 501A signal while repeatedly pressing the 7612D ARM A button, until the monitor display overscans its area.

f. Vary the Trigger Level on the test oscilloscope time base to display two waveforms as shown in Figure 5-13a.

g. Set the test oscilloscope time base to X10 Mag by releasing its Mag button.

h. **CHECK**—that the D0 (Left Vert) waveform is symmetrical and the leading and trailing edges of D1 (Right Vert) are aligned between the 25% and 75% points (optimally 50%) of D0 as shown in Figure 5-13b.

i. **ADJUST**—AR0 (R016) to midrange.

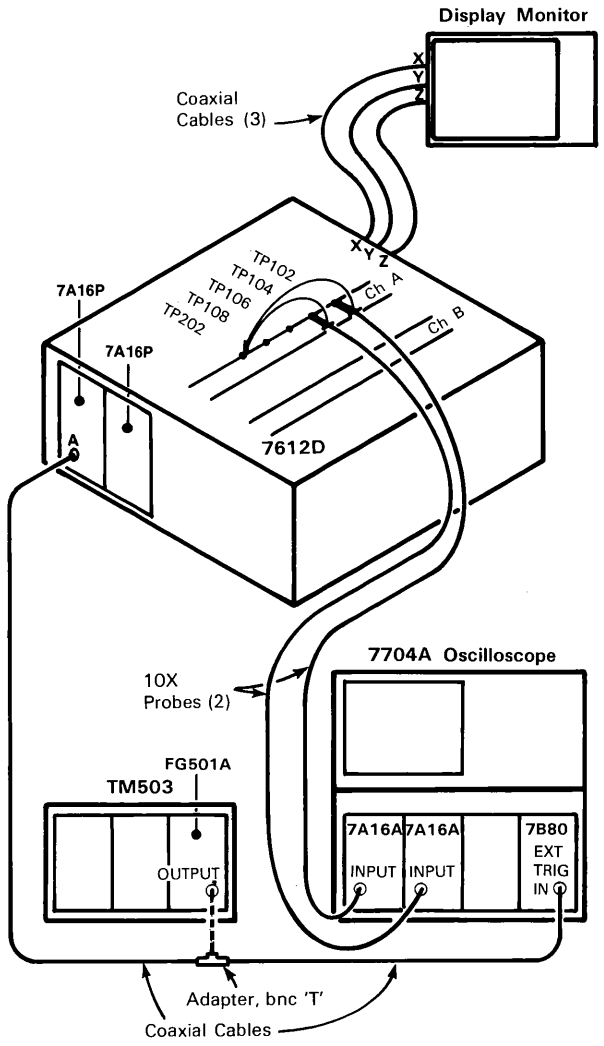
j. **ADJUST**—MRA (R218), for symmetrical waveform at D0 (Left Vert).

k. **ADJUST**—AR1 (R018), so that the leading and trailing edges of D1 are aligned between the 25% and 75% points (optimally 50%) of D0 over entire length of the displayed waveform.

l. Connect the Right Vertical amplifier's test probe to TP106 (D2) on the left CH A A18 Data Storage Board. Connect the Left Vertical amplifier's test probe to TP104 (D1) on the left CH A A18 Data Storage Board. Refer to the D2. Setup Conditions for TP locations.

D2. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 500E-9



Test Equipment Controls:

7A16P Amplifier (left)
- Position ..... Mid-range
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... 20 MHz

7704A Oscilloscope
- Vertical Mode ..... Alt
- Horizontal Mode ..... B
- B Trigger Soruce ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier (both)
- Position ..... Mid-range
- Volts/Div ..... 50 mV
- Coupling ..... AC
- Bandwidth ..... 20 MHz

7B80 Time Base
- Time/Div ..... 1 μs
- Mag ..... X1 (pressed in)
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... EXT

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^4
- Function ..... Sine wave
- Amplitude ..... 9 o'clock

2387-580

m. **CHECK**—that the leading and trailing edges of D2 are aligned between the 25% and 75% points of D1 over the entire length of the displayed waveforms. See Figure 5-13b.

n. **ADJUST**—AR2 (R112), so that the leading and trailing edges of D2 are aligned between the 25% and 75% points (optimally 50%) of D1 over the entire length of the displayed waveforms.

o. Connect the Right Vertical amplifier's test probe to TP108 (D3) on the left CH A A18 Data Storage Board. Refer to the D2. Setup Conditions.

p. **CHECK**—that the leading and trailing edges of D3 are aligned between the 25% and 75% points of D1 over the entire length of the displayed waveforms.

q. **ADJUST**—AR3 (R114), so that the leading and trailing edges of D3 are aligned between the 25% and 75% points (optimally 50%) of D1 over the entire length of the displayed waveforms.

r. Connect the Right Vertical amplifier's test probe to TP102 (D4, which is labeled D0) and the ground lead to TP202 on the right CH A A18 Data Storage Board.

s. **CHECK**—that the leading and trailing edges of D4 are aligned between the 25% and 75% points of D1 over the entire length of the displayed waveforms.

t. **ADJUST**—AR4 (R116), so that the leading and trailing edges of D4 are aligned between the 25% and 75% points (optimally 50%) of D1 over the entire length of the displayed waveforms.

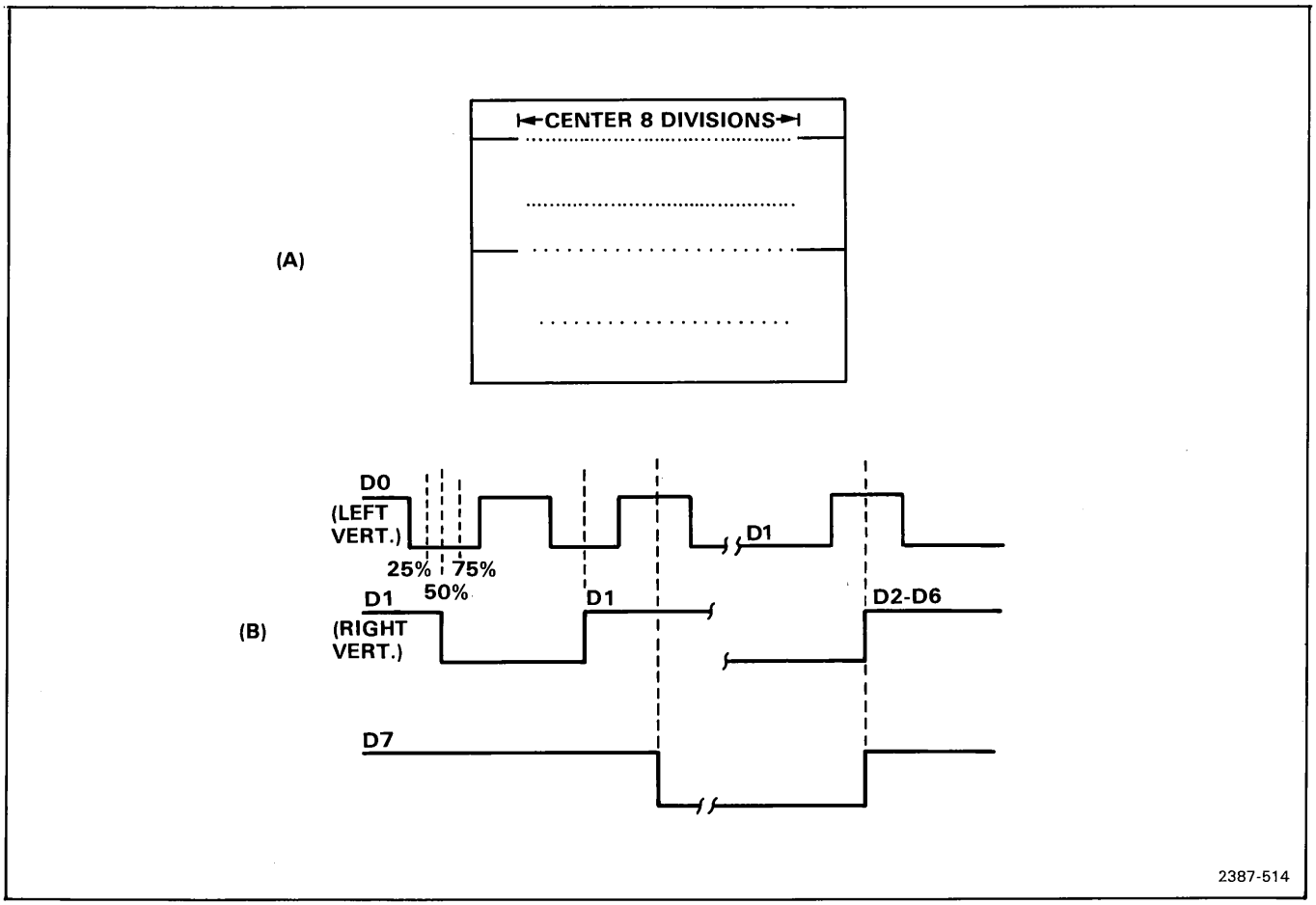


Fig. 5-13. Bit symmetry waveforms.

u. Connect the Right Vertical amplifier's test probe to TP104 (D5, which is labeled D1) on the right CH A A18 Data Storage Board.

v. **CHECK**—that the leading and trailing edges of D5 are aligned between the 25% and 75% points of D1 over the entire length of the displayed waveform.

w. **ADJUST**—AR5 (R212), so that the leading and trailing edges of D5 are aligned between the 25% and 75% points (optimally 50%) of D1 over the entire length of the displayed waveforms.

x. Connect the Right Vertical amplifier's test probe to TP106 (D6 which is labeled D2) on the right CH A A18 Data Storage Board.

y. **CHECK**—that the leading and trailing edges of D6 are aligned between the 25% and 75% points of D1 over the entire length of the displayed waveform.

z. **ADJUST**—AR6 (R214), so that the leading and trailing edges of D6 are aligned between the 25% and 75% points (optimally 50%) of D1 over the entire length of the displayed waveforms.

aa. Connect the Right Vertical amplifier's test probe to TP108 (D7, which is labeled D3) on the right CH A A18 Data Storage Board.

bb. **CHECK**—that the leading edge of D7 (see Fig. 5-13) is aligned between 25% and 75% points of D1.

cc. **ADJUST**—AR7 (R216), so that the leading edge of D7 is aligned between the 25% and 75% points (optimally 50%) of D1.

dd. Repeat parts l through o for check of overall bit symmetry.

ee. Disconnect test oscilloscope probes.

D3. CHECK/ADJUST CHANNEL B BIT SYMMETRY

NOTE

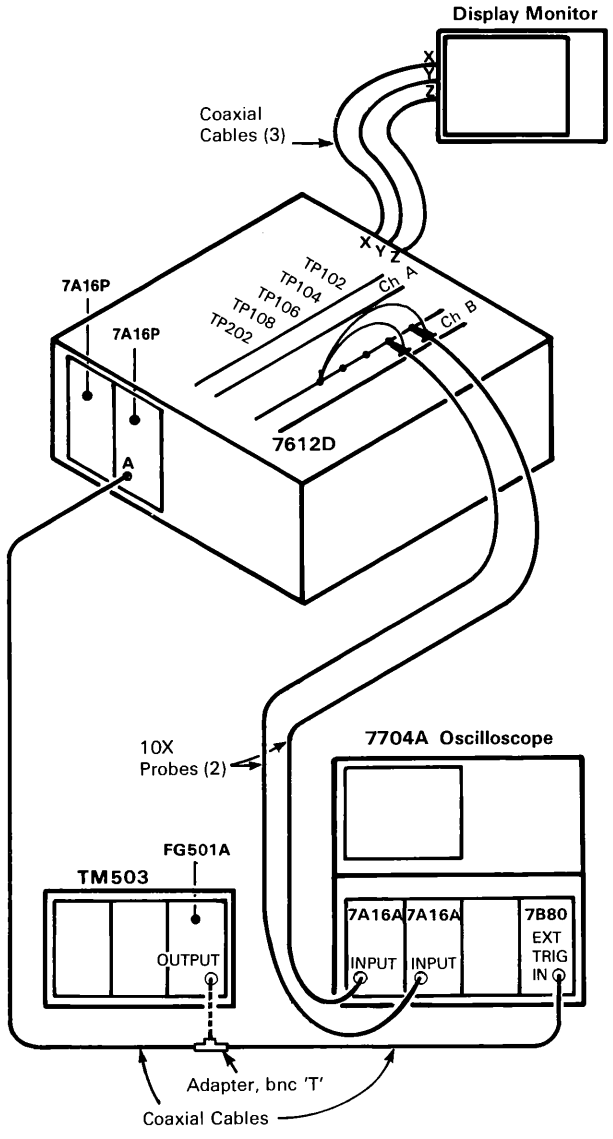
If the preceding step was not performed, first perform step D1, then proceed.

a. Observe the display on the monitor.

b. While repeatedly pressing the 7612D ARM B button, vary the FG 501A Amplitude control so that the monitor display just fits in its display area.

D3. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 500E-9
- TRIGGER FUNCTIONS
  - SELECT ..... R
- INSTRUMENT FUNCTION
  - PROGRAM ..... CHANNEL B



Test Equipment Controls:

7A16P Amplifier (right)
- Position ..... Mid-range
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... 20 MHz

7704A Oscilloscope
- Vertical Mode ..... Alt
- Horizontal Mode ..... B
- B Trigger Soruce ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier (both)
- Position ..... Mid-range
- Volts/Div ..... 50 mV
- Coupling ..... AC
- Bandwidth ..... 20 MHz

7B80 Time Base
- Time/Div ..... 1 μs
- Mag ..... X1 (pressed in)
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... EXT

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^4
- Function ..... Sine wave
- Amplitude ..... 9 o'clock

2387-581

c. Adjust the Position control on the 7612D Channel B amplifier as needed to center the display on the monitor.

d. Increase the amplitude of the FG 501A signal while repeatedly pressing the 7612D ARM B button, until the monitor display overscans its area.

e. Vary the Trigger Level on the test oscilloscope time base to display two waveforms as shown in Figure 5-13.

f. Set the test oscilloscope time base to X10 Mag by releasing its Mag button.

g. Repeat parts g through dd of D2. CHECK/ADJUST CHANNEL A BIT SYMMETRY, using the left and right Channel B A18 Data Storage Boards. Refer to TEST POINT AND ADJUSTMENT LOCATIONS B pullout page in Section 8, Diagrams and Circuit Board Illustrations.

E. CLOCK BUFFER

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
2. Amplifier, 7A16A
4. Programmable Amplifier, 7A16P (two needed)
7. Counter, 7D15
10. Test Leads
11. Digital Multimeter, DM 501A
14. Sine-Wave Generator, SG 503
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cable (four needed)
22. Dual-Input Coupler

E1. CLOCK BUFFER PRELIMINARY SETUP

a. Turn the 7612D Power off.

b. Remove the nine screws that retain the 7612D front panel (eight on the front panel and one in the plug-in compartment) and lay the front panel flat on the workbench.

c. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

d. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

e. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

f. See the TEST POINT AND ADJUSTMENT LOCATIONS E page in Section 8, Diagrams and Circuit Board Illustrations.

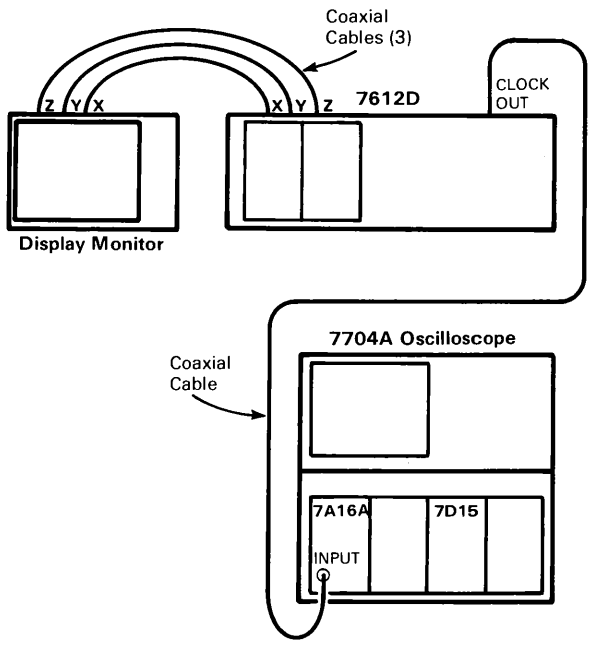
E2. ADJUST CLOCK THRESHOLD

NOTE

First perform step E1, then proceed.

E3. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- A Trigger Source ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A16A Amplifier
- Volts/Div ..... 20 mV
- Bandwidth ..... Full
- Coupling ..... AC

7D15 Universal Counter/Timer
- Gate ..... Norm
- Mode ..... Freq B
- Time ..... 10 ms
- Trigger
  - B ..... Trig Source
  - Level 0

2387-583

a. While repeatedly pressing the 7612D ARM A and ARM B buttons, adjust the SG 503 Amplitude to provide two displays of 2 to 3 divisions each on the display monitor.

b. **ADJUST**—Threshold Level (R228) for the cleanest looking display on the monitor, for both A and B channels. By "clean," we mean no stray bits outside the envelope of the waveform.

c. Connect the Low lead of the DM 501A to TP310, and connect the Volts/Ω lead to pin 2 or 3 of J418.

d. Check that the voltage reads −8.55, ± 0.05 V, at both pins 2 and 3.

e. If the voltage at pins 2 and 3 of J418 is outside the −8.50 to −8.60 V range, adjust the B DC Level (R510) control to set the voltage to −8.55 V.

f. Connect the DMM Volts/Ω lead to pin 2 of J524.

g. Check that the DMM reads −8.55 V ±0.05 V at both pins 2 and 3.

h. If the voltage on pins 2 and 3 of J524 is outside the −8.50 to −8.60 V range, ADJUST the A DC Level control (R528) to set the voltage to −8.55 V.

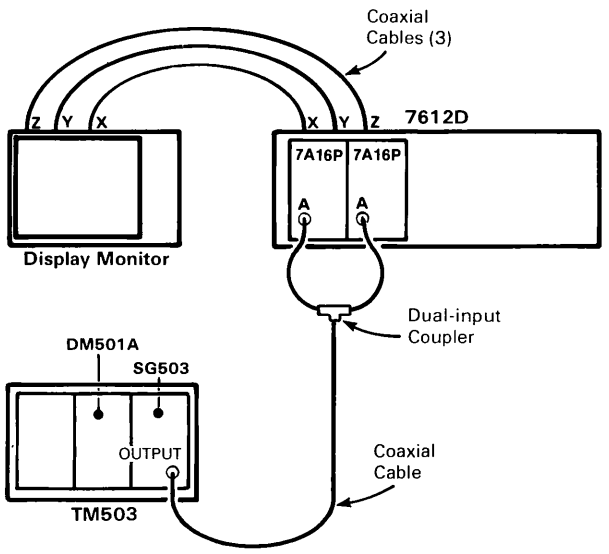
E3. CHECK CLOCK FREQUENCY

NOTE

If the preceding step was not performed, first perform step E1, then proceed.

E2. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7A16 Amplifier (both)
- Position ..... Mid-range
- Volts/Div 0.5
- Coupling ..... AC
- Input ..... 1 MΩ
- Bandwidth ..... Full

SG503 Leveled Sine Wave Generator
- Frequency Range (MHz) 50-100
- Frequency Variable ..... For a readout of 79.9 MHz
- Amplitude Multiplier X1

DM501A Digital Multimeter
- Volts ..... DC
- Input ..... Ext
- Range ..... 20 V

2387-582

a. **CHECK**—the 7D15 readout of the clock frequency on the test oscilloscope. The frequency should be 200 MHz ±7 kHz (1.993 to 200.007 MHz).

NOTE

It may be necessary to adjust the Trigger B Level on the 7D15 to get a frequency readout on the test oscilloscope.

b. Turn off the 7612D.

c. Replace the front panel.

F. XYZ DISPLAY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
2. Amplifier, 7A16A
6. Time Base, 7B80
17. Coaxial Cable
19. Calibration Fixture

F1. XYZ DISPLAY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

d. See the TEST POINT AND ADJUSTMENT LOCATIONS F page in Section 8, Diagrams and Circuit Board Illustrations.

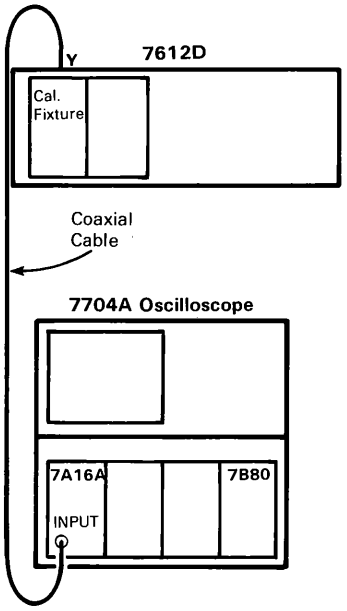
F2. CHECK/ADJUST Y GAIN

NOTE

First perform step F1, then proceed.

F2. SETUP CONDITIONS

7612D Controls:
ON/OFF ..... OFF



Test Equipment Controls:
7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... B
B Trigger Source ..... Vert Mode

7A16A Amplifier
Volts/Div 0.2
Coupling ..... DC
Polarity ..... +Up

7B80 Time Base
Time/Div ..... 2 ms
Triggering
Mode ..... Norm
Coupling ..... AC
Source ..... Int
Slope ..... +
Level ..... Centered

Calibration Fixture
Rep Rate ..... 1 kHz
Position ..... Centered
Test ..... Vert or Horiz Gain

2387-584

a. Turn on the 7612D.

b. Press the 7612D SAMPLE INTERVAL button.

c. Use the DECREMENT/INCREMENT buttons to set the A Sample Interval to 20E-6.

d. Press the 7612D COPY button. This programs Channel B with the Sample Interval (20E-6) from Channel A.

e. Press the 7612D ARM A button.

f. Observe the display on the test oscilloscope. If necessary, adjust the time base Variable Time/Div to provide a stable display.

g. Leave the 7612D turned on, and move the calibration fixture from Channel A to Channel B.

h. Press the PROGRAM CHANNEL B button.

i. Press the TRIGGER SELECT R button.

j. Press the ARM B button.

k. Observe the display on the test oscilloscope. If necessary, adjust the Variable Time/Div to provide a stable display.

l. **CHECK**—that the distance between the top and bottom stairsteps is 5.0 ±0.15 (4.85 to 5.15) divisions. See Figure 5-14.

m. Remove the 7612D top cover.

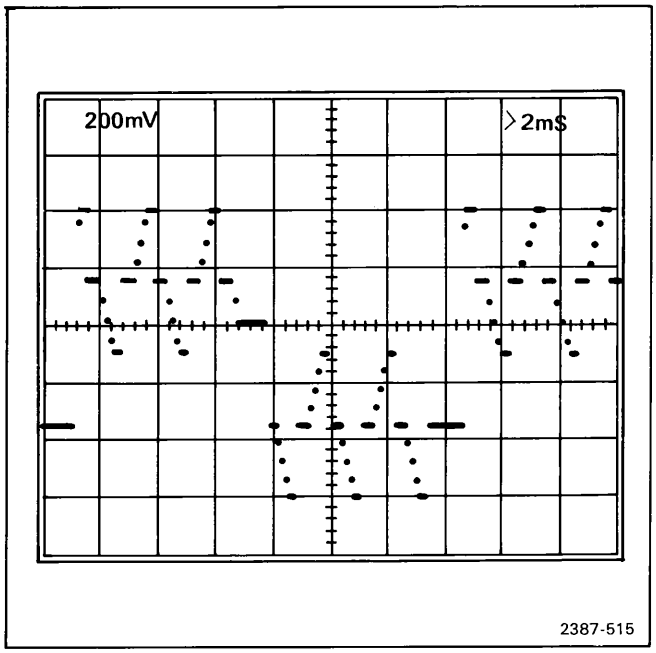


Fig. 5-14. Display of staircase waveforms for checking Y gain.

n. **ADJUST**—Gain (R200) for a display amplitude of 5.0 divisions between the top and bottom steps of the staircase waveform.

o. Replace the 7612D top cover.

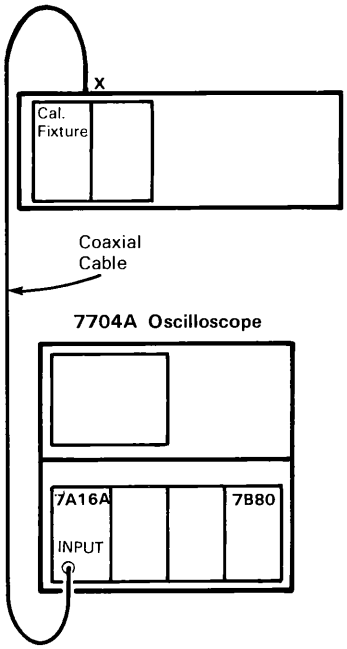
F3. CHECK/ADJUST X GAIN

NOTE

If the preceding step was not performed, first perform step F1, then proceed.

F3. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



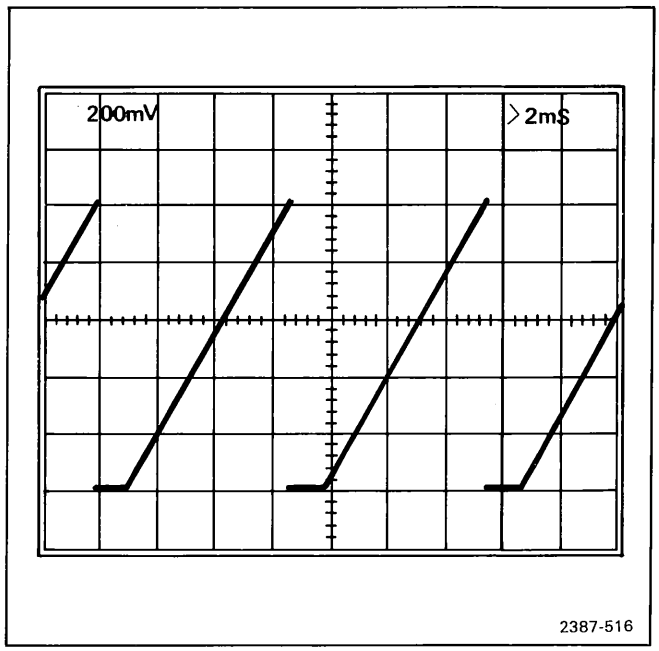
Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode

7A16A Amplifier
- Volts/Div 0.2
- Coupling ..... DC
- Polarity ..... +Up

7B80 Time Base
- Time/Div ..... 2 ms
- Triggering
  - Mode ..... Norm
  - Coupling ..... AC
  - Source ..... Int
  - Slope ..... –
  - Level ..... Centered

2387-585



2387-516

Fig. 5-15. Display of ramp waveform for checking X gain.

a. Observe the test oscilloscope display. If necessary, adjust the Variable Time/Div to provide a stable display.

b. **CHECK**—that the amplitude of the ramp displayed on the test oscilloscope is between 4.85 and 5.15 divisions (5.0 ±0.15 div). See Figure 5-15.

c. Remove the 7612D top cover.

d. **ADJUST**—X Gain (R300) to set the amplitude of the ramp to 5.0 divisions.

e. Replace the 7612D top cover.

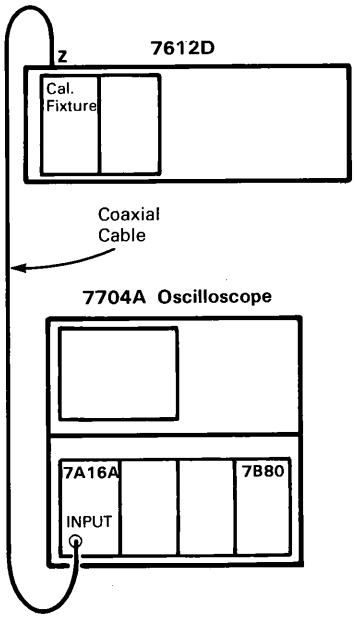
F4. CHECK Z GAIN

NOTE

If the preceding step was not performed, first perform step F1, then proceed.

F4. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Vert Mode

7A16A Amplifier
- Volts/Div 0.5
- Coupling ..... DC
- Bandwidth ..... 20 MHz
- Polarity ..... +Up

7B80 Time Base
- Time/Div ..... 2 μs
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... Int
  - Slope ..... +
  - Level ..... Centered

2387-586

a. **CHECK**—that the amplitude of the unblanking pulse is at least one volt (two divisions).

G. TRIGGER

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
4. Programmable Amplifier, 7A16P (two needed)
6. Time Base, 7B80
13. Function Generator, FG 501A
14. Sine-Wave Generator, SG 503
15. Power Module Mainframe, TM 503
17. Coaxial Cable (four needed)
20. Adapter, bnc T
23. Attenuator, 10X

G1. TRIGGER PRELIMINARY SETUP

a. Remove the 7612D top cover for steps G2, G3, and G7 only.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS G page in Section 8, Diagrams and Circuit Board Illustrations.

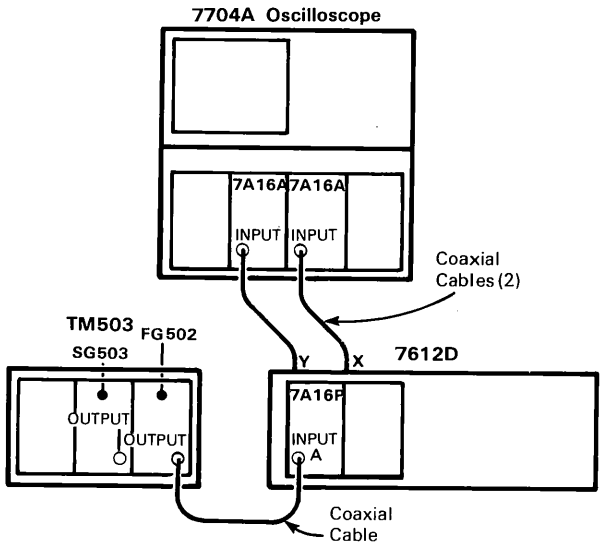
G2. CHECK/ADJUST CHANNEL A INTERNAL TRIGGER

NOTE

First perform step G1, then proceed.

G2. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6



Test Equipment Controls:

7A16P Amplifier
Volts/Div 0.2
Input 50Ω
Coupling ..... AC
Bandwidth ..... Full
Polarity ..... +Up
Position ..... Centered

PG 501A Function Generator
Frequency Hz 5
Multiplier ..... 10^4
Function ..... ~ (sine wave)
Offset ..... Pressed in
Amplitude ..... Min

7704 Oscilloscope
Vertical Mode ..... Right
Horizontal Mode ..... A

7A16A Amplifier (both)
Volts/Div 0.1
Coupling ..... DC
Bandwidth ..... Full
Polarity ..... +Up
Position ..... Centered

2387-587

NOTE

The L Slope Bal (R703) adjustment should be set 90° from the clockwise end of its rotation.

a. Find the upper and lower limiting points of the Channel A amplifier as follows:

1. While observing the test oscilloscope display, repeatedly press the ARM A button and advance the FG 501A Amplitude control until the amplitude of the sine wave displayed on the oscilloscope will increase no more. The sine wave will then appear clipped on its tops and bottoms.

2. Set the Right Vertical 7A16A to 50 mV/Div.

3. Release the Right Vertical 7A16A Variable Volts/Div control.

4. Use the Right Vertical 7A16A Variable Volts/Div and Position controls to set the top and bottom of the waveform to the top and bottom graticule lines. The display will be eight divisions high.

b. Set the 7A16P, in the 7612D, to 2 V/Div.

c. Repeatedly press the ARM A button while adjusting the FG 501A Amplitude control to produce a display of three minor divisions on the test oscilloscope. (If the 7612D will not trigger at this low amplitude, slightly adjust the 7A16P Position control until it triggers again.)

d. **CHECK**—for a triggered XY display (L TRIGGERED light on) on the test oscilloscope in the following eight Trigger settings:

COUPLING	SLOPE	HF REJ
1. AC	+	On
2. AC	+	Off
3. AC	−	On
4. AC	−	Off
5. DC	+	On
6. DC	+	Off
7. DC	−	On
8. DC	−	Off

e. **ADJUST**—L Norm Offset (R802) for a triggered display (L TRIGGERED light on) in the eight Trigger settings given in part d.

f. Set the FG 501A to 40 Hz.

g. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude control as needed to cause a display of three minor divisions on the test oscilloscope.

h. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the following eight Trigger settings:

COUPLING	SLOPE	HF REJ
1. AC	+	On
2. AC	+	Off
3. AC	−	On
4. AC	−	Off
5. DC	+	On
6. DC	+	Off
7. DC	−	On
8. DC	−	Off

Set 7A16P Position and TRIGGER LEVEL as necessary to verify triggering. If the 7612D acquires the wrong slopes, readjust L Norm Offset (R802) and recheck it at 50 kHz.

i. Connect the signal cable to the SG 503 Leveled Sine Wave Generator, and set the SG 503 as follows:

Frequency Range 25-50
Frequency Variable . . . . . To cause a readout of 50.0 on the Frequency MHz readout.
Amplitude Multiplier X1
Output Amplitude Volts P-P . . . Minimum

j. While repeatedly pressing the ARM A button, set the SG 503 Output Amplitude control to produce a display of 1.18 major divisions on the oscilloscope display.

k. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the four following Trigger settings:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

l. Set the SG 503 to 100 MHz.

m. Set the 7612D SAMPLE INTERVAL to 100E-9.

n. Repeatedly press the ARM A button and check that the XY display on the oscilloscope is 1.18 major divisions in amplitude. If necessary, adjust the SG 503 Output Amplifier for the desired amplitude.

o. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the following four Trigger settings:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

p. Replace the 7612D top cover.

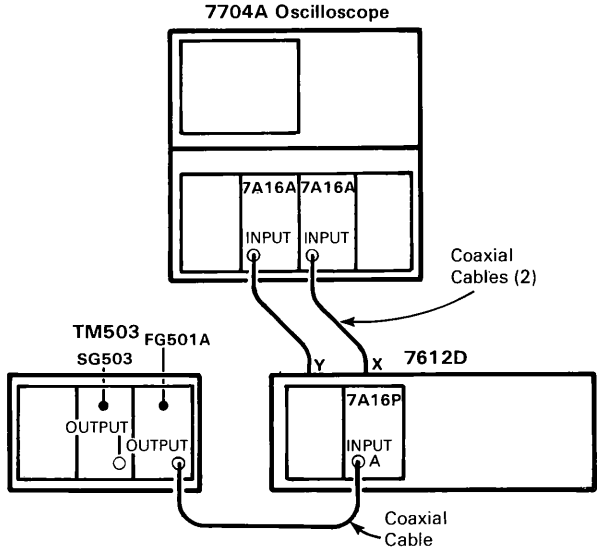
G3. CHECK/ADJUST CHANNEL B INTERNAL TRIGGER

NOTE

If the preceding step was not performed, first perform step G1, then proceed

G3. SETUP CONDITIONS

7612D Controls:
- INST FUNCT
  - PROGRAM ..... CHAN B
- TRIGGER FUNCTIONS
  - SELECT ..... R



Test Equipment Controls:
- 7A16P Amplifier
  - Volts/Div 0.2
  - Input 50Ω
  - Coupling ..... AC
  - Bandwidth ..... Full
  - Polarity ..... +Up
  - Position ..... Centered
- PG 501A Function Generator
  - Frequency Hz 5
  - Multiplier ..... 10^4
  - Function ..... ∿(sine wave)
  - Offset ..... Pressed in
  - Amplitude ..... Min
- 7704 Oscilloscope
  - Vertical Mode ..... Right
  - Horizontal Mode ..... A
- 7A16A Amplifiers (both)
  - Volts/Div 0.1
  - Coupling ..... DC
  - Bandwidth ..... Full
  - Polarity ..... +Up
  - Position ..... Centered

2387-588

NOTE

The R Slope Bal adjustment (R302) should be set 90° from the clockwise end of its rotation.

a. Find the upper and lower limiting points of the Channel B amplifier as follows:

1. While observing the test oscilloscope display, repeatedly press the ARM B button and advance the FG 501A Amplitude control until the amplitude of the sine wave displayed on the oscilloscope will increase no more. The sine wave will then appear clipped on its tops and bottoms.

2. Set the Right Vertical 7A16A to 50 mV/Div.

3. Release the Right Vertical 7A16A Variable Volts/Div control.

4. Use the Right Vertical 7A16A Variable Volts/Div and Position controls to set the top and bottom of the waveform to the top and bottom graticule lines. The display will be eight divisions high.

b. Set the 7A16P, in the 7612D, to 2 V/Div.

c. Repeatedly press the ARM A button while adjusting the FG 501A Amplitude control to produce a display of three minor divisions on the test oscilloscope. (If the 7612D will not trigger at this low amplitude, slightly adjust the 7A16P Position control until it triggers again.)

d. **CHECK**—for a triggered (XY display (R TRIGGERED light on) on the test oscilloscope in the following eight Trigger settings:

	SLOPE	COUPLING	HF REJ
1.	+	AC	On
2.	+	AC	Off
3.	+	DC	On
4.	+	DC	Off
5.	−	AC	On
6.	−	AC	Off
7.	−	DC	On
8.	−	DC	Off

e. **ADJUST**—R Norm Offset (R306) for a triggered display (R TRIGGERED light on) in the eight Trigger settings given in part d.

f. Set the FG 501A to 40 Hz.

g. While repeatedly pressing the ARM B button, adjust the FG 501A Amplitude control as needed to cause a display of three minor divisions on the test oscilloscope.

h. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the following eight Trigger settings:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	AC	Off
3. +	DC	On
4. +	DC	Off
5. −	AC	On
6. −	AC	Off
7. −	DC	On
8. −	DC	Off

Set 7A16P Position and the 7612D TRIGGER LEVEL as necessary to verify triggering. If the 7612D acquires the wrong slopes, readjust R Norm Offset (R306) and recheck it at 50 kHz.

i. Connect the signal cable to the SG 503 Leveled Sine Wave Generator, and set the SG 503 as follows:

Frequency Range 25-50
Frequency Variable ..... To cause a readout of 50.0 on the Frequency MHz readout.
Amplitude Multiplier X1
Output Amplitude Volts P-P ... Minimum

j. While repeatedly pressing the ARM B button, set the SG 503 Output Amplitude control to produce a display of 1.18 major divisions on the oscilloscope display.

k. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the four following Trigger settings:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

l. Set the SG 503 to 100 MHz.

m. Set the 7612D SAMPLE INTERVAL to 100E-9.

n. Repeatedly press the ARM B button and check that the XY display on the oscilloscope is 1.18 major divisions in amplitude. If necessary, adjust the SG 503 Output Amplifier for the desired amplitude.

o. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the following four Trigger settings:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

p. Replace the 7612D top cover.

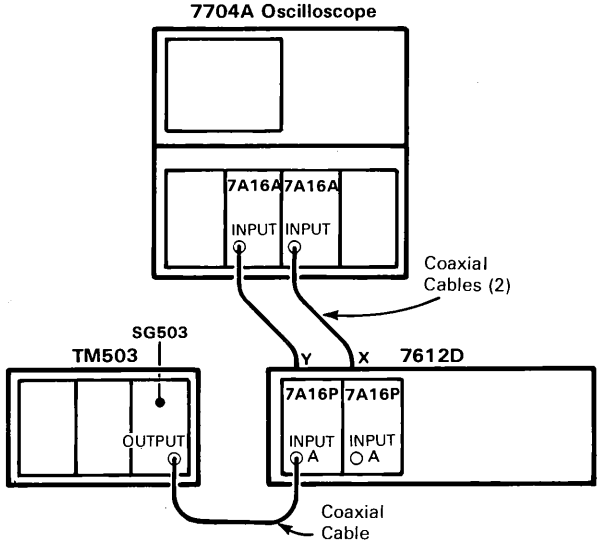
G4. CHECK INTERNAL HIGH-FREQUENCY REJECT

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G4. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6



Test Equipment Controls:
7A16P Amplifier (both)
Volts/Div 0.5
Input 50Ω
Coupling ..... AC
Bandwidth ..... Full

SG 503 Leveled Sine Wave Generator
Frequency Range (MHz) 25-50
Frequency Variable ..... To produce an output of 50 MHz
Amplitude Multiplier X1

7704A Oscilloscope
Vertical Mode ..... Right
Horizontal Mode ..... A

7A16A Amplifiers (both)
Volts/Div 0.1
Coupling ..... DC
Bandwidth ..... Full
Polarity ..... +Up
Position ..... Centered

2387-589

a. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude control for a two-major-division display on the test oscilloscope.

b. Set the 7612D to High-Frequency Reject mode.

c. **CHECK**—that the Trigger circuit does not operate (L TRIGGERED light is off) in the four following Trigger modes (the 7612D may trigger when switching modes and need to be re-armed):

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	DC	On
3. −	AC	On
4. −	DC	On

d. Press the 7612D COPY button.

e. Connect the SG 503 signal to the 7612D CHANNEL B input and press the PROGRAM CHANNEL B button.

f. Repeat steps a, b, and c, using the ARM B button.

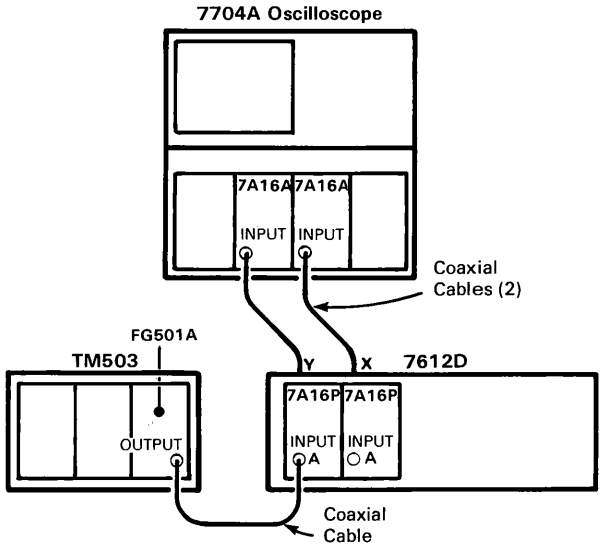
G5. CHECK INTERNAL TRIGGER LEVEL RANGE

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G5. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 6E-6



Test Equipment Controls:

7A16P Amplifier (both)
- Volts/Div 0.5
- Input 50Ω
- Coupling ..... AC
- Bandwidth ..... Full

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^3
- Function ..... ~(sinewave)
- Offset ..... Pressed in
- Amplitude ..... Centered

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifiers (both)
- Volts/Div 0.1
- Coupling ..... DC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

2387-590

a. While repeatedly pressing the ARM A button, set the FG 501A Amplitude so that the oscilloscope display begins to clip.

b. Repeatedly press the ARM A button and adjust the 7A16P Position control so that the displayed waveform is clipped equally at its top and bottom.

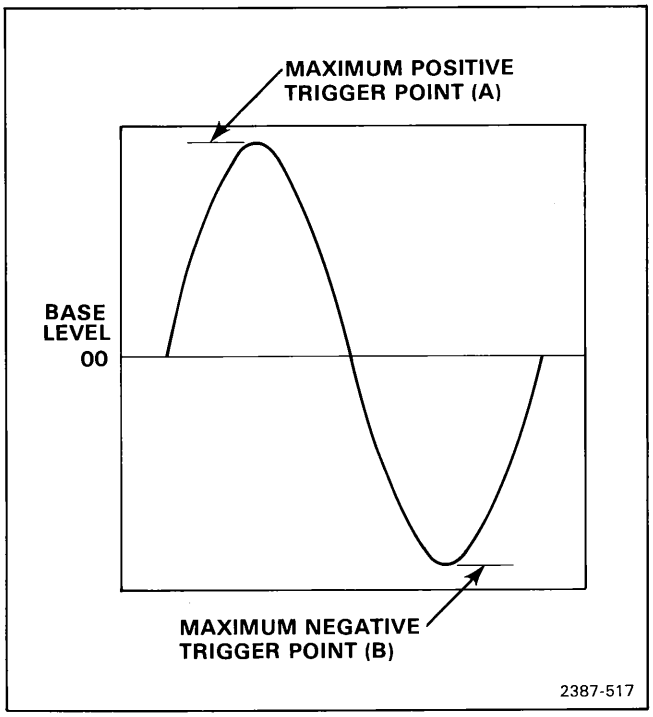


Fig. 5-16. XY display showing maximum positive and negative trigger points.

c. Continue pressing the ARM A button, and adjust the FG 501A Amplitude control so that the displayed waveform amplitude is just short of the clipping points.

d. **CHECK**—the oscilloscope for a triggered XY display (7612D L TRIGGERED light on) that varies, while changing the 7612D TRIGGER LEVEL and pressing the ARM A button, from a base level (00) to a maximum positive level between 90 and 126, then back to the base level and on to a maximum negative level between −90 and −127. Figure 5-16 shows the desired display.

e. Connect the FG 501A output to the 7612D CHANNEL B input.

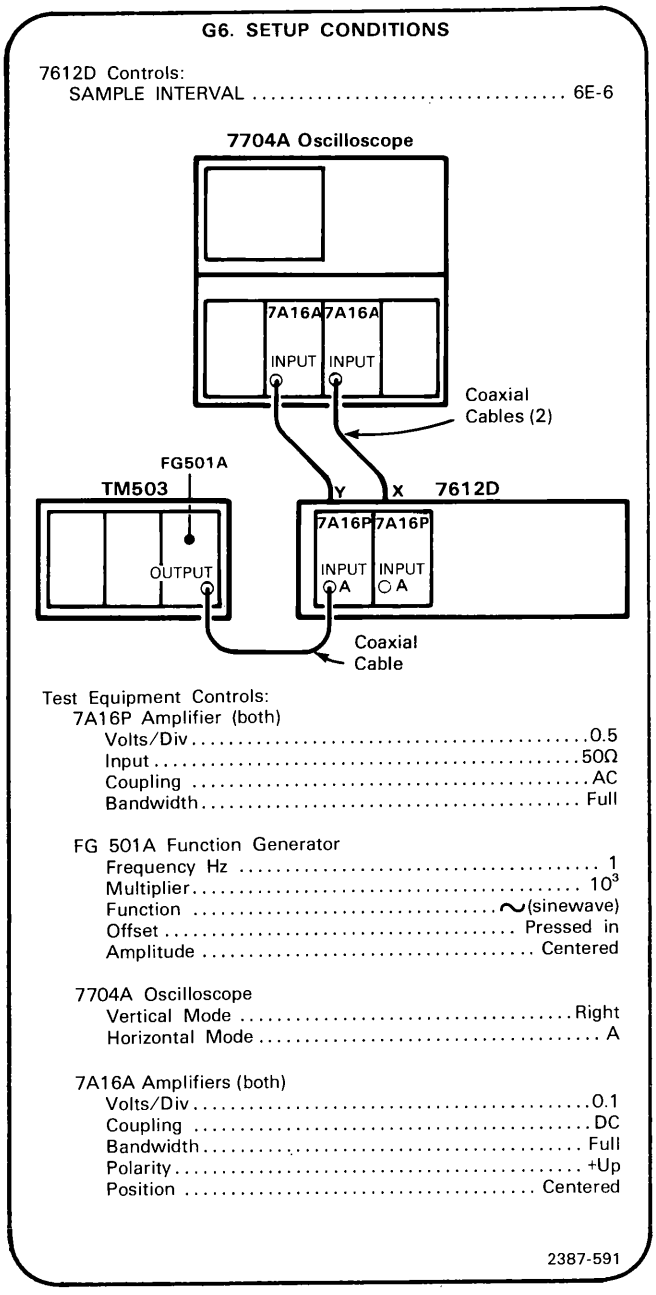
f. Press the COPY button, then press PROGRAM CHANNEL B.

g. Repeat parts a through d, using the ARM B button.

G6. CHECK MANUAL TRIGGER

NOTE

If the preceding step was not performed, first perform step G1, then proceed



a. Increase the left 7A16D Volts/Div until the L TRIGGERED light goes out. If necessary, reduce the amplitude of the input signal.

b. Press the ARM A button; observe that the ARM A button lights and stays lit.

c. **CHECK**—that pressing the MAN TRIG button causes the L TRIGGERED button to light momentarily, that a triggered XY display appears on the test oscilloscope, and that the ARM A button is now extinguished.

d. Press COPY, then press PROGRAM CHANNEL B.

e. Connect the FG 501A output signal to the 7612D CHANNEL B input.

f. Repeat parts a through c for CHANNEL B, using the R TRIGGERED light and the ARM B button.

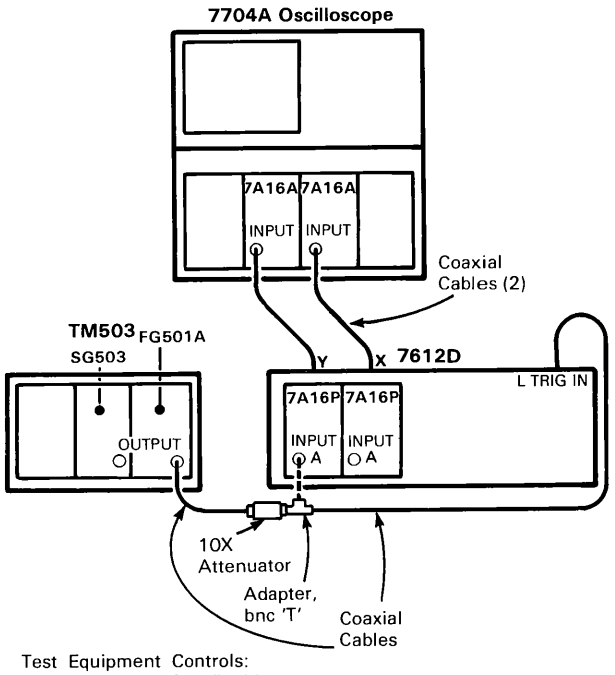
G7. CHECK/ADJUST EXTERNAL TRIGGER

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G7. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 100E-9
- TRIGGER FUNCTIONS
  - SOURCE ..... EXT



Test Equipment Controls:

7A16P Amplifier (both)
- Volts/Div 50mV
- Input 1MΩ
- Coupling ..... AC
- Bandwidth ..... Full

FG 501A Function Generator
- Frequency Hz 5
- Multiplier ..... 10^4
- Function ..... ~(sinewave)
- Offset ..... Pressed in
- Amplitude ..... Minimum

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A16A Amplifiers (both)
- Volts/Div 0.1
- Coupling ..... DC
- Bandwidth ..... Full
- Polarity ..... +Up
- Position ..... Centered

2387-592

a. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude for an XY display of one major division in amplitude on the 7704A.

b. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the following eight Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	AC	Off
3. +	DC	On
4. +	DC	Off
5. −	AC	On
6. −	AC	Off
7. −	DC	On
8. −	DC	Off

Set the vertical Position and TRIGGER LEVEL controls as necessary to verify triggering.

c. **ADJUST**—Offset (R702), for a triggered XY display (L TRIGGER light on) and balanced + and − SLOPE trigger points in the eight Trigger modes listed in part b.

d. Change the FG 501A to 40 Hz.

e. Set the 7612D SAMPLE INTERVAL to 100E-6.

f. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude for an XY display of one major division on the 7704A.

g. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the eight following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	AC	Off
3. +	DC	On
4. +	DC	Off
5. −	AC	On
6. −	AC	Off
7. −	DC	On
8. −	DC	Off

Set the Vertical Position and TRIGGER LEVEL controls as necessary for stable triggering.

h. Change the 7612D to:

SAMPLE INTERVAL 100E-9
HF REJ . . . . . Off

i. Connect the SG 503 in place of the FG 501A and set it to 50 MHz.

j. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude to cause a one-major-division XY display on the 7704A.

k. **CHECK**—for a triggered XY display (L TRIGGERED light on) in the four following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

Set Vertical Position and TRIGGER LEVEL as necessary for stable triggering.

l. Change the SG 503 to 100 MHz.

m. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude to cause a two-major-division XY display on the 7704A.

n. Set the 7612D SAMPLE INTERVAL to 30E-9. Set the Vertical position and TRIGGER LEVEL as necessary for stable triggering.

o. **CHECK**—for a triggered XY display (L TRIGGERED Light on) in the four following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	Off
2. +	DC	Off
3. −	AC	Off
4. −	DC	Off

p. Move the bnc "T" adapter from the CHANNEL A vertical input to the CHANNEL B vertical input, and move the coaxial cable from the L TRIG IN to the R TRIG IN connector.

q. Connect the FG 501A in place of the SG 503.

r. Set the 7612D to:

TRIGGERING LEVEL 200
PROGRAM . . . . . CHANNEL B
SAMPLE INTERVAL 100E-9

s. Set the FG 501A to 50 kHz.

t. While repeatedly pressing the ARM B button, adjust the FG 501A Amplitude to cause a one-major-division XY display on the 7704A.

u. **CHECK**—for a triggered XY display (R TRIGGERED light on) in the eight following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	AC	Off
3. +	DC	On
4. +	DC	Off
5. −	AC	On
6. −	DC	Off
7. −	AC	On
8. −	DC	Off

Set the Vertical Position and TRIGGER LEVEL as necessary for stable triggering.

v. **ADJUST**—Offset (R204) for a triggered XY display (R TRIGGER light on) and balanced + and − SLOPE trigger points in the eight Trigger modes listed in part u.

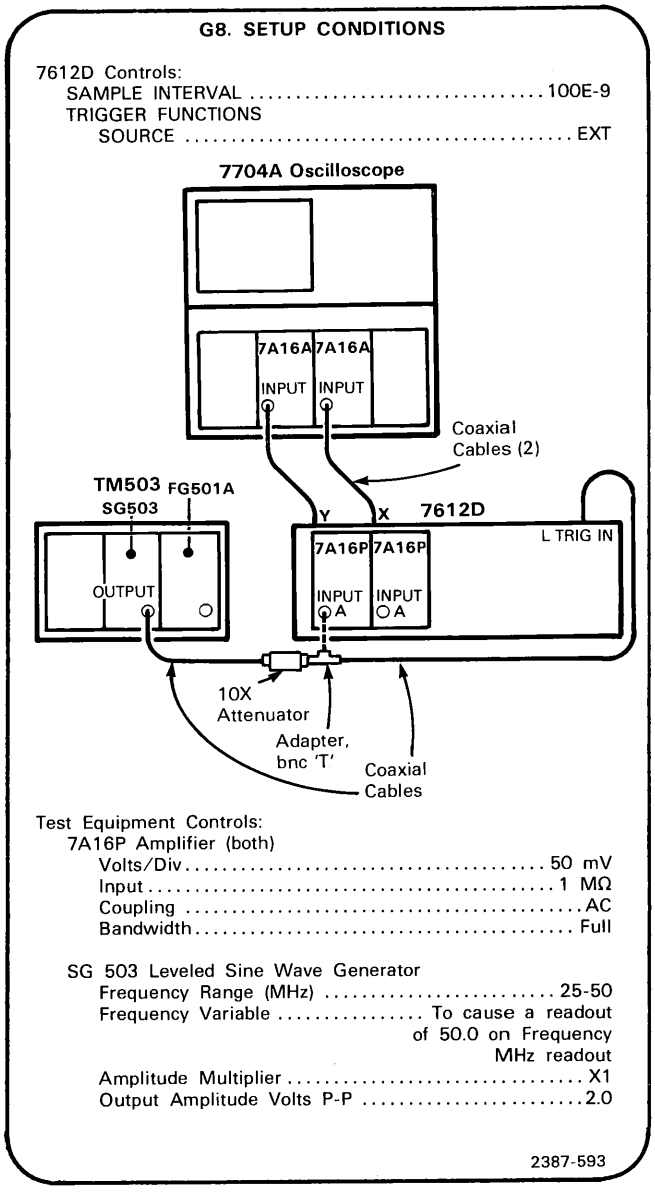
w. Repeat parts d through o, using the R TRIGGER light and the ARM button.

x. Replace the 7612D top cover.

G8. CHECK EXTERNAL HIGH-FREQUENCY REJECT

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. While repeatedly pressing the ARM A button, adjust the SG 503 Output Amplitude to cause a three-major-division XY display on the 7704A.

b. Set the 7612D HF REJ to on (lighted).

c. **CHECK**—that the trigger circuit will not operate (L TRIGGERED light stays off) in the four following Trigger modes:

SLOPE	COUPLING	HF REJ
1. +	AC	On
2. +	DC	On
3. −	AC	On
4. −	DC	On

d. Move the SG 503 inputs to the CHANNEL B and R TRIG IN connectors.

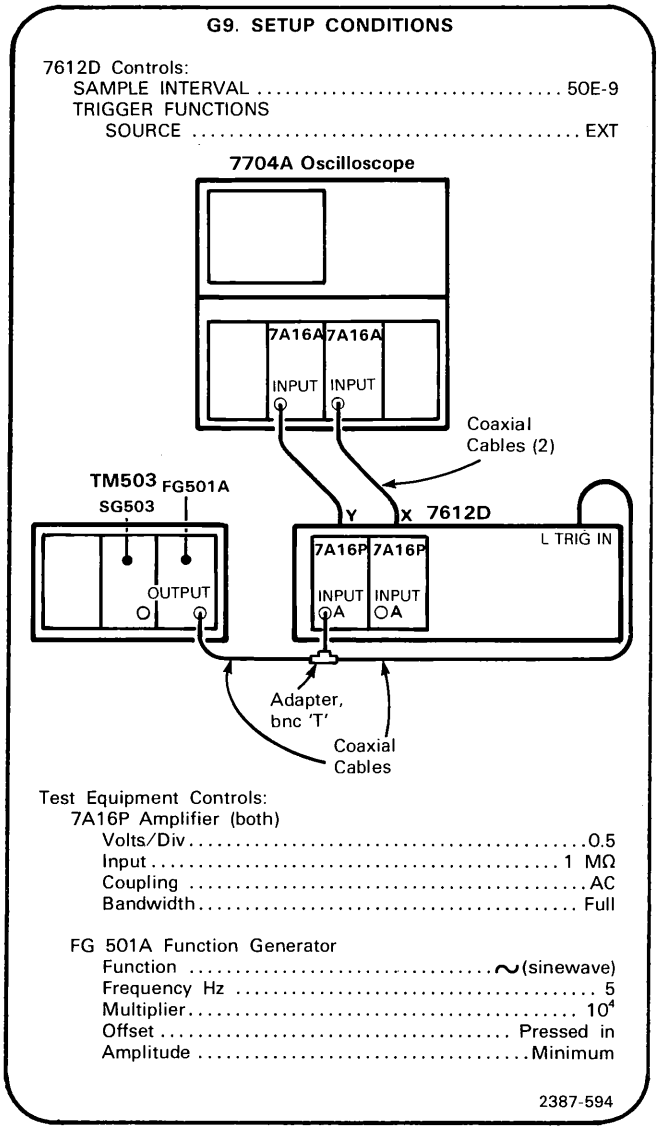
e. Press the COPY button, then press the PROGRAM CHANNEL B button.

f. **CHECK**—that the trigger circuit will not operate (R TRIGGER light stays off) in the four Trigger modes listed in part c.

G9. CHECK EXTERNAL TRIGGER LEVEL RANGE

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. While repeatedly pressing the ARM A button, adjust the FG 501A Amplitude control to cause a 5.12-major-division XY display on the 7704A.

b. **CHECK**—the 7704A for a triggered XY display (7612D L TRIGGERED light on) that varies, while changing the 7612D TRIGGER LEVEL and pressing the ARM A button, from a base level (00) to a maximum positive level, then back to the base level and on to a maximum negative level. See Figure 5-5.

c. Disconnect the inputs from the CHANNEL A and L TRIG IN connectors, and connect them to the CHANNEL B input and rear-panel R TRIG IN connectors, respectively.

d. Press the 7612D COPY button, then press PROGRAM CHANNEL B.

e. Repeat parts a and b, using the ARM B button and the R TRIGGERED light.

H. TIME BASE

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
2. Amplifier, 7A19
3. Amplifier, 7A16A (two needed)
4. Programmable Amplifier, 7A16P (two needed)
6. Time Base, 7B80
9. Probe, P6053B
12. Pulse Generator, PG 502
15. Power Module Mainframe TM 503
18. Coaxial Cable, Precision

H1. TIME BASE PRELIMINARY SETUP

a. Remove the 7612D top cover.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS H page in Section 8, Diagrams and Circuit Board Illustrations.

H2. CHECK EXTERNAL CLOCK INPUT

NOTE

First perform step H1, then proceed.

a. Connect and set the equipment as shown in H2. SETUP CONDITIONS.

b. Disconnect the PG 502 cable from the 7A19 input and connect the cable to the 7612D EXT CLOCK IN connector on the rear panel.

c. Connect the test oscilloscope 7A16A to the probe, and connect the probe to the integrated circuit end of R302 on the right Data Storage Board (A18) of Channel A. Connect the probe ground lead to TP 202.

d. Change the test oscilloscope Vertical Mode to Right.

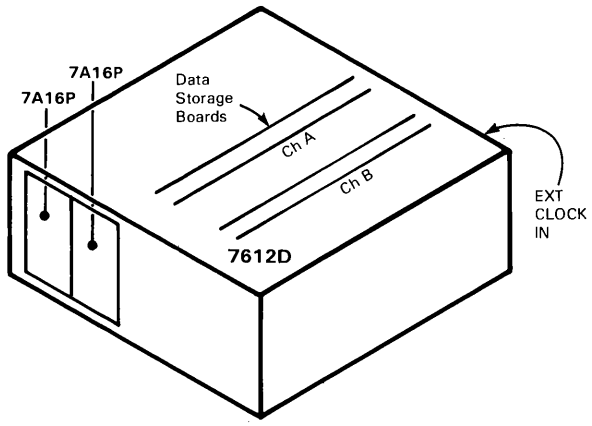
e. Press the ARM A button. The L TRIGGERED light should be off.

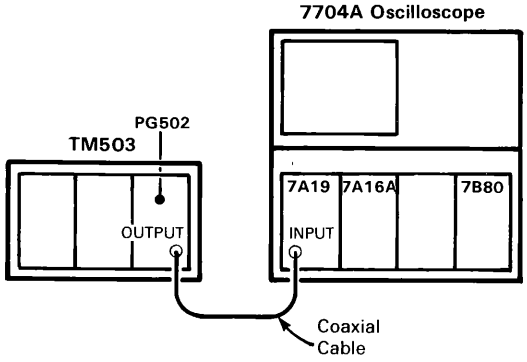
f. Set the 7B80 Time Base to 20 ns/Div.

g. **CHECK**—the test oscilloscope display for one pulse every 40 ns (the 200 MHz input is divided by eight).

H2. SETUP CONDITIONS

7612D Controls:
- INSTRUMENT FUNCTION
  - CLK ..... EXT
- TRIGGER FUNCTIONS
  - HF REJ ..... ON
- SAMPLE INTERVAL ..... IE+0 (MULTIPLIER)





Test Equipment Controls:
- 7A16P Amplifier (both) ..... As desired

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal mode ..... B
- B Trigger Source ..... Vert Mode
- Intensity, Focus, Readout ..... As needed for good display

7A19 Amplifier
- Volts/Div 0.5
- Coupling ..... DC
- Polarity ..... +Up

7B80 Time Base
- Time/Div ..... 5 ns
- Mag X1
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... Int

7A16A Amplifier in 7704A
- Volts/Div ..... 50 mV
- Coupling ..... AC
- Polarity ..... +Up
- Bandwidth ..... Full

PG 502 Pulse Generator
- Pulse Duration ..... ≤2ns
  - Variable ..... X1 (ccw)
- Period ..... ≤4 ns
  - Variable ..... For 200 MHz waveform (5 ns period) on test oscilloscope
- Output (Volts)
  - Low Level ..... Set bottom of waveform to -0.3V
  - High Level ..... Set top of waveform to +1.4V

2387-595

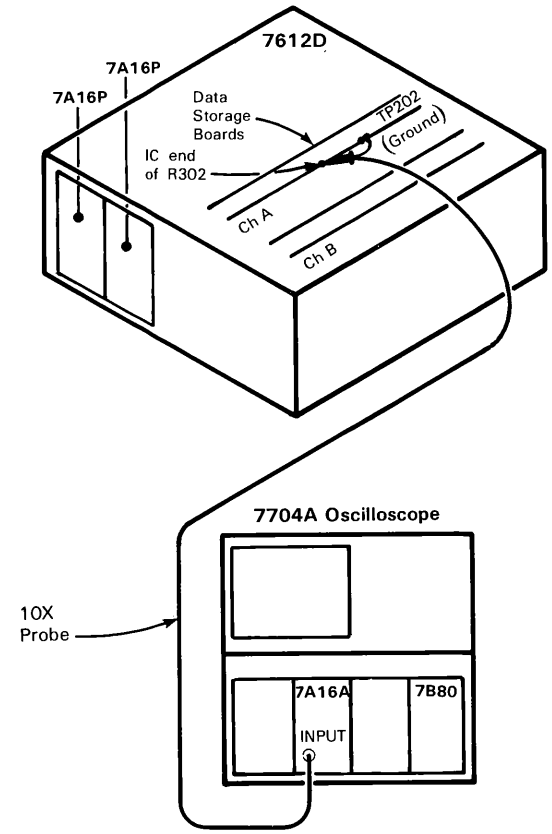
H3. CHECK INTERNAL/EXTERNAL SAMPLING INTERVAL

NOTE

If the preceding step was not performed, first perform step H1, then proceed.

H3. SETUP CONDITIONS

7612D Controls:
TRIGGER FUNCTIONS
HF REJ ..... ON



Test Equipment Controls:
7A16P Amplifier (both) ..... As desired
7704A Oscilloscope
Vertical Mode ..... Right
Horizontal Mode ..... B
B Trigger Source ..... Vert Mode
7A16A Amplifier
Volts/Div ..... 50 mV
Coupling ..... AC
Polarity ..... +Up
Bandwidth ..... Full
7B80 Time Base
Time/Div ..... 20 ns
Mag X1
Triggering
Mode ..... Norm
Coupling ..... AC
Source ..... Int

2387-596

a. Press ARM A (the L TRIGGERED light should be off).

b. **CHECK**—the test oscilloscope display for one pulse every 40 ns (the 200 MHz input is divided by eight).

c. Set the 7612D for:
SAMPLING 10E-9

d. Press ARM A.

e. **CHECK**—the test oscilloscope display for pulses every 80 ns.

f. Repeat parts b through d to check the sampling intervals shown in Table 5-8.

TABLE 5-8
7612D Sampling Interval & Test Oscilloscope Display

7612D Sampling Interval	Test Oscilloscope Time/Div (Seconds)	Period of Displayed Waveform
20E-9	50 nano	160 ns
30E-9	50 nano	240 ns
40E-9	50 nano	325 ns
50E-9	50 nano	400 ns
60E-9	0.1 micro	.470 μs
70E-9	0.1 micro	.560 μs
80E-9	0.1 micro	.640 μs
90E-9	0.1 micro	.720 μs
100E-9	0.1 micro	.800 μs
1E-6	1 micro	8 μs
10E-6	10 micro	80 μs
100E-6	0.1 milli	.8 μs
1E-3	1 milli	8 ms
10E-3	10 milli	80 ms
100E-3	0.1 sec	.800 s
200E-3	0.2 sec	1.6 s
1E-0	1 sec	8 s

g. Move the test oscilloscope probe to:
7A16A Amplifier ..... Integrated circuit end of R302 on the right Data Storage Board (A18) of Channel B. Connect probe ground lead to TP202.

h. Change the 7612D controls as follows:
INSTRUMENT FUNCTION
PROGRAM ..... CHANNEL B

i. Set the test oscilloscope time base to 20 ns/Div.

j. Repeat parts a through f using the ARM B button.

k. Disconnect the probe from the 7612D.

l. Replace the 7612D top cover.

I. TIME-MEASUREMENT ACCURACY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
9. Probe, P6053B
7. Counter, 7D15

I1. TIME-MEASUREMENT ACCURACY PRELIMINARY SETUP

a. Remove the 7612D top cover.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS I page in Section 8, Diagrams and Circuit Board Illustrations.

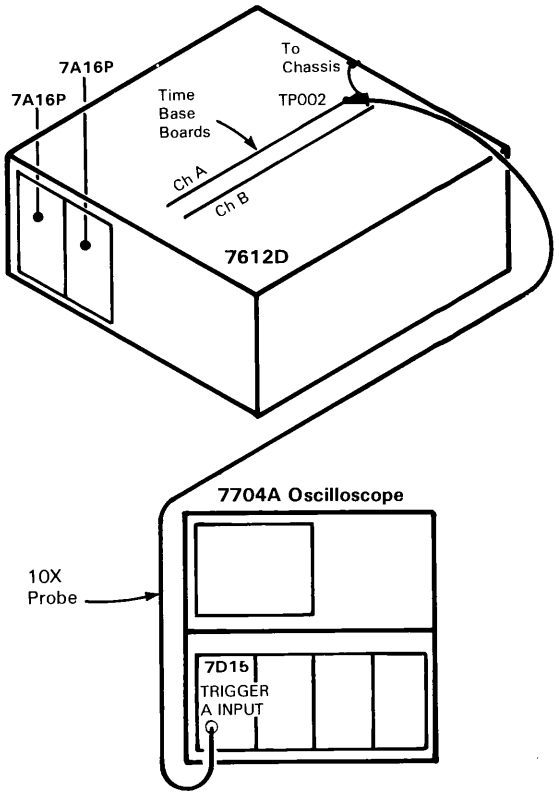
I2. CHECK ACCURACY OF TIME BASE A

NOTE

First perform step I1, then proceed.

I2. SETUP CONDITIONS

7612D Controls:
TRIGGER FUNCTIONS
SELECT ..... L or R



Test Equipment Controls:
7A16P Amplifiers (both) ..... As desired

7704A Oscilloscope
Readout ..... For good display of 7D15 readout

7D15 Counter
Gate ..... Norm
Mode ..... Tim Width A
Averg X1
Clock ..... 1 μs
Trigger A ..... -Slope, DC Coupl
P-P Sens ..... 0.1 V
Display Waveform switch ..... Pseudo Gate
Display Time ..... Fully clockwise

2387-597

a. Enter the Breakpoint and Sample Interval data from Table 5-9 into the 7612D memory as follows:

1. Press the BREAKPOINT SET button.
2. Press the DECREMENT/INCREMENT buttons to set the BREAKPOINT LOCATION readout to 0000 to start the sequence.
3. Press the SAMPLE INTERVAL button.
4. Use the DECREMENT/INCREMENT buttons to set the SAMPLE INTERVAL display to correct sample interval listed for that breakpoint.
5. Press the ARM A button to enter the pair of settings into the 7612D memory.
6. Press BREAKPOINT SET button and use DECREMENT/INCREMENT buttons to set the next breakpoint location.
7. Repeat subparts 3 through 6 until entire table is entered.
8. Press the 7612D COPY button. This will transfer all the breakpoint locations and sample intervals for Channel A into Channel B.

b. Connect the 10X probe from the 7D15 Trigger A input to TP002 on the A Time Base Board (A20).

TABLE 5-9
Sample Intervals and Breakpoints

Breakpoint Location	Sample Interval
0	10E-9
16	10E-3
96	1E-3
208	500E-6
368	40E-6
560	1E-6
808	300E-9
816	4E-6
824	10E-9
1024	1E-3
2024	2E-6
2040	400E-9

c. Press the 7D15 Reset button, and rotate the A Trigger Level clockwise until the Gate indicator lights. Rotate the Level control counterclockwise until the Gate indicator just extinguishes.

d. Press the 7D15 Reset button. The readout on the crt should now be all zeros.

e. Press ARM A and MAN TRIG on the 7612D.

f. **CHECK**—that the counter readout is between 2000.070 ms and 1999.930 ms (2000 ms ±.0035%).

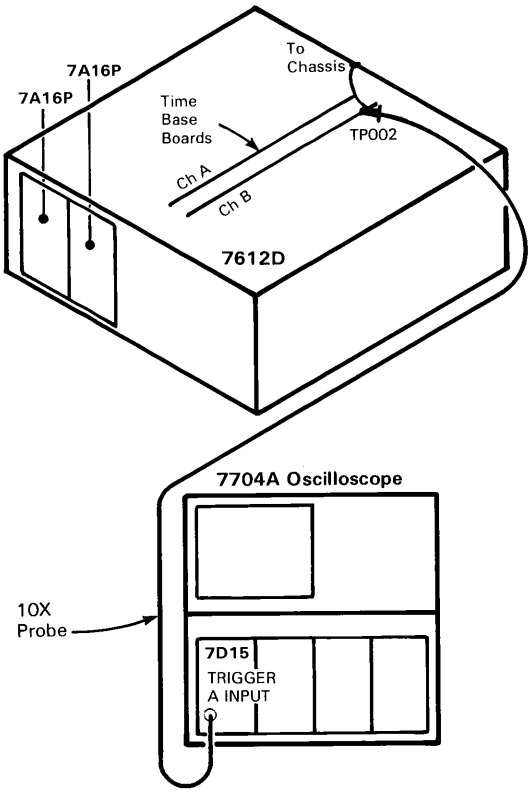
I3. CHECK ACCURACY OF TIME BASE B

NOTE

If the preceding step was not performed, first perform step I1, then proceed.

I3. SETUP CONDITIONS

7612D Controls:
TRIGGER FUNCTIONS
SELECT ..... L or R



Test Equipment Controls:
7A16P Amplifier (both)
7704A Oscilloscope
Readout ..... For good display of 7D15 readout

7D15 Counter
Gate ..... Norm
Mode ..... Tim Width A
Averg X1
Clock ..... 1 μs
Trigger A ..... -Slope, DC Coupl
P-P Sens ..... 0.1 V
Display Waveform Switch ..... Pseudo Gate
Display Time ..... Fully clockwise

2387-598

a. Enter the Breakpoint and Sample Interval data from Table 5-9 (step I2) into the 7612D memory as follows: (If you performed step I2, skip this procedure and go directly to part b.)

1. Press the BREAKPOINT SET button.
2. Press the DECREMENT/INCREMENT buttons to set the BREAKPOINT LOCATION readout to 0000 to start the sequence.
3. Press the SAMPLE INTERVAL button.
4. Use the DECREMENT/INCREMENT buttons to set the SAMPLE INTERVAL display to correct sample interval corresponding to that breakpoint.
5. Press the ARM A button to enter the pair of settings into the 7612D memory.
6. Press BREAKPOINT SET button and use DECREMENT/INCREMENT buttons to set the next breakpoint location.
7. Repeat subparts 3 through 6 until entire table is entered.

b. Connect the 10X probe from the 7D15 Trigger A input to TP002 on the B Time Base Board.

c. Press the 7D15 Reset button, and rotate the A Trigger Level clockwise until the Gate indicator lights. Rotate the Level control counterclockwise until the Gate indicator just extinguishes.

d. Press the Reset button. The readout should be all zeros.

e. Press PROGRAM CHANNEL B, ARM B, and MAG TRIG.

f. **CHECK**—that the counter readout is between 2000.070 ms and 1999.930 ms (2000 ms ±.0035%).

g. Replace the 7612D top cover.

J. MONOTONICITY

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
2. Amplifier, 7A19 (two needed)
5. Differential Amplifier, 7A22 (two needed)
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
16. Display Monitor
17. Coaxial Cables (four needed)

J1. MONOTONICITY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

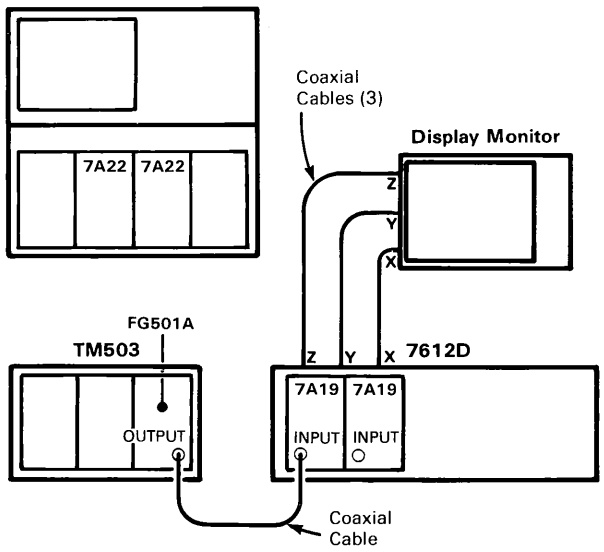
J2. CHECK CHANNEL A MONOTONICITY

NOTE

First perform step J1, then proceed.

J2. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 20E-9
- PROGRAM ..... CHANNEL A
- TRIGGER FUNCTIONS
  - SELECT ..... R
  - SLOPE ..... –
  - HF REJ ..... On



Test Equipment Controls:

7A19 Amplifer (both)
- Volts/Div 0.2
- Coupling ..... DC
- Polarity ..... +Up
- Position ..... Centered

FG501A Function Generator
- Frequency Hz 3
- Multiplier ..... 10^5
- Function .....
- Offset ..... Pressed in

7704A Oscilloscope
- Vertical Mode ..... Right
- Horizontal Mode ..... A

7A22 Differential Amplifiers

	Right Vert	A Horiz
Volts/Div	2 mV	5 mV
HF-3dB Point	0.3 MHz	0.3 MHz
LF-3dB Point	DC Offset	DC Offset
Coupling		
+Input	DC	DC
-Input	Gnd	Gnd

2387-599

a. While repeatedly pressing the ARM A button, increase the FG 501A output amplitude until the waveform display on the monitor reaches, and goes slightly past, either top or bottom of the display area.

b. Continue pressing the ARM A button and use the Channel A 7A19 Position control to center the waveform in the Monitor's display area.

c. Continue pressing the ARM A button and adjust the FG 501A Amplitude control until the waveform blanks equally at the top and bottom of the ramp. See Figure 5-17.

d. Set the 7704A as follows:

A Intensity . . . . . Visible display

e. Disconnect the X and Y cables from the monitor and connect the them to the + inputs of the test oscilloscope's A Horiz and Right Vert 7A22's, respectively.

f. Set both 7A22 Offset controls to obtain a waveform display similar to that shown in Figure 5-18a.

g. **CHECK**—that the ramp steps ascend progressively (see Fig. 5-18a) as you rotate the left and right 7A22 Offset controls with no decrease in step levels (see Fig. 5-18b) across the entire ramp.

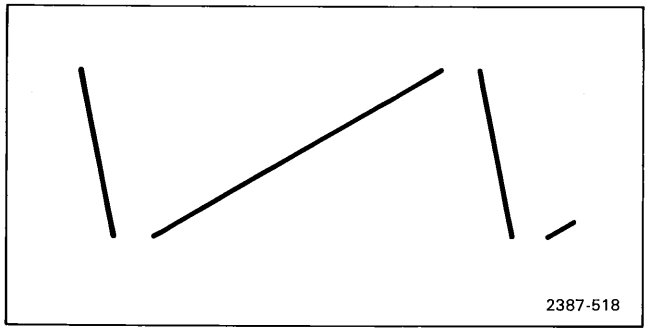


Fig. 5-17. Ramp blanked equally at top and bottom.

J3. CHECK CHANNEL B MONOTONICITY

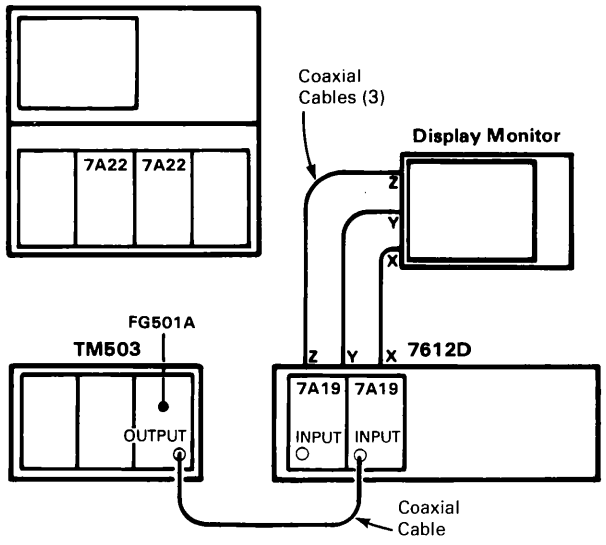
NOTE

If the preceding step was not performed, first perform step J1, then proceed.

J3. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 20E-9
- PROGRAM . . . . . CHANNEL B
- TRIGGER FUNCTIONS
  - SELECT . . . . . R
  - SLOPE . . . . . -
  - HF REJ . . . . . On

7704A Oscilloscope

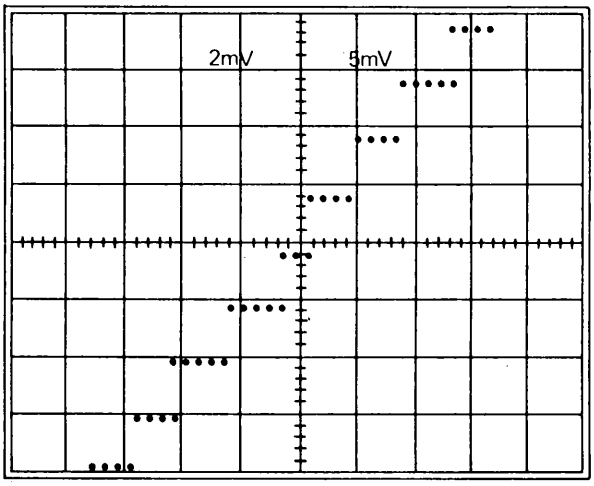


Test Equipment Controls:
- 7A19 Amplifer (both)
  - Volts/Div 0.2
  - Coupling . . . . . DC
  - Polarity . . . . . +Up
  - Position . . . . . Centered
- FG501A Function Generator
  - Frequency Hz 3
  - Multiplier . . . . . 10^5
  - Function . . . . .
  - Offset . . . . . Pressed in
- 7704A Oscilloscope
  - Vertical Mode . . . . . Right
  - Horizontal Mode . . . . . A
- 7A22 Differential Amplifiers

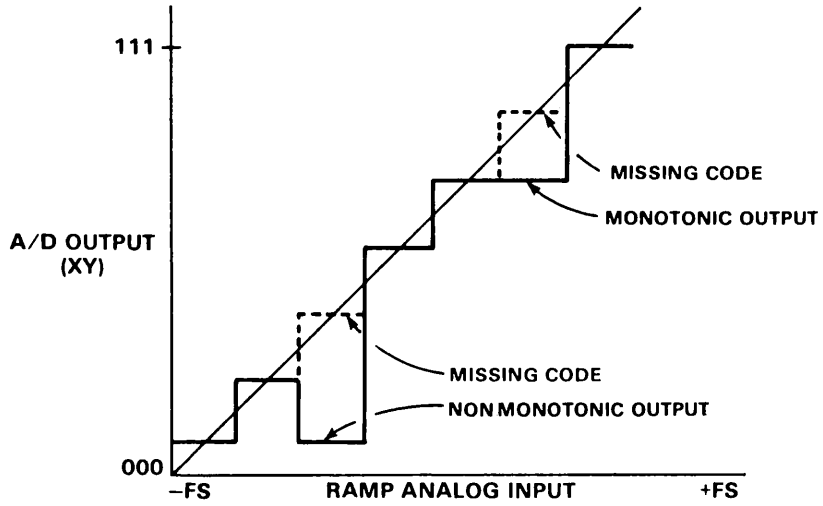
	Right Vert	A Horiz
Volts/Div	2 mV	5 mV
HF-3dB Point	0.3 MHz	0.3 MHz
LF-3dB Point	DC Offset	DC Offset
Coupling		
+Input	DC	DC
-Input	Gnd	Gnd

2387-600

a. While repeatedly pressing the ARM B button, increase the FG 501A Amplitude until the waveform displayed on the monitor reaches, and goes slightly past, either top or bottom of the display area.



a. Monotonic XY output display.



b. Nonmonotonic output.

2387-519

Fig. 5-18. Monotonic and nonmonotonic outputs.

b. Continue pressing the ARM B button and use the Channel B 7A19 Position control to center the waveform in the monitor's display area.

c. Continue pressing the ARM B button and adjust the FG 501A Amplitude control until the waveform blanks equally at top and bottom of the ramp. See Figure 5-19.

d. Disconnect the X and Y cables from the monitor and connect them to the + inputs of the test oscilloscope's A Horiz and Right Vertical 7A22s respectively.

e. Set both 7A22 Offset controls to obtain a waveform display similar to that shown in Figure 5-20a.

f. **CHECK**—that the ramp steps ascend progressively (see Fig. 5-20a) as you rotate the left and right 7A22 Offset controls with no decrease in step levels (see Fig. 5-20b) across the entire ramp.

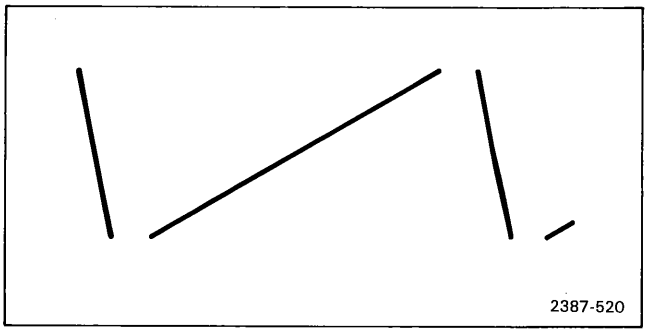
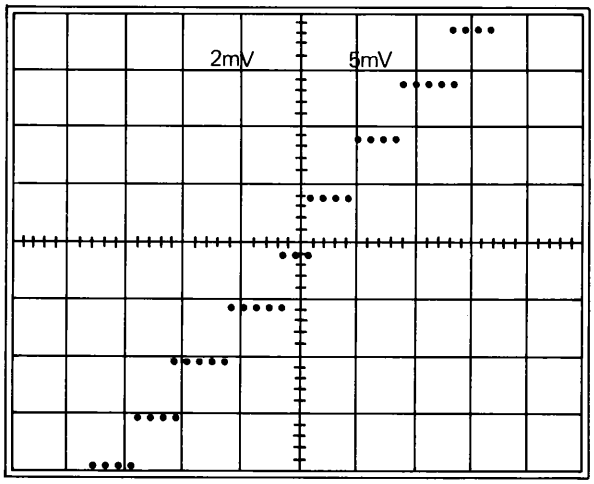
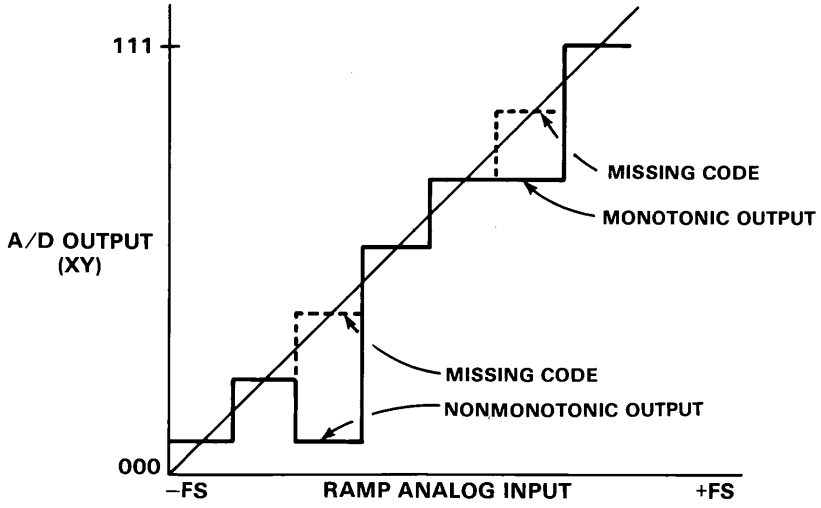


Fig. 5-19. Ramp blanked equally at top and bottom.



a. Monotonic XY output display.



b. Nonmonotonic output.

2387-521

Fig. 5-20. Monotonic and nonmonotonic outputs.

K. VERTICAL

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
6. Time Base, 7B80
11. Digital Multimeter, DM 501A
14. Sine-Wave Generator, SG 503
15. Power Module Mainframe, TM 503
17. Coaxial Cable (three needed)
18. Coaxial Cable, Precision
19. Calibration Fixture

K1. VERTICAL PRELIMINARY SETUP

a. Remove the 7612D right side cover for steps K2, K3, K4, K5, K7 and K8 only.

b. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

c. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

d. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

e. See the TEST POINT AND ADJUSTMENT LOCATIONS K page in Section 8, Diagrams and Circuit Board Illustrations.

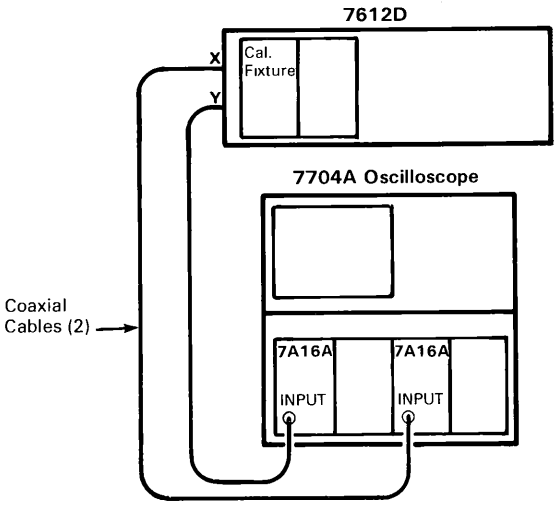
K2. CHECK/ADJUST CHANNEL A CENTERING

NOTE

First perform step K1, then proceed.

K2. SETUP CONDITIONS

7612D Controls:
Make no change to the control settings.



Test Equipment Controls:
Calibration Fixture
Test ..... Aux In

7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Polarity	+Up	+Up
Position	9 o'clock	Centered

2387-601A

a. Connect the outpjut of the SG 503 to the Aux In connector on the Calibration Fixture with a coaxial cable.

b. Set the SG 503 as follows:

Frequency ..... 50 kHz
Output Amplitude ..... 600 mV
Output Multiplier X1

c. While repeatedly pressing the ARM A button, adjust the left vertical 7A16A Position and Variable Volts/Div controls to obtain a clipped sine-wave display eight divisions high (Fig. 5-9a shows the desired waveform).

d. Disconnect the signal from the Calibration Fixture.

e. Set the Calibration Fixture to Vert or Horiz Com Mode.

f. Press ARM A.

g. Press MAN TRIG.

h. **CHECK**—that the trace on the test oscilloscope is at graticule center +0.75 minor divisions (+5 LSB's).

i. **ADJUST**—Centering (R408) to position the trace to graticule center while repeatedly pressing the ARM A button.

j. Set the DMM to 200 V range and measure the collector voltages on the cases of transistors Q508 and Q518. Average the two voltages. The result should be 27.8 + or −0.2 V.

k. **ADJUST**—DC Level (R407), to obtain an average Voltage of 27.8 V + or −0.2 V.

l. Repeat parts a through f as necessary to eliminate interaction.

m. Replace the 7612D right side cover.

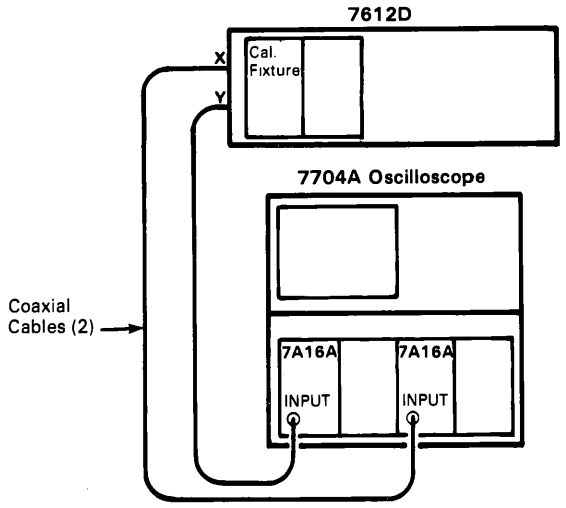
K3. CHECK/ADJUST CHANNEL A GAIN

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K3. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 20E-6



Test Equipment Controls:
Calibration Fixture
Test ..... Vert or Horiz Gain
Rep Rate ..... 1 kHz

7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Polarity	+Up	+Up
Position	9 o'clock	Centered

2387-602

a. Press the SAMPLE INTERVAL button.

b. Use the DECREMENT/INCREMENT controls to set the A SAMPLE INTERVAL to 20E-6.

c. Press the COPY button.

d. Press the ARM A button.

e. Use the left vertical 7A16A Position control to set the bottom of the staircase waveform to the bottom graticule line.

f. Move the left vertical 7A16 Variable Volts/Div control to set the top staircase step at the top graticule line. See Figure 5-21.

g. Observe that the longest lines are at the center graticule line on the test oscilloscope.

h. If the longest lines do not align with the center graticule line, repeatedly press the ARM A button while adjusting the calibration fixture Position control to bring the longest lines to the center graticule line.

i. **CHECK**—that each of the marks from −3 divisions to +3 divisions aligns with the appropriate graticule line (see Fig. 5-21).

j. Use the left 7A16A Position control to align the first stairstep with the first graticule line (see Fig. 5-21).

k. **CHECK**—that the sixth step aligns with the sixth graticule line, + or − 0.1 division (see Fig. 5-21).

NOTE

This CHECK will verify that the gain is within ±2% of specified value. When Gain is adjusted according to the ADJUST procedure that follows, it will be accurate to ±2 LSB.

l. **ADJUST**—Gain (R612) while repeatedly pressing the ARM button so that the middle six staircase steps align with the graticule lines. See Figure 5-21.

m. **ADJUST**—Gain (R612) clockwise while repeatedly pressing the ARM button to reduce the gain so that the top and bottom staircase steps separate and part of each moves toward the center of the display. See Figure 5-22. (In Fig. 5-22, the top step of the waveform moved down three LSBs and the bottom step moved up two LSBs.)

n. **ADJUST**—Gain (R612) counterclockwise very gradually while repeatedly pressing ARM A until the two line segments at the top and the bottom of the display just become single lines. DO NOT ADJUST R612 PAST THIS POINT.

o. Replace the 7612D right side cover.

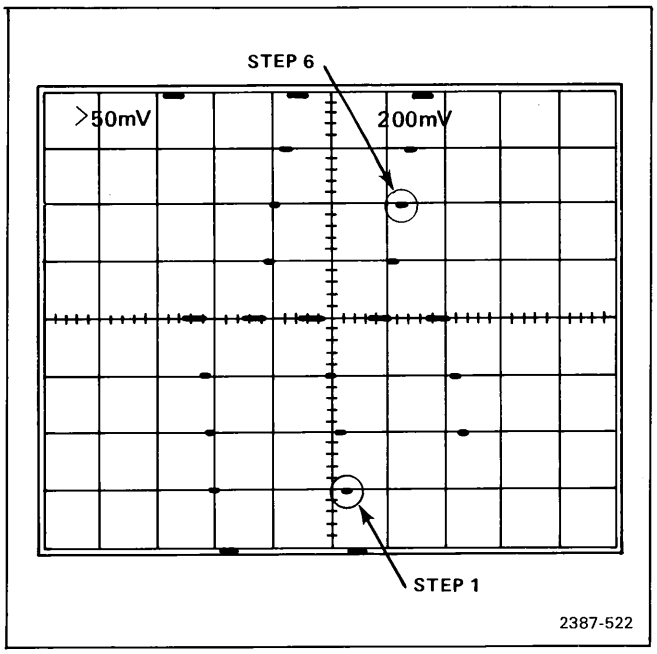


Fig. 5-21. Display of staircase waveform with its top and bottom steps set to the top and bottom graticule lines.

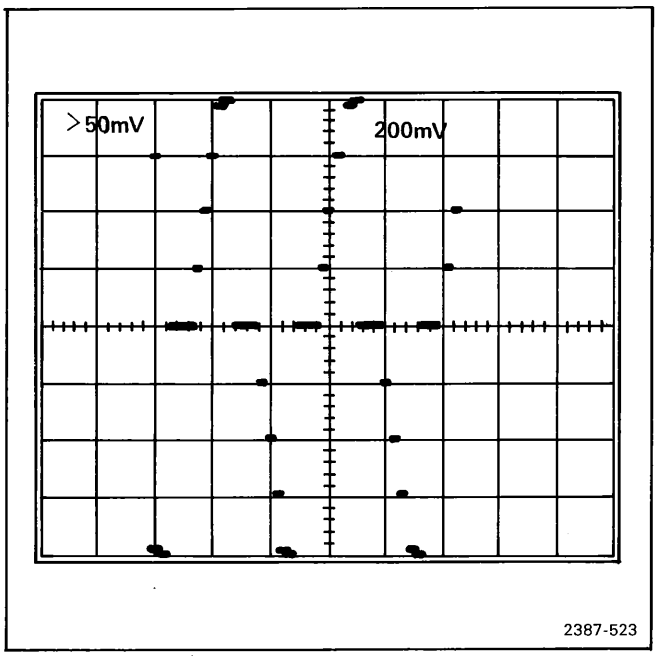
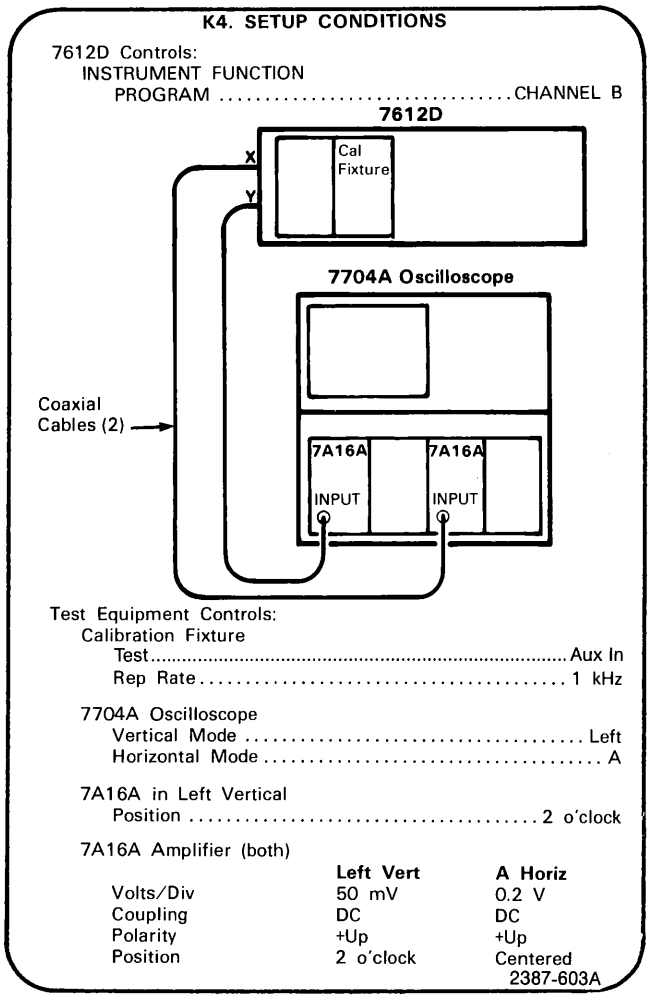


Fig. 5-22. Display of staircase waveform with Gain reduced just enough to cause the top and bottom steps to separate.

K4. CHECK/ADJUST CHANNEL B CENTERING

NOTE

If the preceding step was not performed, first perform step K1, then proceed.



a. Connect the output of the SG 503 to the Aux In connector on the Calibration Fixture with a coaxial cable.

b. Set the SG 503 as follows:

Frequency ..... 50 kHz
Output Amplitude ..... 600 mV
Output Multiplier X1

c. While repeatedly pressing the ARM B button, adjust the left vertical 7A16A Position and Variable Volts/Div controls to obtain a clipped sine-wave display eight divisions high (Fig. 5-9a shows the desired waveform).

d. Disconnect the signal from the Calibration Fixture.

e. Set the Calibration Fixture to Vert or Horiz Com Mode.

f. Press the ARM B button.

g. Press the MAN TRIG button.

h. **CHECK**—that the trace on the test oscilloscope is at graticule center + or − 0.75 minor divisions (+ or − five LSBs).

i. **ADJUST**—Centering (R531) to position the trace to graticule center while repeatedly pressing the ARM B button.

j. Set the DMM to 200 V range and measure the collector voltages on the cases of transistors Q534 and Q546. Add the two voltages and divide by two. The result should be 27.8 ±0.2 V.

k. **ADJUST**—DC LEVEL (R524), to obtain an average voltage of +27.8 ±0.2 V.

l. Repeat parts f through k as necessary to eliminate interaction.

m. Replace the 7612D right side cover.

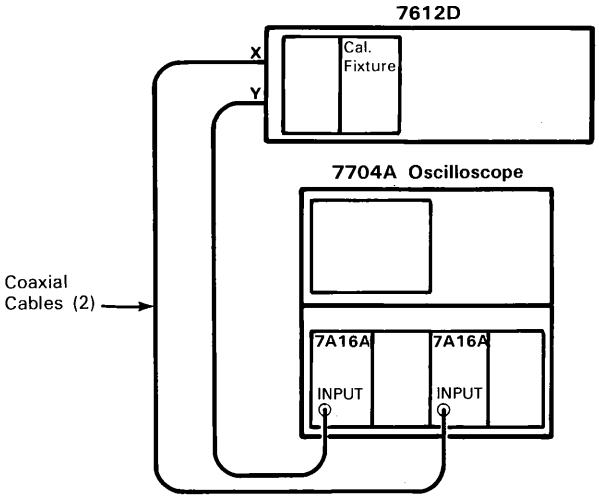
K5. CHECK/ADJUST CHANNEL B GAIN

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K5. SETUP CONDITIONS

7612D Controls:
- TRIGGER FUNCTIONS
  - SELECT ..... R
- SAMPLE INTERVAL 20E-6
- INSTRUMENT FUNCTION
  - PROGRAM ..... CHANNEL B



Test Equipment Controls:
- Calibration Fixture
  - Test ..... Vert or Horiz Gain
  - Rep Rate ..... 1 kHz
- 7704A Oscilloscope
  - Vertical Mode ..... Left
  - Horizontal Mode ..... A
- 7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Polarity	+Up	+Up
Position	9 o'clock	Centered

2387-604

a. Press the SAMPLE INTERVAL button.

b. Press the PROGRAM CHANNEL B button.

c. Use the DECREMENT/INCREMENT controls to set the B SAMPLE INTERVAL to 20E-6.

d. Press the ARM B button.

e. Use the 7A16A Position control to set the top of the staircase waveform to the top graticule line.

f. Move the 7A16A Variable Volts/Div control to set the bottom staircase step at the bottom graticule line. See Figure 5-23.

g. Observe that the longest lines are at the center graticule line on the test oscilloscope.

h. If the longest lines to not align with the center graticule line, repeatedly press the ARM B button while adjusting the calibration fixture Position control to bring the longest lines to the center graticule line.

i. **CHECK**—that each of the marks from −3 divisions to +3 divisions aligns with the appropriate graticule line.

j. Use the 7A16A Position control to align the first stairstep with the first graticule line (see Fig. 5-23).

k. **CHECK**—that the sixth step aligns with the sixth graticule line, + or − 0.1 division (See Fig. 5-23).

NOTE

This CHECK will verify that the gain is within ±2% of specified value. When Gain is adjusted according to the ADJUST procedure that follows, it will be accurate to ±2 LSB.

l. **ADJUST**—Gain (R636) clockwise while repeatedly pressing the ARM B button to reduce the gain so that the top and bottom staircase steps separate and part of each moves toward the center of the display. See Figure 5-24. (In Fig. 5-24 the top part of the waveform moved down three LSBs and the bottom part moved up two LSBs.)

m. **ADJUST**—Gain (R636) counterclockwise very gradually while repeatedly pressing ARM B until the two line segments at the top and bottom of the display just become single lines. DO NOT ADJUST R636 PAST THIS POINT.

n. Replace the 7612D right side cover.

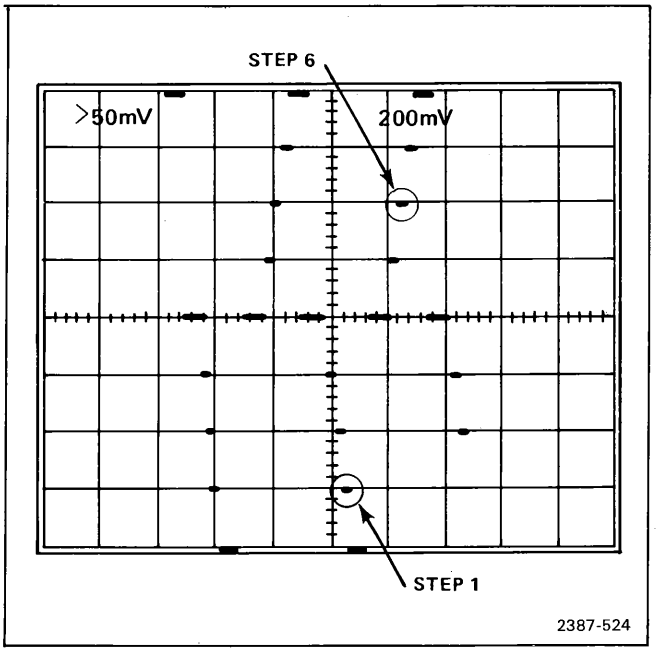


Fig. 5-23. Display of staircase waveform with its top and bottom steps set to the top and bottom graticule lines.

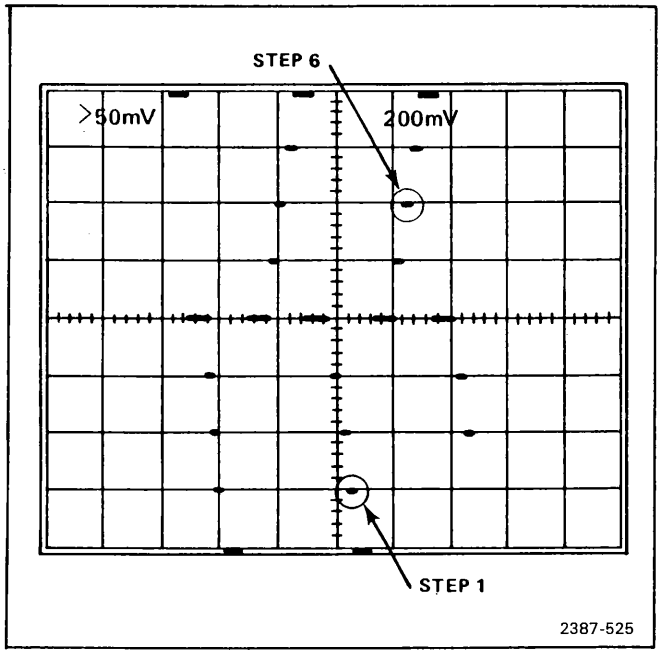


Fig. 5-24. Display of staircase waveform with Gain reduced just enough to cause the top and bottom steps to separate.

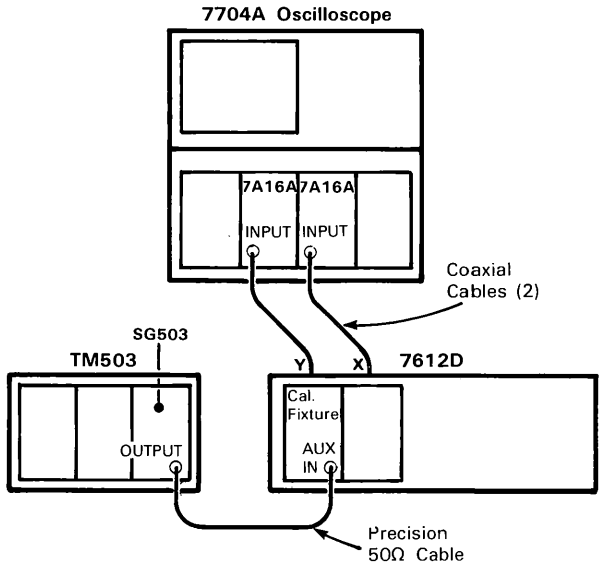
K6. CHECK CHANNEL ISOLATION

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K6. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 50E-9



Test Equipment Controls:
Calibration Fixture
Test ..... Vert or Horiz Freq Resp
Position ..... Centered
Amplitude ..... Fully Clockwise

7704A Oscilloscope
Vertical Mode ..... Right
Horizontal Mode ..... A

7A16A Amplifiers (both)
Volts/Div ..... 50 mV
Coupling ..... DC
Polarity ..... +Up
Bandwidth ..... Full

SG503 Leveled Sine Wave Generator
Frequency Range MHz ..... Ref ≈0.05
Frequency Variable ..... To cause Frequency MHz read 0.050
Amplitude Multiplier X1
Output Amplitude
Volts P-P 0.6

2387-605

a. While repeatedly pressing the 7612D ARM A button, adjust the right vertical 7A16A Position and Variable Volts/Div to obtain a clipped sine-wave display as shown in Figure 5-25a. The display should be eight divisions high.

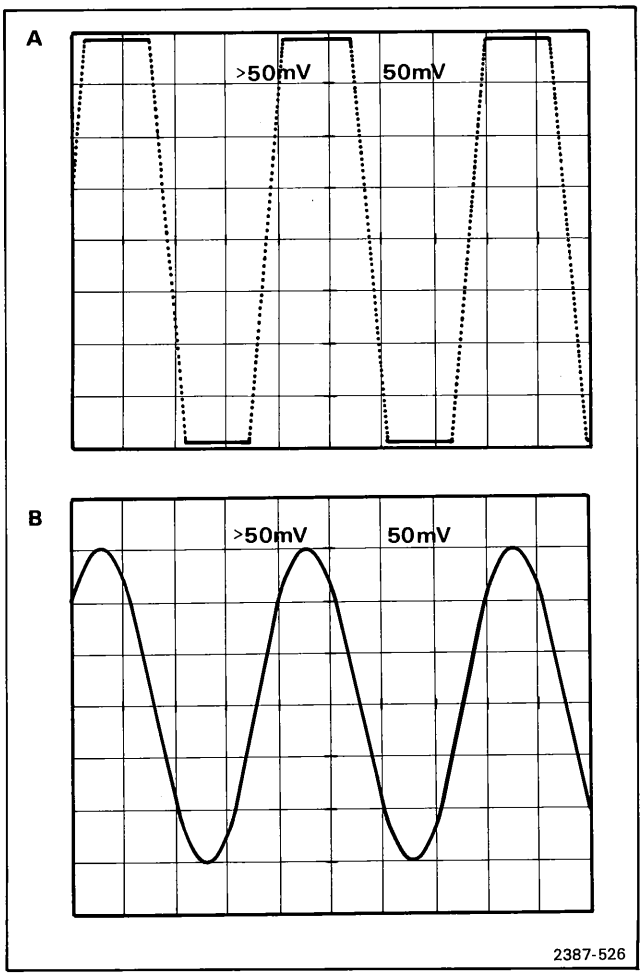


Fig. 5-25. Vertical setup waveforms.

b. Repeatedly press the 7612D ARM A button and adjust the calibration fixture Amplitude and, if necessary, Position control(s) to obtain a centered six-division display as shown in Figure 5-25b.

c. Set the SG 503 to 75 MHz.

d. Set the 7612D SAMPLE INTERVAL to 200E-9.

e. Press the 7612D ARM A button, and adjust the right vertical 7A16A Position control to bring the 7612D's Channel B trace on screen. (The Channel B trace will be below the sine-wave display on Channel A.)

f. **CHECK**—that the amplitude of the Channel B signal is 1.5 minor divisions or less.

g. Turn off the 7612D.

h. Set the SG 503 to 50 kHz.

i. Move the calibration fixture from Channel A to Channel B.

j. Turn the 7612D on, and set it as follows:

INSTRUMENT FUNCTION
PROGRAM . . . . . CHANNEL B
TRIGGER FUNCTIONS
SELECT . . . . . R
SAMPLE INTERVAL 50E-9

k. Set the calibration fixture Amplitude control fully clockwise.

l. While repeatedly pressing the 7612D ARM B button, adjust the right vertical 7A16A Position and Variable Volts/Div controls to obtain a clipped sine-wave display as shown in Figure 5-25a. The display should be eight divisions high.

m. Repeatedly press the 7612D ARM B button and adjust the Calibration Fixture Amplitude and, if necessary, Position control(s) to obtain a centered six-division display as shown in Figure 5-25b.

n. Set the SG 503 to 75 MHz.

o. Set the 7612D SAMPLE INTERVAL to 200E-9.

p. Press the 7612D ARM B button and adjust the right vertical 7A16A Position control to bring the 7612D Channel A trace on screen. (The Channel A trace will be above the sine-wave display on Channel B.)

q. **CHECK**—that the amplitude of the Channel A signal is 1.5 minor divisions or less.

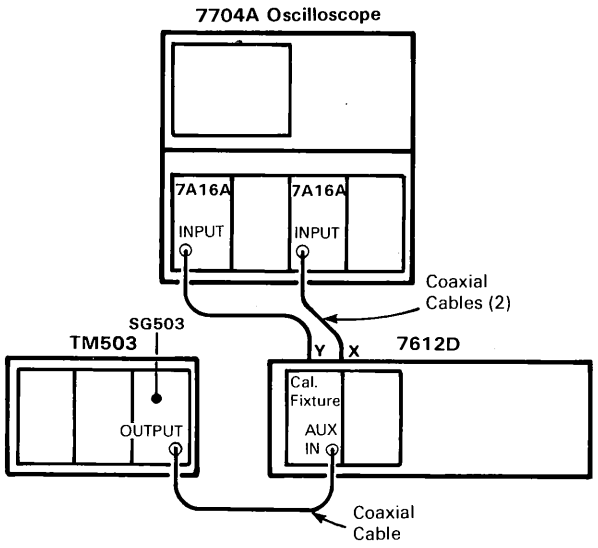
K7. CHECK/ADJUST CHANNEL A BANDWIDTH

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K7. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 2E-6



Test Equipment Controls:

Calibration Fixture
- Test ..... Vert or Horiz Freq Resp
- Position ..... Centered

SG503 Leveled Sine Wave Generator
- Frequency Range (MHz) ..... Ref ≈0.05
- Amplitude Multiplier X.1
- Output Amplitude Volts P-P .....Turn clockwise from zero until CW Leveled indicator on Calibration Fixture lights. Then advance the Output Amplitude Volts P-P 0.1 V

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	Up

2387-606

a. Press the ARM A button.

b. Use the Position control on the left vertical 7A16A to center the display on the test oscilloscope.

c. Use the Variable Volts/Div Control on the left vertical 7A16A to set the display for six divisions of amplitude; then re-center the display with the Position control.

d. Set the SG 503 Frequency to 20.0 MHz, and press the ARM A button. Check that the CW Leveled indicator on the calibration fixture is lit.

e. **CHECK**—for at least 4.2 vertical divisions of signal.

f. Set the SG 503 Frequency to 40.0 MHz, check that the CW Leveled indicator is lit, and press the ARM A button.

g. **CHECK**—for at least 4.2 vertical divisions of signal.

h. Set the SG 503 Frequency to 60.0 MHz, check that the CW Leveled indicator is lit, and press the ARM A button.

i. **CHECK**—for at least 4.2 vertical divisions of signal.

j. Set the SG 503 Frequency to 80.0 MHz, check that the CW Leveled indicator is lit, and press the ARM A button.

k. **CHECK**—for at least 4.2 vertical divisions of signal.

l. Set the SG 503 Frequency to 90.0 MHz, check that the CW Leveled indicator is lit, and press the ARM A button.

m. **CHECK**—for at least 4.2 vertical divisions of signal.

n. **ADJUST**—C717 and R717 (HF Comp) for at least 4.2 and not more than 4.4 major vertical divisions of deflection.

o. Replace the 7612D right side cover.

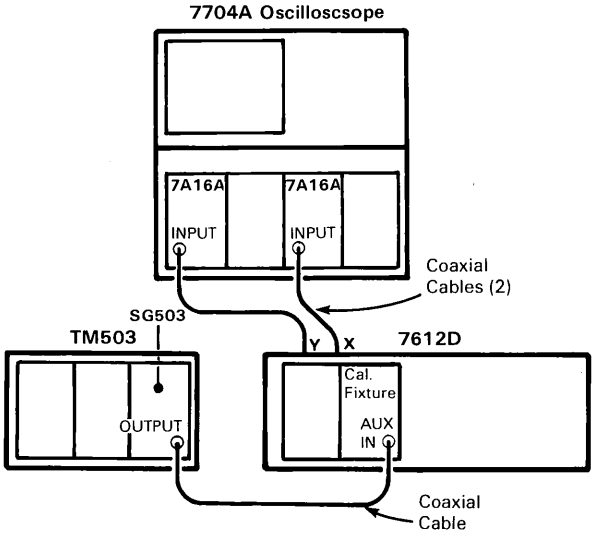
K8. CHECK/ADJUST CHANNEL B BANDWIDTH

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K8. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 2E-6



Test Equipment Controls:

Calibration Fixture
- Test ..... Vert or Horiz Freq Resp
- Position ..... Centered

SG503 Leveled Sine Wave Generator
- Frequency Range (MHz) ..... Ref ≈0.05
- Amplitude Multiplier X.1
- Output Amplitude Volts P-P ..... Turn clockwise from zero until CW Leveled indicator on Calibration Fixture lights. Then advance the Output Amplitude Volts P-P 0.1 V

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	Up

2387-607

a. Press the ARM B button.

b. Use the Position control on the left vertical 7A16A to center the display on the test oscilloscope.

c. Use the Variable Volts/Div Control on the left vertical 7A16A to set the display to be six divisions in amplitude; then re-center the display with the Position control.

d. Set the SG 503 Frequency to 20.0 MHz, press the ARM B button, and check that the CW Leveled indicator on the calibration fixture is lit.

e. **CHECK**—for at least 4.2 vertical divisions of signal.

f. Set the SG 503 Frequency to 40.0 MHz, check that the CW Leveled indicator is lit, and press the ARM B button.

g. **CHECK**—for at least 4.2 vertical divisions of signal.

h. Set the SG 503 Frequency to 60.0 MHz, check that the CW Leveled indicator is lit, and press the ARM B button.

i. **CHECK**—for at least 4.2 vertical divisions of signal.

j. Set the SG 503 Frequency to 80.0 MHz, check that the CW Leveled indicator is lit, and press the ARM B button.

k. **CHECK**—for at least 4.2 vertical divisions of signal.

l. Set the SG 503 Frequency to 90.0 MHz, check that the CW Leveled indicator is lit, and press the ARM B button.

m. **CHECK**—for at least 4.2 vertical divisions of signal.

n. **ADJUST**—HF Comp. (C738, R738) for at least 4.2 and not over 4.4 vertical divisions of deflection.

o. Replace the 7612D right side cover.

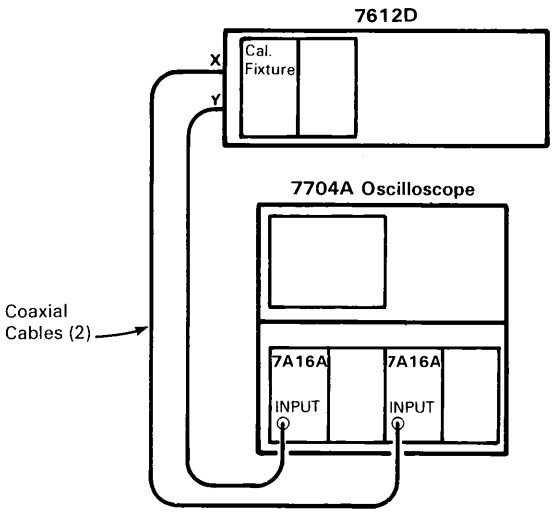
K9. CHECK CHANNEL A ABERRATION

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K9. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 5E-9



Test Equipment Controls:
7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	+Up

Calibration Fixture
Test ..... Vert or Horiz + Step Resp
Rep Rate ..... 1 MHz
Position } ..... To produce six-division
Amplitude } square wave centered on 7704A display. Press ARM A repeatedly while setting Position and Amplitude

2387-608A

a. Change the A Horiz 7A16A Volts/Div to 10 mV and center the waveform front corner to obtain a display similar to that shown in Figure 5-26.

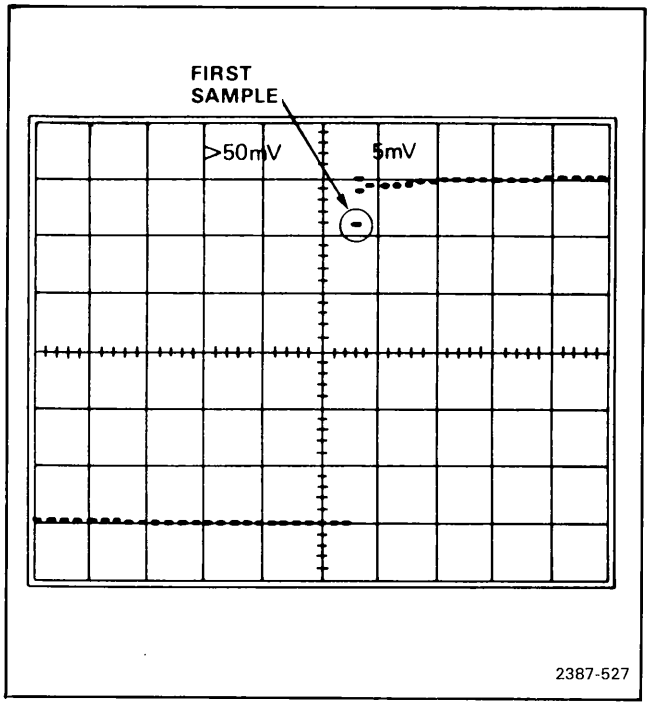


Fig. 5-26. Aberration waveform showing undershoot.

b. Press ARM A repeatedly to display samples of the aberrations on the waveform front corner.

NOTE

Figure 5-26 is an example of a waveform that is just within the −4% undershoot tolerance. The first sample dot is ignored in Figure 5-26.

c. **CHECK**—that the front corner overshoot and undershoot does not exceed +1.2, −1.2 minor vertical graticule divisions (+4, −4%).

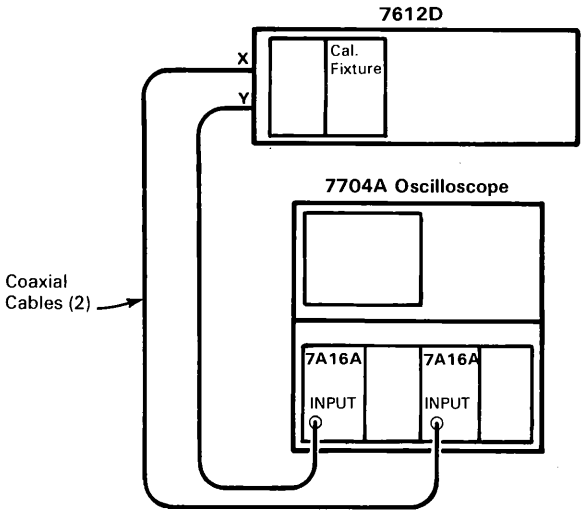
K10. CHECK CHANNEL B ABERRATION

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K10. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings



Test Equipment Controls:
7A16A Amplifiers

	Left Vert	A Horiz
Volts/Div	50 mV	0.2 V
Coupling	DC	DC
Bandwidth	Full	Full
Polarity	+Up	+Up

7704A Oscilloscope
Vertical Mode ..... Left
Horizontal Mode ..... A

Calibration Fixture
Test .....Vert or Horiz + Step Resp
Rep Rate ..... 1 MHz
Position, Amplitude .....To produce six-division square wave centered on 7704A display. Press ARM A repeatedly while setting Position and Amplitude

2387-609

a. Change the A Horiz 7A16A Volts/Div to 10 mV and center the waveform front corner to obtain a display similar to that shown in Figure 5-26.

b. Press the ARM B button repeatedly to display samples of the aberrations on the waveform front corner.

NOTE

Figure 5-26 is an example of a waveform that is just within the −4% undershoot tolerance. The first dot is ignored in Figure 5-26.

c. **CHECK**—that the front corner undershoot does not exceed +1.2 or −1.2 minor graticule divisions (±4%).

NOTE

The bandwidth and aberration characteristics are interdependent. If the aberrations do not meet minimum specifications, repeat the bandwidth adjustments for the best compromise between bandwidth and aberrations.

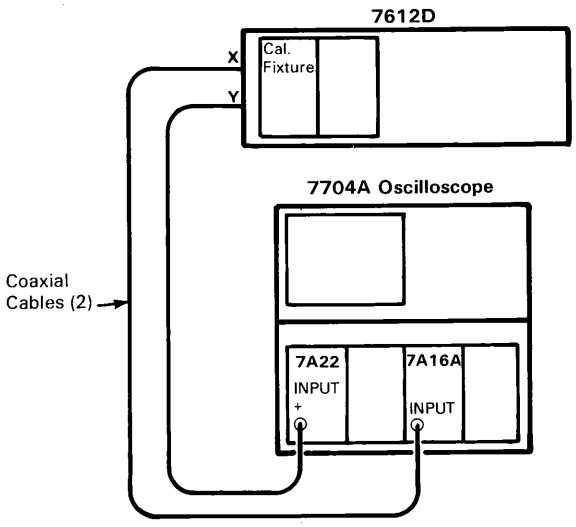
K11. CHECK CHANNEL A LOW-FREQUENCY STEP RESPONSE

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K11. SETUP CONDITIONS

7612D Controls:
SAMPLE INTERVAL 100E-6



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... A

7A22
- Volts/Div ..... 50 mV
- HF −3 dB Point ..... 1 MHz
- LF −3 dB Point ..... DC
- Coupling ..... DC

7A16A Amplifier
- Volts/Div ..... 0.1 V
- Polarity ..... +Up
- Coupling ..... DC
- Bandwidth ..... Full

Calibration Fixture
- Test ..... Vert or Horiz Step Resp
- Rep Rate ..... 10 Hz
- Position } ..... To produce a five-division display centered on the 7704A display. Press ARM A repeatedly while adjusting Position and Amplitude
- Amplitude }

2387-610

a. Set the 7A22 Volts/Div to 5 mV and the LF −3 dB Point to DC Offset.

b. Set the 7A22 Coarse and Fine Offset to view the top of the pulse.

c. **CHECK**—for not over one-half major division (1%) of tilt.

d. Change the calibration fixture Rep Rate to 100 Hz and the 7612D SAMPLING INTERVAL to 10E-6. Press ARM A.

e. **CHECK**—for not over one-half major division of tilt.

f. Change the calibration fixture Rep Rate to 1 kHz and the 7612D SAMPLE INTERVAL to 1E-6. Press ARM A.

g. **CHECK**—for not over one-half major division of tilt.

h. Change the calibration fixture Rep Rate to 10 kHz and the 7612D SAMPLING INTERVAL to 100E-9. Press ARM A.

i. **CHECK**—for not over one-half major division of tilt.

j. Change the calibration fixture Rep Rate to 100 kHz and the 7612D SAMPLING INTERVAL to 10E-9. Press ARM A.

k. **CHECK**—for not over one-half major division of tilt.

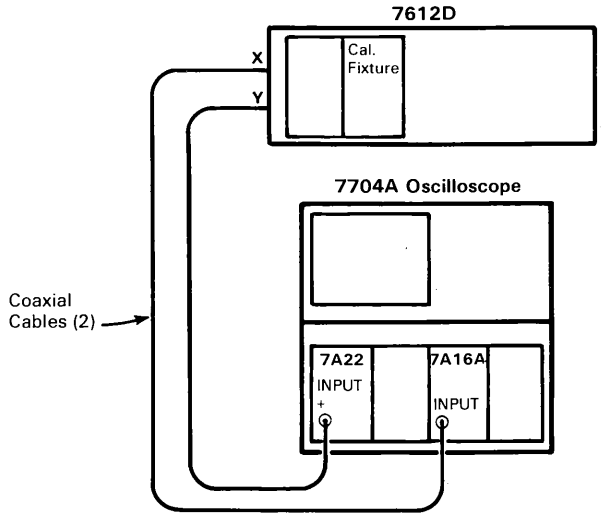
K12. CHECK CHANNEL B LOW-FREQUENCY STEP RESPONSE

NOTE

If the preceding step was not performed, first perform step K1, then proceed.

K12. SETUP CONDITIONS

7612D Controls:
- SAMPLE INTERVAL 100E-6
- TRIGGER FUNCTIONS
  - SELECT ..... R
- INSTRUMENT FUNCTION
  - PROGRAM ..... CHANNEL B



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... A

7A22
- Volts/Div ..... 50 mV
- HF -3 dB Point ..... 1 MHz
- LF -3 dB Point ..... DC
- Coupling ..... DC

7A16A Amplifier
- Volts/Div ..... .1 V
- Polarity ..... +Up
- Coupling ..... DC
- Bandwidth ..... Full

Calibration Fixture
- Test ..... Vert or Horiz Step Resp
- Rep Rate ..... 10 Hz
- Position, Amplitude ..... To produce a five-division display centered on the 7704A display. Press ARM A repeatedly while adjusting Position and Amplitude

2387-611

a. Move the calibration fixture from CHANNEL A to CHANNEL B of the 7612D.

b. Press PROGRAM CHANNEL B and SELECT R buttons.

c. Set the 7A22 Volts/Div to 5 mV and set its LF-3 dB Point to DC Offset.

d. Set the 7A22 Coarse and Fine Offset controls to bring the top of the pulse on the oscilloscope screen.

e. Press the ARM B button.

f. **CHECK**—for not over one-half major division of tilt.

g. Change the calibration fixture Rep Rate to 100 Hz and the 7612D SAMPLING INTERVAL to 10E-6. Press the ARM B button.

h. **CHECK**—for not over one-half major division of tilt.

i. Change the calibration fixture Rep Rate to 1 kHz and the 7612D SAMPLING INTERVAL to 1E-6. Press the ARM B button.

j. **CHECK**—for not over one-half major division of tilt.

k. Change the calibration fixture Rep Rate to 10 kHz and the 7612D SAMPLING INTERVAL to 100E-9. Press the ARM B button.

l. **CHECK**—for not over one-half major division of tilt.

m. Change the calibration fixture Rep Rate to 100 kHz and the 7612D SAMPLING INTERVAL to 10E-9. Press the ARM B button.

n. **CHECK**—for not over one-half major division of tilt.

o. Disconnect the test oscilloscope and remove the calibration fixture.

L. POWER SUPPLY REMOTE CONTROL

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

1. Test Oscilloscope, 7704A
3. Amplifier, 7A16A (two needed)
11. Digital Multimeter, DM 501A
13. Function Generator, FG 501A
15. Power Module Mainframe, TM 503
17. Coaxial Cables (four needed)
20. Adapter, bnc "T" (two needed)
21. Adapter, bnc female to dual banana plug

L1. POWER SUPPLY REMOTE CONTROL PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

L2. CHECK REMOTE ACTUATE INPUT

NOTE

First perform step L1, then proceed.

a. Connect and set the equipment as shown in L2. SETUP CONDITIONS.

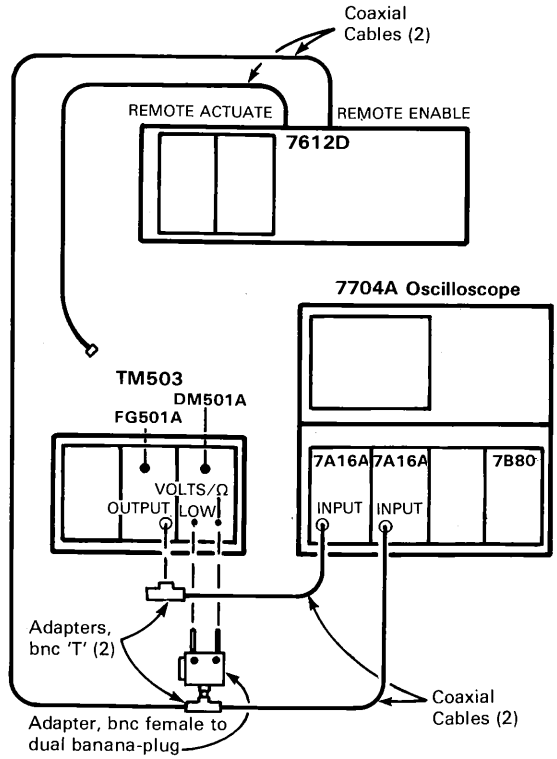
b. Set the FG 501A Frequency Multiplier to 10^{-1}.

c. Set the 7704A Vertical Mode to Chop.

d. Set the input coupling switches on both 7A16As to GND.

L2. SETUP CONDITIONS

7612D Controls:
Make no changes.



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- Trigger Source ..... Left Vert

7A16A Amplifiers

	Left	Right
Volts/Div	1	5
Coupling	DC	DC

7B80 Time Base
- Time/Div ..... 5 ms
- Triggering
  - Mode ..... P-P auto
  - Coupling ..... AC
  - Source ..... Int

FG 501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^2
- Function ..... ⌐ (square wave)
- Amplitude ..... To produce square wave of 1:6 V P-P
- Offset ..... To set negative excursion of square wave to +0.5 V. Results should be square wave between +0.5 V and −2.1 Vdc

DM 501A Digital Multimeter
- KΩ ..... Pressed in
- Input ..... EXT
- Range ..... 2 k ohm]

In this test the DM 501A acts as a current source for a pull-up on the 7612D REMOTE ENABLE input. Any current source of less than 16 mA will work. For example, a 1 kΩ resistor connected to +5 V will provide 5 mA.

2387-612

e. Set both oscilloscope traces to graticule center.

f. Set both 7A16A input coupling switches to DC.

g. Set the time base to Norm triggering and 50 ms/div.

h. Connect the coaxial cable from the 7612D REMOTE ACTUATE connector to the bnc T on the FG 501A Output.

i. **CHECK**—that the 7612D powers on, then off at the FG 502 frequency (about five seconds on, five seconds off).

L3. CHECK REMOTE ENABLE OUTPUT

NOTE

If the preceding step was not performed, first perform step L1, then proceed.

a. Connect and set the equipment as shown in L3. SETUP CONDITIONS.

b. Set the FG 501A Multiplier to 10^{-1}.

c. Set the input coupling switches on both 7A16A's to Gnd.

d. Set both oscilloscope traces to graticule center.

e. Set both 7A16A input coupling switches to DC.

f. Set the time base to Norm trigger mode and 50 mV/Div.

g. Connect the coaxial cable from the FG 501A output to the 7612D REMOTE ACTUATE input.

h. **CHECK**—that the REMOTE ENABLE waveform (on the right 7A16A) switches high between 150 ms and 250 ms after the ACTUATE waveform switches high. Because the time base is triggered by the left vertical (REMOTE ACTUATE) signal, its transition will not be visible. (For best triggering, the time base trigger slope should be set to +, and the trigger level should be just on the + side of zero.) Figure 5-27 shows the test oscilloscope display.

i. **CHECK**—that the low part of the REMOTE ENABLE waveform is within 0.8 V of the ground reference level.

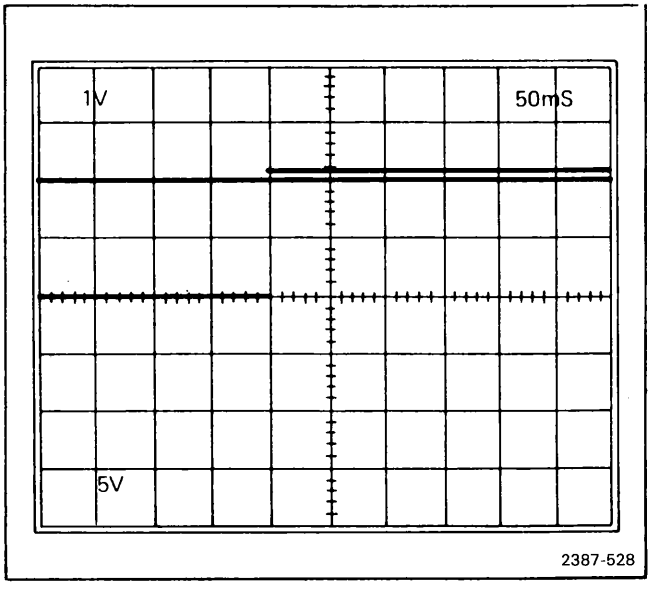
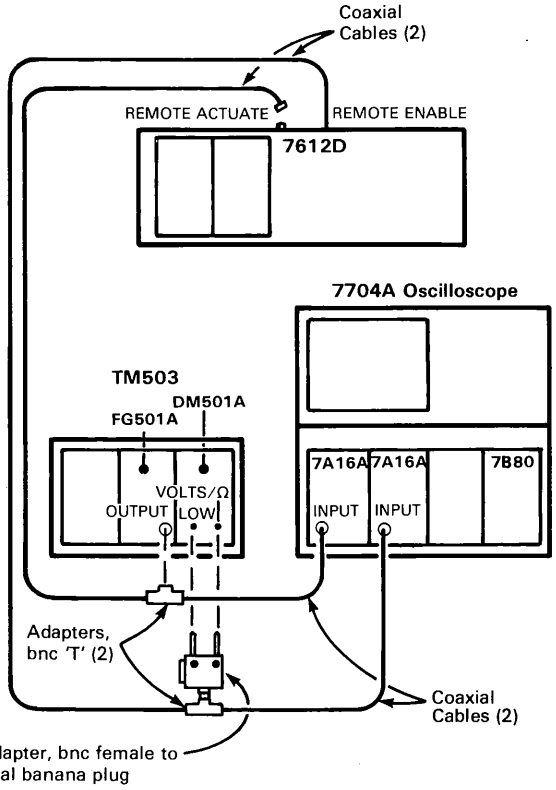


Fig. 5-27. The REMOTE ENABLE output check display.

L3. SETUP CONDITIONS

7612D Controls:
Make no changes to the control settings.



Test Equipment Controls:

7704A Oscilloscope
- Vertical Mode ..... Chop
- Horizontal Mode ..... B
- Trigger Source ..... Left Vert

7A16A Amplifiers

	Left	Right
Volts/Div	1	5
Coupling	DC	DC

7B80 Time Base
- Time/Div ..... 5 mS
- Triggering
  - Mode ..... P-P Auto
  - Coupling ..... AC
  - Source ..... Int

FG501A Function Generator
- Frequency Hz 1
- Multiplier ..... 10^2
- Function ..... ⊓ (square wave)
- Amplitude ..... To produce square wave of 1:6 V P-P
- Offset ..... To set negative excursion of square wave to +0.5 V. Results should be squarewave between +0.5 V and −2.1 Vdc

DM501A Digital Multimeter
- KΩ ..... Pressed in
- Input ..... EXT
- Range ..... 2 kΩ

2387-613

M. EXTERNAL CONNECTORS

Equipment Required: (Numbers match those used in Table 5-3, Test Equipment.)

11. Digital Multimeter, DM 501A
15. Power Module Mainframe, TM 503
17. Cable, Coaxial
24. Shorting Cap

M1. EXTERNAL CONNECTORS PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

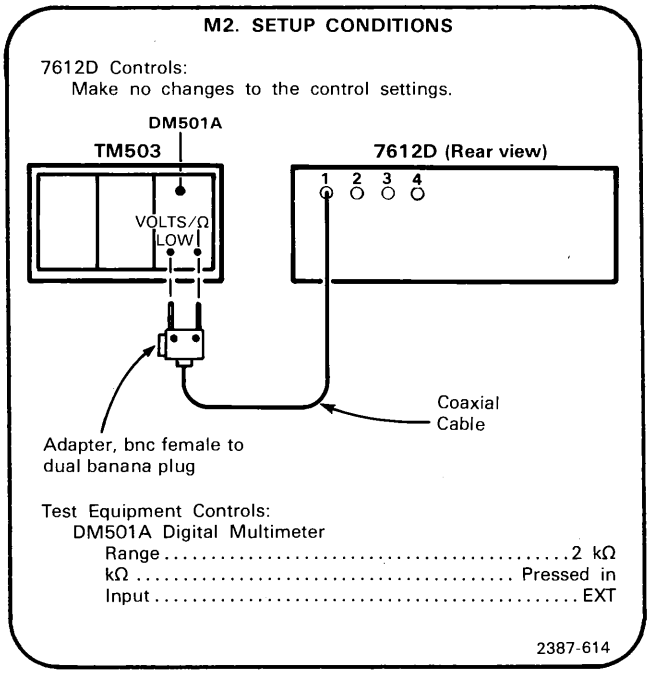
b. Leave the programmable parameters in their power-up conditions, as listed in the Adjustment and Performance Check Initial Setup Procedure.

c. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

M2. CHECK CONTINUITY BETWEEN FRONT- AND REAR-PANEL CONNECTORS

NOTE

First perform step M1, then proceed.



a. Put the shorting cap on bnc connector no. 1 on the 7612D front panel.

b. **CHECK**—that the digital multimeter indicates continuity.

c. Repeat parts a and b for bnc connectors 2, 3, and 4.

INSTRUMENT OPTIONS

Your 7612D may have an optional power cord. This section includes a brief description of each option, and an Option Information Locator Table. The table lists all the options and tells where they are mentioned in this manual. For further information about options see your Tektronix Products catalog or contact your Tektronix Field Office.

OPTION A1

The standard power cord is replaced with the Universal European 240-volt type power cord.

OPTION A2

The standard power cord is replaced with the United Kingdom 240-volt type power cord.

OPTION A3

The standard power cord is replaced with the Australian 240-volt type power cord.

OPTION A4

The standard power cord is replaced with the North American 240-volt type power cord.

OPTION A5

The standard power cord is replaced with the Switzerland 240-volt type power cord.

TABLE 6-1
Option Information Locator

Option	Location in Manual		Information
	Section	Heading	
A1	4 Installation & Maintenance	Power Cord Information (Fig. 4-3)	Lists details of Option A1.
	6 Instrument Options	Option A1	Gives brief description of Option A1.
	9 Replaceable Mechanical Parts	(Near end of Section 9)	Gives part number of power cord.
A2	4 Installation & Maintenance	Power Cord Information (Fig. 4-3)	Lists details of Option A2.
	6 Instrument Options	Option A2	Gives brief description of Option A2.
	9 Replaceable Mechanical Parts	(Near end of Section 9)	Gives part number of power cord.

TABLE 6-1 (CONT)
Option Information Locator

Option	Location in Manual		Information
	Section	Heading	
A3	4 Installation & Maintenance	Power Cord Information (Fig. 4-3)	Lists details of Option A3.
	6 Instrument Options	Option A3	Gives brief description of Option A3.
	9 Replaceable Mechanical Parts	(Near end of Section 9)	Gives part number of power cord.
A4	4 Installation & Maintenance	Power Cord Information (Fig. 4-3)	Lists details of Option A4.
	6 Instrument Options	Option A4	Gives brief description of Option A4.
	9 Replaceable Mechanical Parts	(Near end of Section 9)	Gives part number of power cord.
A5	4 Installation & Maintenance	Power Cord Information (Fig. 4-3)	Lists details of Option A5.
	6 Instrument Options	Option A5	Gives brief descripiton of Option A5.
	9 Replaceable Mechanical Parts	(Near end of Section 9)	Gives part number of power cord.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

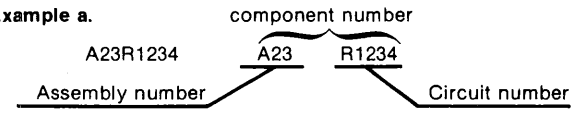
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

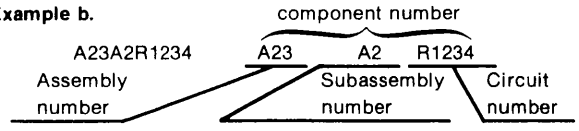
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000FJ	MARCOM SWITCHES INC.	67 ALBANY STREET	CAZENOVIA, N.Y. 13035
000HX	SAN-O INDUSTRIAL CORP.	170 WILBUR PLACE	BAHEMIA, LONG ISLAND, NY. 11
000LI	TOPTRON CORP		TOKYO, JAPAN
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01281	TRW ELECTRONIC COMPONENTS, SEMICONDUCTOR OPERATIONS	14520 AVIATION BLVD.	LAWNDALE, CA 90260
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
03888	KDI PYROFILM CORPORATION	60 S JEFFERSON ROAD	WHIPPANY, NJ 07981
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09023	CORNELL-DUBILIER ELECTRONIC DIVISION FEDERAL PACIFIC ELECTRIC CO.	2652 DALRYMPLE ST.	SANFORD, NC 27330
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
12954	SIEMENS CORPORATION, COMPONENTS GROUP	8700 E THOMAS RD, P O BOX 1390	SCOTTSDALE, AZ 85252
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14298	AMERICAN COMPONENTS, INC., AN INSILCO COMPANY	8TH AVE. AT HARRY STREET	CONSHOHOCKEN, PA 19428
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 E FAIRVIEW ST.	SANTA ANA, CA 92704
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
15238	ITT SEMICONDUCTORS, A DIVISION OF INTER NATIONAL TELEPHONE AND TELEGRAPH CORP.	P.O. BOX 168, 500 BROADWAY	LAWRENCE, MA 01841
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
19396	ILLINOIS TOOL WORKS, INC. PAKTRON DIV.	900 FOLLIN LANE, SE	VIENNA, VA 22180
19647	CADDOCK ELECTRONICS INC.	3127 CHICAGO AVENUE	RIVERSIDE, CA 92507
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO, CA 92121
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
23880	STANFORD APPLIED ENGINEERING, INC.	340 MARTIN AVE.	SANTA CLARA, CA 95050
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
25403	AMPEREX ELECTRONIC CORP., SEMICONDUCTOR AND MICROCIRCUITS DIV.	PROVIDENCE PIKE	SLATERSVILLE, RI 02876
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
27193	CUTLER-HAMMER, INC. SPECIALTY PRODUCTS DIVISION	4201 N. 27TH ST.	MILWAUKEE, WI 53216
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
27802	VECTRON LABORATORIES INC.	121 WATER STREET	NORWALK, CT 06854
32293	INTERSIL, INC.	10900 N. TANTAU AVE.	CUPERTINO, CA 95014
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
53184	XCITON CORPORATION	5 HEMLOCK STREET	LATHAM, NY 12110
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
58361	GENERAL INSTRUMENT CORP. OPTO ELECTRONICS DIV.	3400 HILLVIEW AVE	PALO ALTO, CA 94304
CODE 58	854 NOT FOUND		
58361	GENERAL INSTRUMENT CORP. OPTO ELECTRONICS DIV.	3400 HILLVIEW AVE	PALO ALTO, CA 94304
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
59821	CENTRALAB INC SUB NORTH AMERICAN PHILIPS CORP	7158 MERCHANT AVE	EL PASO, TX 79915
60705	CERA-MITE CORP.	1327 6TH AVE.	GRAFTON, WI 53024

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71590	CENTRALAB ELECTRONICS, DIV. OF GLOBE-UNION, INC.	P O BOX 858	FORT DODGE, IA 50501
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
73899	JFD ELECTRONICS COMPONENTS CORP.	PINETREE ROAD	OXFORD, NC 27565
74276	SIGNALITE DIV., GENERAL INSTRUMENT CORP.	1933 HECK AVE.	NEPTUNE, NJ 07753
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
78488	STACKPOLE CARBON CO.		ST. MARYS, PA 15857
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
81073	GRAYHILL, INC.	561 HILLGROVE AVE., PO BOX 373	LA GRANGE, IL 60525
82877	ROTRON, INC.	7-9 HASBROUCK LANE	WOODSTOCK, NY 12498
83003	VARO, INC.	P O BOX 411, 2203 WALNUT STREET	GARLAND, TX 75040
84411	TRW ELECTRONIC COMPONENTS, TRW CAPACITORS	112 W. FIRST ST.	OGALLALA, NE 69153
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
93410	ESSEX INTERNATIONAL, INC., CONTROLS DIV. LEXINGTON PLANT	P. O. BOX 1007	MANSFIELD, OH 44903
95238	CONTINENTAL CONNECTOR CORP.	34-63 56TH ST.	WOODSIDE, NY 11377

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-4947-00			CKT BOARD ASSY:FRONT PANEL	80009	670-4947-00
A12	670-4961-00	B010100	B030450	CKT BOARD ASSY:CLOCK BUFFER	80009	670-4961-00
A12	670-4961-01	B030451		CKT BOARD ASSY:CLOCK BUFFER	80009	670-4961-01
A14	672-0854-00			CKT BOARD ASSY:HEADER	80009	672-0854-00
A16	670-4952-00	B010100	B029999	CKT BOARD ASSY:TRANSLATOR	80009	670-4952-00
A16	670-4952-01	B030000		CKT BOARD ASSY:TRANSLATOR	80009	670-4952-01
A18	670-5940-00			CKT BOARD ASSY:DATA STORAGE	80009	670-5940-00
A20	670-4950-01	B010100	B030254	CKT BOARD ASSY:TIME BASE	80009	670-4950-01
A20	670-4950-02	B030255	B030707	CKT BOARD ASSY:TIME BASE	80009	670-4950-02
A20	670-4950-04	B030708		CKT BOARD ASSY:TIME BASE	80009	670-5940-04
A26	670-4941-00	B010100	B019999	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-00
A26	670-4941-01	B020000	B029999	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-01
A26	670-4941-02	B030000	B030335	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-02
A26	670-4941-03	B030336	B030405	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-03
A26	670-4941-04	B030406		CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-04
A44	----- -----			CKT BOARD ASSY:(NOT REPL,ORDER 672-0648-00)		
A46	----- -----			CKT BOARD ASSY:(NOT REPL,ORDER 672-0648-00)		
A52	670-5772-00	B010100	B019999	CKT BOARD ASSY:MPU MEMORY	80009	670-5772-00
A52	670-5772-01	B020000		CKT BOARD ASSY:MPU MEMORY	80009	670-5772-01
A54	670-5771-00	B010100	B030221	CKT BOARD ASSY:MPU	80009	670-5771-00
A54	670-5771-01	B030222	B030389	CKT BOARD ASSY:MPU	80009	670-5771-01
A54	670-5771-02	B030390		CKT BOARD ASSY:MPU	80009	670-5771-02
A56	670-5773-00	B010100	B029999	CKT BOARD ASSY:IEEE 488 INTERFACE	80009	670-5773-00
A56	670-5773-02	B030000		CKT BOARD ASSY:IEEE 488 INTERFACE	80009	670-5773-02
A60	670-6416-00			CKT BOARD ASSY:SHIELD	80009	670-6416-00
A62	670-4958-00	B010100	B030221	CKT BOARD ASSY:TRIGGER	80009	670-4958-00
A62	670-4958-01	B030222	B030368	CKT BOARD ASSY:TRIGGER	80009	670-4958-01
A62	670-4958-02	B030369		CKT BOARD ASSY:TRIGGER	80009	670-4958-02
A68	670-4940-00	B010100	B030658	CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-4940-00
A68	670-4940-01	B030659		CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-4940-01
A70	119-1189-00			CKT BOARD ASSY:HV RESISTOR	80009	119-1189-00
A72	119-0907-00			POWER SUPPLY:BEAM CONTROL	80009	119-0907-00
A74	119-0906-00	B010100	B029999	POWER SUPPLY:HIGH VOLTAGE MULTIPLIER	80009	119-0906-00
A74	119-0906-01	B030000		POWER SUPPLY:HIGH VOLTAGE MULTIPLIER	80009	119-0906-01
A76	670-4949-00	B010100	B029999	CKT BOARD ASSY:HIGH VOLTAGE OSCILLATOR	80009	670-4949-00
A76	670-4949-01	B030000	B030405	CKT BOARD ASSY:HIGH VOLTAGE OSCILLATOR	80009	670-4949-01
A76	670-4949-02	B030406		CKT BOARD ASSY:HIGH VOLTAGE OSCILLATOR	80009	670-4949-02
A80	670-5442-00	B010100	B030174	CKT BOARD ASSY:LINE POWER	80009	670-5442-00
A80	670-5442-01	B030175		CKT BOARD ASSY:LINE POWER	80009	670-5442-01
A82	670-4956-00	B010100	B030174	CKT BOARD ASSY:MAIN	80009	670-4956-00
A82	670-4956-03	B030175	B030729	CKT BOARD ASSY:MAIN	80009	670-4956-03
A82	670-4956-04	B030730		CKT BOARD ASSY:CONTROL	80009	670-4956-04
A86	670-4955-00	B010100	B030254	CKT BOARD ASSY:RECTIFIER FILTER	80009	670-4955-00
A86	670-4955-01	B030255	B030729	CKT BOARD ASSY:RECTIFIER FILTER	80009	670-4955-01
A86	670-4955-02	B030730		CKT BOARD ASSY:RECTIFIER FILTER	80009	670-4955-02
A88	670-4954-00	B010100	B030174	CKT BOARD ASSY:REGULATOR	80009	670-4954-00
A88	670-4954-02	B030175		CKT BOARD ASSY:REGULATOR	80009	670-4954-02
A10	670-4947-00			CKT BOARD ASSY:FRONT PANEL	80009	670-4947-00
A10C124	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C134	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C144	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C212	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10C214	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C216	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C226	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C246	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C256	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C318	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C338	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C346	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C348	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C414	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C416	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C436	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C442	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	56289	502D231
A10C544	283-0187-00			CAP.,FXD,CER DI:0.047UF,10%,400V	72982	8131N401X5R0473K
A10C546	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	56289	502D231
A10C614	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C632	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C636	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C714	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C716	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C828	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C832	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C838	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C842	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C852	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10C858	283-0083-00			CAP.,FXD,CER DI:0.0047UF,20%,500V	72982	811-565C471J
A10C954	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A10DS006	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS008	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS102	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS106	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS110	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS204	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS214	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS220	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS230	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS240	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS250	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS306	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS308	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS314	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS324	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS344	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS354	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS402	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS406	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS410	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS432	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	53184	XC209G
A10DS456	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS506	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS508	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS518	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS524	150-1069-00			LAMP,LED,RDOUT:RED,660NM,2V,510 UCD	50522	MAN73A
A10DS526	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10DS536	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS556	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS602	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS606	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS616	150-1043-00			LT EMITTING DIO:RED,20MA,5V	58361	MV5774C
A10DS618	150-1043-00			LT EMITTING DIO:RED,20MA,5V	58361	MV5774C
A10DS620	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS656	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS702	150-1069-00			LAMP,LED,RDOUT:RED,660NM,2V,510 UCD	50522	MAN73A
A10DS704	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS734	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	53184	XC209G
A10DS804	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS808	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS814	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS822	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS832	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS852	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS902	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS906	150-1022-00			LAMP,LED,RDOUT:7 SEG NUMERIC,LH DEC ORANGE	50522	MAN72A
A10DS916	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS926	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS936	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS946	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10DS956	150-0048-01			LAMP,INCAND:5V,0.06A,SEL	58854	683AS15
A10J548	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A10J550	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A10J552	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A10J554	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A10J556	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A10Q716	151-0366-00			TRANSISTOR:SILICON,PNP	03508	X45C277
A10Q718	151-0366-00			TRANSISTOR:SILICON,PNP	03508	X45C277
A10Q914	151-0366-00			TRANSISTOR:SILICON,PNP	03508	X45C277
A10Q916	151-0366-00			TRANSISTOR:SILICON,PNP	03508	X45C277
A10Q918	151-0366-00			TRANSISTOR:SILICON,PNP	03508	X45C277
A10Q926	151-0366-00			TRANSISTOR:SILICON,PNP	03508	X45C277
A10R010	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R012	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R014	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R016	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R018	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R019	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R020	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R110	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R214	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R220	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R230	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R240	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R250	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R300	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R302	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R303	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R304	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R305	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R306	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10R308	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R314	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R324	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R344	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R354	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R410	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R432	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A10R436	307-0502-00			RES NTWK,FXD,FI:(9) 1.8K OHM,20%,0.125W	91637	MSP10A01-182M
A10R510	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R511	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R512	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R514	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R516	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R518	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R520	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R528	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R536	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R554	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R556	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R636	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A10R656	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R700	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R702	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R703	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R704	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R706	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R708	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R710	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R712	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A10R714	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A10R814	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R820	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A10R821	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A10R822	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R823	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A10R824	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A10R826	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A10R828	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A10R832	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R852	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R856	315-0824-00			RES.,FXD,CMPSN:820K OHM,5%,0.25W	01121	CB8245
A10R858	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A10R916	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R926	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R936	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10R946	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A10S110	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S214	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S220	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S230	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S240	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S250	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S314	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S324	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10S334	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S344	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S354	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S410	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S416	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S446	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S456	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S518	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S536	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S544	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S556	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S640	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S646	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S656	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S814	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S822	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S832	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S842	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S852	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S916	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S926	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S936	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S946	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10S956	263-0019-06			SWITCH,PB ASSY:MOMENTARY	80009	263-0019-06
A10TP942	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A10TP944	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A10TP946	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A10TP948	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A10U114	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U124	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U144	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U154	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A10U210	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U226	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U236	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U246	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U256	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U328	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U338	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U358	156-0531-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR,SCRN	80009	156-0531-02
A10U424	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U426	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U436	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A10U452	156-0531-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR,SCRN	80009	156-0531-02
A10U624	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U632	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U638	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A10U724	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U726	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U736	156-0141-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR/DEMX	80009	156-0141-02
A10U746	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A10U756	156-0030-03			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE,SCRN	01295	SN7400(NP3 OR JP
A10U838	156-0888-02			MICROCIRCUIT,DI:HEX DIGIT DRIVER,SCREENED	80009	156-0888-02
A10U848	156-0544-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH	07263	93L34
A10U858	156-0402-02			MICROCIRCUIT,LI:TIMER,CHK	27014	LM555CN/A+
A10W544	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A12	670-4961-00	B010100	B030450	CKT BOARD ASSY:CLOCK BUFFER	80009	670-4961-00
A12	670-4961-01	B030451		CKT BOARD ASSY:CLOCK BUFFER	80009	670-4961-01
A12C110	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C112	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C124	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C300	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C312	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C314	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C320	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C322	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C400	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A12C402	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A12C404	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A12C406	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C410	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C422	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A12C510	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C516	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A12C526	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12CR220	152-0153-00	B010100	B030450	SEMICOND DEVICE:SILICON,15V,50MA	07263	FD7003
A12CR222	152-0153-00	B010100	B030450	SEMICOND DEVICE:SILICON,15V,50MA	07263	FD7003
A12CR300	152-0153-00			SEMICOND DEVICE:SILICON,15V,50MA	07263	FD7003
A12CR302	152-0153-00			SEMICOND DEVICE:SILICON,15V,50MA	07263	FD7003
A12CR310	152-0153-00			SEMICOND DEVICE:SILICON,15V,50MA	07263	FD7003
A12CR312	152-0153-00			SEMICOND DEVICE:SILICON,15V,50MA	07263	FD7003
A12J328	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J328	----- -----			(QTY 4)		
A12J406	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J406	----- -----			(QTY 8)		
A12J418	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J418	----- -----			(QTY 4)		
A12J428	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J428	----- -----			(QTY 4)		
A12J500	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J500	----- -----			(QTY 9)		
A12J510	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J510	----- -----			(QTY 3)		
A12J524	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A12J524	----- -----			(QTY 4)		
A12J300	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A12J310	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A12Q114	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A12Q122	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A12Q214	151-0434-00			TRANSISTOR:SILICON,PNP	04713	SS7144
A12Q222	151-0434-00			TRANSISTOR:SILICON,PNP	04713	SS7144
A12Q424	151-0434-00			TRANSISTOR:SILICON,PNP	04713	SS7144
A12L114	108-0170-01			COIL,RF:FIXED,36ONH	80009	108-0170-01
A12L120	108-0170-01			COIL,RF:FIXED,36ONH	80009	108-0170-01
A12L210	108-0170-01			COIL,RF:FIXED,36ONH	80009	108-0170-01
A12L224	108-0170-01			COIL,RF:FIXED,36ONH	80009	108-0170-01
A12Q516	151-0434-00			TRANSISTOR:SILICON,PNP	04713	SS7144
A12Q518	151-0434-00			TRANSISTOR:SILICON,PNP	04713	SS7144
A12Q524	151-0434-00			TRANSISTOR:SILICON,PNP	04713	SS7144
A12R112	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A12R114	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F
A12R120	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F
A12R122	317-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.125W	01121	BB3005
A12R124	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F
A12R210	323-0071-00			RES.,FXD,FILM:53.6 OHM,1%,0.50W	75042	CECT0-53R60F
A12R212	317-0200-00	B010100	B030450	RES.,FXD,CMPSN:20 OHM,5%,0.125W	01121	BB2005
A12R214	321-0126-00			RES.,FXD,FILM:200 OHM,1%,0.125W	91637	MFF1816G200R0F
A12R220	317-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.125W	01121	BB4715
A12R222	317-0200-00	B010100	B030450	RES.,FXD,CMPSN:20 OHM,5%,0.125W	01121	BB2005
A12R224	323-0071-00			RES.,FXD,FILM:53.6 OHM,1%,0.50W	75042	CECT0-53R60F
A12R228	311-0643-00			RES.,VAR,NONWIR:50 OHM,10%,0.50W	73138	82-33-2
A12R312	321-0771-01			RES.,FXD,FILM:50 OHM,0.5%,0.125W	91637	MFF1816G50R00D
A12R320	307-0677-00			RES NTWK,FXD FI:4,56 OHM,2%,0.2W	75042	BWH-1R000J
A12R322	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A12R324	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A12R410	307-0677-00			RES NTWK,FXD FI:4,56 OHM,2%,0.2W	75042	BWH-1R000J
A12R416	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R418	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R422	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R424	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R426	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F
A12R427	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R428	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R429	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A12R510	311-0634-00			RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	32997	3329H-G48-501
A12R512	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A12R516	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F
A12R517	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R518	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A12R519	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A12R524	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A12R528	311-0634-00			RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	32997	3329H-G48-501
A12T220	120-0487-00	B030451		XFMR,TOROID:5 TURNS BIFILAR	80009	120-0487-00
A12TP310	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12U320	156-1032-02			MICROCIRCUIT,DI:QUINT 2 OR/NOR,CHK	80009	156-1032-02
A12U410	156-1032-02			MICROCIRCUIT,DI:QUINT 2 OR/NOR,CHK	80009	156-1032-02
A12W226	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A12Y200	119-0957-00			CRYSTAL OSC:200MHZ	27802	CO-233MEHA

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A14	672-0854-00			CKT BOARD ASSY:HEADER	80009	672-0854-00
A14C006	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C007	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C008	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C009	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C014	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C015	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C016	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C017	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C100	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C101	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C102	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C103	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C112	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C113	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14C114	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C115	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A14C116	283-0191-00			CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N075Z5U0223M
A14J007	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J007	----- -----			(QTY 4)		
A14J008	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J008	----- -----			(QTY 7)		
A14J009	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J009	----- -----			(QTY 3)		
A14J015	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J015	----- -----			(QTY 7)		
A14J016	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J016	----- -----			(QTY 5)		
A14J101	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J101	----- -----			(QTY 7)		
A14J102	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J102	----- -----			(QTY 6)		
A14J113	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J113	----- -----			(QTY 3)		
A14J114	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A14J114	----- -----			(QTY 7)		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A16	670-4952-00	B010100	B029999	CKT BOARD ASSY:TRANSLATOR	80009	670-4952-00
A16	670-4952-01	B030000		CKT BOARD ASSY:TRANSLATOR	80009	670-4952-01
A16C020	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C100	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C110	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C111	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C120	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C121	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C122	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C130	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C200	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C220	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A16C230	283-0622-00			CAP.,FXD,MICA D:450PF,1%,300V	00853	D155F451F0
A16C231	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C300	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C310	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C320	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A16C330	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C400	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A16C410	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C420	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C421	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C430	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C431	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C510	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C610	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C620	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C630	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C700	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C720	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C730	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C810	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C830	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C910	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C920	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C930	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C1000	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1001	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1010	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1011	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1020	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1021	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1030	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16C1031	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A16F231	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A16F232	159-0094-00			FUSE,WIRE LEAD:32V,0.75A.FAST BLOW	75915	273-750
A16F331	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A16L230	108-0735-00			COIL,RF:FIXED,560NH	80009	108-0735-00
A16L320	108-0858-00			COIL,RF:FIXED,3.2NH	80009	108-0858-00
A16R120	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A16R130	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A16R330	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A16R400	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A16R420	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A16R430	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A16R930	315-0102-00	B030000		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A16R1000	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A16TP100	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A16TP600	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A16TP1000	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A16U010	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U020	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U100	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U110	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U120	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U130	156-0266-01			MICROCIRCUIT,DI:EMITTER COUPLED OSCILLATOR	04713	MC16648PD/LD
A16U200	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U210	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A16U230	156-0316-04			MICROCIRCUIT,DI:QUAD ECL TO TTL TRANS	04713	MC10125PD/LD
A16U300	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U310	156-0679-01			MICROCIRCUIT,DI:4 BIT BINARY ADDER,BURN-IN	04713	SN74LS283NDS
A16U320	156-0316-04			MICROCIRCUIT,DI:QUAD ECL TO TTL TRANS	04713	MC10125PD/LD
A16U330	156-0687-01			MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PD
A16U400	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A16U410	156-0679-01			MICROCIRCUIT,DI:4 BIT BINARY ADDER,BURN-IN	04713	SN74LS283NDS
A16U420	156-0316-04			MICROCIRCUIT,DI:QUAD ECL TO TTL TRANS	04713	MC10125PD/LD
A16U430	156-0687-01			MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PD
A16U500	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A16U510	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A16U520	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A16U600	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A16U610	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A16U620	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A16U700	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A16U710	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A16U720	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A16U730	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A16U800	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A16U810	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A16U820	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A16U830	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A16U900	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A16U910	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A16U920	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A16U930	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A16U935	156-0388-03	B030000		MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A16U1000	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A16U1010	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A16U1020	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A16U1030	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18	670-5940-00			CKT BOARD ASSY:DATA STORAGE	80009	670-5940-00
A18C016	290-0773-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A18C024	290-0773-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A18C136	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C302	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C312	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C314	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C332	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C426	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C428	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C522	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C526	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C528	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C624	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C722	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C724	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C728	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C824	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C826	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C924	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18C938	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A18CR124	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR138	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18J002	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A18J844	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A18J944	131-1426-00			CONTACT SET,ELE:R ANGLE,0.250 L,STRIP OF 36	22526	65524-136
A18J946	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A18F026	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A18F036	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A18R102	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A18R104	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A18R106	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A18R108	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A18R136	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18R138	307-0640-00			RES NTWK,FXD FI:9,50 OHM,5%,0.125W	32997	4308R101-151J
A18R206	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18R208	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R228	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R302	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18R312	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R322	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R338	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18R424	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R526	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R632	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A18R720	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R824	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R910	307-0545-00			RES NTWK,FXD,FI:9,75 OHM,5%,0.15W	32997	4310R-101-750
A18R916	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	106A101
A18R932	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18R934	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18R936	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A18TP102	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP104	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18TP106	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP108	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP202	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP808	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18U202	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U212	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U222	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U224	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U232	156-1033-03			MICROCIRCUIT,DI:QUINT DIFF LINE RCVR,CHK	80009	156-1033-03
A18U302	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U312	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U322	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U324	156-1030-02			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A18U332	156-1034-02			MICROCIRCUIT,DI:TRIPLE 5 OR/NOR,CHECKED	80009	156-1034-02
A18U416	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U436	156-0630-01			MICROCIRCUIT,DI:HEX INVERTER/BUFFER,SCRN	04713	MC10195PD/LD
A18U512	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U518	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U532	156-0630-01			MICROCIRCUIT,DI:HEX INVERTER/BUFFER,SCRN	04713	MC10195PD/LD
A18U538	156-0458-01			MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A18U614	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U712	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U718	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U816	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01
A18U836	156-1033-03			MICROCIRCUIT,DI:QUINT DIFF LINE RCVR,CHK	80009	156-1033-03
A18U914	156-1297-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM,BURN-IN	80009	156-1297-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20	670-4950-01	B010100	B030254	CKT BOARD ASSY:TIME BASE	80009	670-4950-01
A20	670-4950-02	B030255	B030707	CKT BOARD ASSY:TIME BASE	80009	670-4950-02
A20	670-4950-04	B030708		CKT BOARD ASSY:TIME BASE	80009	670-4950-04
A20C004	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C012	290-0773-00	B010100	B030707	CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A20C014	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C016	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C018	281-0814-00	B010100	B030707	CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A20C032	290-0773-00	B010100	B030707	CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A20C034	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C036	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C107	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C109	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C111	290-0773-00	B030708		CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A20C114	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C116	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C117	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C119	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C120	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C121	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C122	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C123	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C131	290-0773-00	B030708		CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A20C133	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C134	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C136	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C141	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C200	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C201	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C202	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C203	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C207	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C209	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C214	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C216	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C220	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C221	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C222	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C223	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C234	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C236	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C237	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C239	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C241	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C247	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C302	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C306	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C307	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C309	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C314	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C316	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C321	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C323	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C330	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20C332	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C407	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C409	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C410	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C412	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C417	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C419	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C432	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C436	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C440	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C447	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C449	281-0814-00	B030708		CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A20C500	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C502	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C507	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C509	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C511	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C513	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C514	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C516	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C534	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C536	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C540	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C546	281-0814-00	B010100	B030707	CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A20C547	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C549	281-0814-00	B030708		CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A20C604	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C606	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C607	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C609	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C617	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C619	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C620	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C622	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C634	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C636	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C649	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C700	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C707	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C709	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C710	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C720	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C721	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C723	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C727	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C729	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C740	281-0773-00	B010100	B030707	CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C747	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C841	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20C843	281-0773-00	B030708		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A20CR642	152-0141-02	B010100	B030707	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR702	152-0141-02	B010100	B030707	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR707	152-0141-02	B030708		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR811	152-0141-02	B030708		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20F042	159-0059-00	B010100	B030707	FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A20F046	159-0059-00	B010100	B030707	FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A20F141	159-0059-00	B030708		FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A20F143	159-0059-00	B030708		FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A20J658	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A20J754	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A20L851	120-0487-00	B030708		XFMR,TOROID:5 TURNS BIFILAR	80009	120-0487-00
A20R006	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R026	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R100	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R101	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R106	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R110	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R111	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R126	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R127	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R130	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R137	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R147	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R206	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R210	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R217	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R226	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R227	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R230	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R231	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R240	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R300	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R301	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R306	315-0680-00	B010100	B030707	RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A20R310	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R317	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R326	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R327	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R331	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R336	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R337	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R340	307-0489-00	B010100	B030707	RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A20R346	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R400	307-0489-00	B010100	B030707	RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A20R406	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R411	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R416	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R420	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R421	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R426	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R427	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R428	315-0680-00	B010100	B030707	RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A20R430	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R431	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R441	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R501	307-0489-00	B030708		RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A20R506	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R510	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20R517	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R520	307-0489-00	B010100	B030707	RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A20R521	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R526	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R530	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R537	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R546	315-0152-00	B010100	B030707	RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A20R547	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R600	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R601	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R610	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R611	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R616	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R626	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R627	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R636	315-0680-00	B010100	B030707	RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A20R630	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R637	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R640	315-0511-00	B010100	B030707	RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A20R642	315-0471-00	B010100	B030707	RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A20R646	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R647	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R648	315-0511-00	B030708		RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A20R649	315-0152-00	B030708		RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A20R701	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R707	315-0471-00	B030708		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A20R711	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R717	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R720	315-0510-00	B010100	B030707	RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R730	307-0587-00	B010100	B030707	RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R737	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R740	315-0161-00	B010100	B030707	RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
A20R747	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R821	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20R831	307-0587-00	B030708		RES NTWK,FXD,FI:7,68 OHM,20%,1.0W	91637	MSP08A01-680
A20TP002	214-0579-00	B010100	B030707	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP107	214-0579-00	B030708		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP301	214-0579-00	B030708		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP311	214-0579-00	B030708		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP320	214-0579-00	B010100	B030707	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP546	214-0579-00	B010100	B030707	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP547	214-0579-00	B030708		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP706	214-0579-00	B010100	B030707	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP801	214-0579-00	B030708		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20U006	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U026	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U036	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U100	156-0205-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U101	156-0687-01	B030708		MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PD
A20U106	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U107	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U110	156-0230-02	B010100	B030707	MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U111	156-0687-01	B030708		MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PD
A20U116	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20U117	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U120	156-0230-02	B010100	B030707	MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U121	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U126	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U127	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U130	156-0230-02	B010100	B030707	MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U131	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U136	156-0205-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U137	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U140	156-1031-03	B010100	B030707	MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U141	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U146	156-1032-02	B010100	B030707	MICROCIRCUIT,DI:QUINT 2 OR/NOR,CHK	80009	156-1032-02
A20U147	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U200	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U201	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U206	156-0687-01	B010100	B030707	MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PD
A20U207	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U210	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U211	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U216	156-0687-01	B010100	B030707	MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PD
A20U217	156-0230-02	B030708		MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U220	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U221	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U226	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U227	156-0205-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U230	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U231	156-0205-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U236	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U237	156-0205-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U241	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U246	156-1034-02	B010100	B030707	MICROCIRCUIT,DI:TRIPLE 5 OR/NOR,CHECKED	80009	156-1034-02
A20U247	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U300	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U301	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U306	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U310	156-0520-01	B010100	B030707	MICROCIRCUIT,DI:QUAD LATCH,SCRN	04713	MC10133PD/LD
A20U311	156-0230-02	B030708		MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U316	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U317	156-0688-01	B030708		MICROCIRCUIT,DI:DUAL J-K MASTER SLAVE FF	04713	MC10135PD/LD
A20U320	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U321	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U326	156-0205-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U327	156-0920-01	B030708		MICROCIRCUIT,DI:BIN TO 1-8 DECODER,SCRN	04713	MC10161 PD
A20U330	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U331	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U336	156-0205-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U337	156-1022-01	B030708		MICROCIRCUIT,DI:8 INPUT PRIORITY ENCODER	04713	MC10165PD/LD
A20U340	156-1032-02	B010100	B030707	MICROCIRCUIT,DI:QUINT 2 OR/NOR,CHK	80009	156-1032-02
A20U341	156-0520-01	B030708		MICROCIRCUIT,DI:QUAD LATCH,SCRN	04713	MC10133PD/LD
A20U346	156-1031-03	B010100	B030707	MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U347	156-1021-01	B030708		MICROCIRCUIT,DI:HEX & GATE,SCRN	04713	MC10197PD/LD
A20U400	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U401	156-0230-02	B030708		MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U406	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20U407	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U410	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U411	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U416	156-0920-01	B010100	B030707	MICROCIRCUIT,DI:BIN TO 1-8 DECODER,SCRN	04713	MC10161 PD
A20U417	156-0205-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	MC10102PD/LD
A20U420	156-1021-01	B010100	B030707	MICROCIRCUIT,DI:HEX & GATE,SCRN	04713	MC10197PD/LD
A20U421	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U426	156-0847-01	B010100	B030707	MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U427	156-0230-02	B030708		MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U430	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U431	156-1021-01	B030708		MICROCIRCUIT,DI:HEX & GATE,SCRN	04713	MC10197PD/LD
A20U436	156-1021-01	B010100	B030707	MICROCIRCUIT,DI:HEX & GATE,SCRN	04713	MC10197PD/LD
A20U437	156-1031-03	B030708		MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U440	156-1030-02	B010100	B030707	MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A20U441	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U447	156-1031-03	B030708		MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U500	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U501	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U506	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U507	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U510	156-0230-02	B010100	B030707	MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U511	156-0458-01	B030708		MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U516	156-0688-01	B010100	B030707	MICROCIRCUIT,DI:DUAL J-K MASTER SLAVE FF	04713	MC10135PD/LD
A20U517	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U520	156-1022-01	B010100	B030707	MICROCIRCUIT,DI:8 INPUT PRIORITY ENCODER	04713	MC10165PD/LD
A20U521	156-0880-02	B030708		MICROCIRCUIT,DI:DUAL D MASTER SLAVE FF	04713	MC10231PD/LD
A20U526	156-0230-02	B010100	B030707	MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A20U527	156-1501-00	B030708		MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A20U530	156-0458-01	B010100	B030707	MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	MC10104PD/LD
A20U536	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U537	156-1031-03	B030708		MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U540	156-1031-03	B010100	B030707	MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U547	156-1030-02	B030708		MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A20U600	156-0633-02	B010100	B030707	MICROCIRCUIT,DI:HEX D MAST-SLV FF,SCRN	04713	MC10176PD/LD
A20U601	156-0759-02	B030708		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U606	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U607	156-0633-02	B030708		MICROCIRCUIT,DI:HEX D MAST-SLV FF,SCRN	04713	MC10176PD/LD
A20U610	156-0633-02	B010100	B030707	MICROCIRCUIT,DI:HEX D MAST-SLV FF,SCRN	04713	MC10176PD/LD
A20U611	156-0847-01	B030708		MICROCIRCUIT,DI:64 BIT REGISTER FILE,SCRN	07263	10145ADCQR
A20U616	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U617	156-1019-02	B030708		MICROCIRCUIT,DI:DUAL 3-INPUT/OUTPUT,SCRN	04713	MC10210PD/LD
A20U620	156-0759-02	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	MC10103PD/LD
A20U621	156-0870-01	B030708		MICROCIRCUIT,DI:BCD DECADE CNTR,SCRN	07263	SL81658
A20U626	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U627	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U630	156-0252-02	B010100	B030707	MICROCIRCUIT,DI:TRIPLE 4-3-3 INP NOR GATE	04713	MC10106PD/LD
A20U636	156-0870-01	B010100	B030707	MICROCIRCUIT,DI:BCD DECADE CNTR,SCRN	07263	SL81658
A20U637	156-1032-02	B030708		MICROCIRCUIT,DI:QUINT 2 OR/NOR,CHK	80009	156-1032-02
A20U640	156-1030-02	B010100	B030707	MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A20U647	156-1031-03	B030708		MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U700	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U701	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U707	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U710	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20U711	156-1019-02	B030708		MICROCIRCUIT,DI:DUAL 3-INPUT/OUTPUT,SCRN	04713	MC10210PD/LD
A20U716	156-1019-02	B010100	B030707	MICROCIRCUIT,DI:DUAL 3-INPUT/OUTPUT,SCRN	04713	MC10210PD/LD
A20U717	156-0227-01	B030708		MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN	04713	MC1664LD
A20U720	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U721	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U726	156-0227-01	B010100	B030707	MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN	04713	MC1664LD
A20U727	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U730	156-1038-01	B010100	B030707	MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U736	156-1019-02	B010100	B030707	MICROCIRCUIT,DI:DUAL 3-INPUT/OUTPUT,SCRN	04713	MC10210PD/LD
A20U737	156-1034-02	B030708		MICROCIRCUIT,DI:TRIPLE 5 OR/NOR,CHECKED	80009	156-1034-02
A20U740	156-1033-03	B010100	B030707	MICROCIRCUIT,DI:QUINT DIFF LINE RCVR,CHK	80009	156-1033-03
A20U747	156-1031-03	B030708		MICROCIRCUIT,DI:TRIPLE D FF,CHK	80009	156-1031-03
A20U811	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U821	156-1038-01	B030708		MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A20U831	156-1030-02	B030708		MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,CHK	80009	156-1030-02
A20U841	156-1032-02	B030708		MICROCIRCUIT,DI:QUINT 2 OR/NOR,CHK	80009	156-1032-02

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26	670-4941-00	B010100	B019999	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-00
A26	670-4941-01	B020000	B029999	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-01
A26	670-4941-02	B030000	B030335	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-02
A26	670-4941-03	B030336	B030405	CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-03
A26	670-4941-04	B030406		CKT BOARD ASSY:DEFLECTION AMPLIFIER	80009	670-4941-04
A26C002	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C032	290-0766-00			CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	54473	ECEA2CS2R2
A26C040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C302	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A26C322	290-0134-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A26C323	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A26C324	290-0114-00			CAP.,FXD,ELCTLT:47UF,20%,6V	56289	150D476X0006B2
A26C326	290-0134-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A26C344	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A26C402	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C406	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A26C414	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A26C432	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C436	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A26C446	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A26C507	283-0239-00			CAP.,FXD,CER DI:0.022UF,10%,50V	72982	8121N083X7R0223K
A26C511	283-0239-00			CAP.,FXD,CER DI:0.022UF,10%,50V	72982	8121N083X7R0223K
A26C512	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A26C513	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A26C518	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C533	283-0239-00			CAP.,FXD,CER DI:0.022UF,10%,50V	72982	8121N083X7R0223K
A26C534	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A26C538	283-0239-00			CAP.,FXD,CER DI:0.022UF,10%,50V	72982	8121N083X7R0223K
A26C539	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A26C548	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C612	283-0238-00			CAP.,FXD,CER DI:0.01UF,10%,50V	72982	8121N075X7R0103K
A26C616	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C622	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A26C624	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A26C629	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C633	283-0238-00			CAP.,FXD,CER DI:0.01UF,10%,50V	72982	8121N075X7R0103K
A26C642	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C644	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A26C646	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A26C700	281-0775-00	B020000		CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C711	283-0139-00			CAP.,FXD,CER DI:150PF,20%,50V	51642	W100-050-X5F151M
A26C715	283-0139-00			CAP.,FXD,CER DI:150PF,20%,50V	51642	W100-050-X5F151M
A26C717	281-0158-00			CAP.,VAR,CER D1:7-45PF,50V	73899	DVJ-5006
A26C719	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A26C722	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A26C724	283-0348-00	B020000		CAP.,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	100-100-NP0-508B
A26C726	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C728	290-0164-00			CAP.,FXD,ELCTLT:1UF,+50-10%,150V	56289	500D105F150BA7
A26C730	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A26C732	281-0775-00	B020000		CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C737	283-0139-00			CAP.,FXD,CER DI:150PF,20%,50V	51642	W100-050-X5F151M
A26C738	281-0158-00			CAP.,VAR,CER D1:7-45PF,50V	73899	DVJ-5006
A26C739	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A26C743	283-0139-00			CAP.,FXD,CER DI:150PF,20%,50V	51642	W100-050-X5F151M

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26C744	283-0348-00	B020000		CAP.,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	100-100-NP0-508B
A26C804	290-0747-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	500D148
A26C805	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C812	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C813	290-0145-00	B010100	B030405	CAP.,FXD,ELCTLT:10UF,+75-10%,50V	56289	30D106G050CB9
A26C813	290-0194-00	B030406		CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	30D106F100C9
A26C814	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A26C818	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C820	290-0145-00	B010100	B030405	CAP.,FXD,ELCTLT:10UF,+75-10%,50V	56289	30D106G050CB9
A26C820	290-0194-00	B030406		CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	30D106F100C9
A26C821	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C822	290-0747-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	500D148
A26C834	285-0919-00			CAP.,FXD,PLSTC:0.22UF,10%,100V	56289	LP66A1B224K002
A26C836	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A26C846	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C906	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C910	283-0598-00			CAP.,FXD,MICA D:253PF,5%,300V	09023	CD15FD(253)J03
A26C918	290-0164-00			CAP.,FXD,ELCTLT:1UF,+50-10%,150V	56289	500D105F150BA7
A26C920	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C928	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A26C929	290-0846-00	B010100	B030405	CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A26C929	290-0768-00	B030406		CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A26C932	285-0919-00			CAP.,FXD,PLSTC:0.22UF,10%,100V	56289	LP66A1B224K002
A26CR211	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR312	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR316	152-0066-01			SEMICOND DEVICE:SILICON,400V,1A	15238	LG4012
A26CR322	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR330	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR332	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR340	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR342	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR400	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR430	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR614	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR615	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR636	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR730	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR816	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR818	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR900	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR924	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR925	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR926	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR927	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR942	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR944	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR946	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26CR948	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A26E940	119-0429-00			SURGE VOLTAGE P:145V,GAS FILLED	80009	119-0429-00
A26E942	119-0429-00			SURGE VOLTAGE P:145V,GAS FILLED	80009	119-0429-00
A26J002	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J010	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J012	131-1426-00			CONTACT SET,ELE:R ANGLE,0.250 L,STRIP OF 36	22526	65524-136
A26J020	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26J022	131-1426-00			CONTACT SET,ELE:R ANGLE,0.250 L,STRIP OF 36	22526	65524-136
A26J030	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J040	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J622	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A26J646	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A26J714	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A26J716	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A26J836	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A26J838	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A26J906	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J918	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J926	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26J926	----- -----			(QTY 2)		
A26J928	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26J928	----- -----			(QTY 2)		
A26J938	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26J948	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A26L500	108-0997-00			COIL,RF:FIXED,52NH	80009	108-0997-00
A26L512	108-0997-00			COIL,RF:FIXED,52NH	80009	108-0997-00
A26L532	108-0997-00			COIL,RF:FIXED,52NH	80009	108-0997-00
A26L540	108-0997-00			COIL,RF:FIXED,52NH	80009	108-0997-00
A26L610	108-1004-00			COIL,RF:FIXED,9NH	80009	108-1004-00
A26L611	108-1004-00			COIL,RF:FIXED,9NH	80009	108-1004-00
A26L640	108-1004-00			COIL,RF:FIXED,9NH	80009	108-1004-00
A26L641	108-1004-00			COIL,RF:FIXED,9NH	80009	108-1004-00
A26L700	108-0561-00	B020000		COIL,RF:3.75UH	80009	108-0561-00
A26L726	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26L728	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26L735	108-0561-00	B020000		COIL,RF:3.75UH	80009	108-0561-00
A26L806	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26L818	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26L820	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26L900	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26L902	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A26Q006	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q008	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q044	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q048	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q106	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q108	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q145	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q148	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q206	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q208	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q246	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q248	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q306	151-0126-00			TRANSISTOR:SILICON,NPN	04713	ST1046
A26Q308	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A26Q342	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A26Q345	151-0126-00			TRANSISTOR:SILICON,NPN	04713	ST1046
A26Q410	151-0169-00			TRANSISTOR:SILICON,NPN	04713	ST830
A26Q436	151-0169-00			TRANSISTOR:SILICON,NPN	04713	ST830
A26Q508	151-0411-00			TRANSISTOR:SILICON,NPN	04713	SRF709
A26Q512	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26Q514	151-0690-00			TRANSISTOR:NPN,SI,8 LEAD,TO-5	80009	151-0690-00
A26Q516	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q518	151-0411-00			TRANSISTOR:SILICON,NPN	04713	SRF709
A26Q532	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q533	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q534	151-0411-00			TRANSISTOR:SILICON,NPN	04713	SRF709
A26Q546	151-0411-00			TRANSISTOR:SILICON,NPN	04713	SRF709
A26Q626	151-0438-00			TRANSISTOR:SILICON,PNP,SEL FROM SPS692	80009	151-0438-00
A26Q630	151-0690-00			TRANSISTOR:NPN,SI,8 LEAD,TO-5	80009	151-0690-00
A26Q620	151-0438-00			TRANSISTOR:SILICON,PNP,SEL FROM SPS692	80009	151-0438-00
A26Q646	151-0438-00			TRANSISTOR:SILICON,PNP,SEL FROM SPS692	80009	151-0438-00
A26Q710	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A26Q712	153-0650-00			TRANSISTOR:MATCHED,2N5841	80009	153-0650-00
A26Q714	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A26Q716	----- -----			(PART OF Q712)		
A26Q736	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A26Q738	153-0650-00			TRANSISTOR:MATCHED,2N5841	80009	153-0650-00
A26Q742	151-0447-00			TRANSISTOR:SILICON,NPN	04713	SRF502-1
A26Q744	----- -----			(PART OF Q738)		
A26Q746	151-0438-00			TRANSISTOR:SILICON,PNP,SEL FROM SPS692	80009	151-0438-00
A26Q906	151-0280-00			TRANSISTOR:SILICON,PNP	04713	SS8065
A26Q936	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26Q938	151-0297-00			TRANSISTOR:SILICON,NPN	04713	ST613
A26R001	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A26R002	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R003	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R004	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R005	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A26R006	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R007	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	01121	CB4335
A26R008	321-0427-00			RES.,FXD,FILM:274K OHM,1%,0.125W	24546	NA55D2743F
A26R009	321-0427-00			RES.,FXD,FILM:274K OHM,1%,0.125W	24546	NA55D2743F
A26R010	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A26R016	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R017	321-0064-00			RES.,FXD,FILM:45.3 OHM,1%,0.125W	91637	MFF1816G45R30F
A26R018	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R026	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R028	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R032	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A26R040	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R042	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A26R043	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A26R044	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R046	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A26R048	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R102	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A26R103	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R104	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A26R105	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R106	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R107	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A26R108	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R109	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R110	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26R112	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R114	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R116	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R122	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R123	321-0064-00			RES.,FXD,FILM:45.3 OHM,1%,0.125W	91637	MFF1816G45R30F
A26R124	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R126	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R139	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A26R140	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R141	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	01121	CB4335
A26R142	321-0427-00			RES.,FXD,FILM:274K OHM,1%,0.125W	24546	NA55D2743F
A26R143	321-0427-00			RES.,FXD,FILM:274K OHM,1%,0.125W	24546	NA55D2743F
A26R144	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A26R145	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R146	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A26R147	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R148	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R149	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A26R202	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A26R203	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R204	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A26R205	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R206	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R207	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A26R208	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R209	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R210	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A26R211	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A26R212	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R214	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R216	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R218	311-1224-00			RES.,VAR,NONWIR:500 OHM,20%,0.50W	32997	3386F-T04-501
A26R222	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R224	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R226	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
A26R228	311-1224-00			RES.,VAR,NONWIR:500 OHM,20%,0.50W	32997	3386F-T04-501
A26R238	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R239	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A26R240	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R241	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R242	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A26R243	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R244	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A26R245	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A26R246	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R247	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A26R248	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R249	321-0399-00			RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F
A26R302	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A26R305	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A26R306	311-1230-00			RES.,VAR,NONWIR:20K OHM,20%,0.50W	32997	3386F-T04-203
A26R307	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A26R308	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A26R310	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26R311	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A26R312	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A26R313	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A26R314	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A26R315	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R316	321-0364-00			RES.,FXD,FILM:60.4K OHM,1%,0.125W	91637	MFF1816G60401F
A26R320	321-0075-00			RES.,FXD,FILM:59 OHM,1%,0.125W	91637	MFF1816G59R00F
A26R322	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	MFF1816G249R0F
A26R330	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R332	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R334	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R336	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R338	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502
A26R340	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A26R341	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A26R342	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A26R343	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A26R344	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A26R345	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A26R346	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A26R348	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A26R404	321-0258-00			RES.,FXD,FILM:4.75K OHM,1%,0.125W	91637	MFF1816G47500F
A26R406	321-0148-00			RES.,FXD,FILM:340 OHM,1%,0.125W	91637	MFF1816G340R0F
A26R407	311-1260-00			RES.,VAR,NONWIR:250 OHM,10%,0.50W	32997	3329P-L58-251
A26R408	311-0605-00			RES.,VAR,NONWIR:TRMR,200 OHM,0.5W	73138	82-23-2
A26R414	308-0388-00			RES.,FXD,WW:47 OHM,5%,3W	91637	CW2B-47R00J
A26R434	321-0258-00			RES.,FXD,FILM:4.75K OHM,1%,0.125W	91637	MFF1816G47500F
A26R440	311-1230-00			RES.,VAR,NONWIR:20K OHM,20%,0.50W	32997	3386F-T04-203
A26R443	321-0364-00			RES.,FXD,FILM:60.4K OHM,1%,0.125W	91637	MFF1816G60401F
A26R444	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A26R445	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R446	308-0388-00			RES.,FXD,WW:47 OHM,5%,3W	91637	CW2B-47R00J
A26R506	315-0180-00			RES.,FXD,CMPSN:18 OHM,5%,0.25W	01121	CB1805
A26R507	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A26R508	321-0176-00			RES.,FXD,FILM:665 OHM,1%,0.125W	91637	MFF1816G665R0F
A26R509	321-0112-00			RES.,FXD,FILM:143 OHM,1%,0.125W	91637	MFF1816G143R0F
A26R510	321-0053-00			RES.,FXD,FILM:34.8 OHM,1%,0.125W	91637	MFF1816G34R80F
A26R511	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A26R512	321-0053-00			RES.,FXD,FILM:34.8 OHM,1%,0.125W	91637	MFF1816G34R80F
A26R514	325-0045-00			RES.,FXD,FILM:46.4 OHM,0.5%,0.05W	03888	PME50 46.4 OHM
A26R517	315-0180-00			RES.,FXD,CMPSN:18 OHM,5%,0.25W	01121	CB1805
A26R518	317-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.125W	01121	BB7505
A26R519	317-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.125W	01121	BB7505
A26R524	311-1260-00			RES.,VAR,NONWIR:250 OHM,10%,0.50W	32997	3329P-L58-251
A26R530	321-0148-00			RES.,FXD,FILM:340 OHM,1%,0.125W	91637	MFF1816G340R0F
A26R531	311-0605-00			RES.,VAR,NONWIR:TRMR,200 OHM,0.5W	73138	82-23-2
A26R532	321-0053-00			RES.,FXD,FILM:34.8 OHM,1%,0.125W	91637	MFF1816G34R80F
A26R533	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A26R534	321-0053-00			RES.,FXD,FILM:34.8 OHM,1%,0.125W	91637	MFF1816G34R80F
A26R537	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A26R538	315-0180-00			RES.,FXD,CMPSN:18 OHM,5%,0.25W	01121	CB1805
A26R539	321-0176-00			RES.,FXD,FILM:665 OHM,1%,0.125W	91637	MFF1816G665R0F
A26R546	315-0180-00			RES.,FXD,CMPSN:18 OHM,5%,0.25W	01121	CB1805
A26R547	317-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.125W	01121	BB7505

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26R548	317-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.125W	01121	BB7505
A26R600	321-0095-00			RES.,FXD,FILM:95.3 OHM,1%,0.125W	91637	MFF1816G95R30F
A26R601	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R602	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R606	321-0248-00			RES.,FXD,FILM:3.74K OHM,1%,0.125W	91637	MFF1816G37400F
A26R609	321-0158-00	B010100	B019999	RES.,FXD,FILM:432 OHM,1%,0.125W	91637	MFF1816G432R0F
A26R609	321-0226-00	B020000		RES.,FXD,FILM:2.21K OHM,1%,0.125W	91637	MFF1816G22100F
A26R611	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R612	311-0978-00	B010100	B010139	RES.,VAR,NONWIR:250 OHM,10%,0.50W	73138	82-4-2
A26R612	311-0634-00	B010140		RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	32997	3329H-G48-501
A26R613	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R616	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R617	321-0093-01			RES.,FXD,FILM:90.9 OHM,0.5%,0.125W	91637	MFF1816G90R90D
A26R618	321-0093-01			RES.,FXD,FILM:90.9 OHM,0.5%,0.125W	91637	MFF1816G90R90D
A26R620	325-0052-00			RES.,FXD,FILM:80 OHM,0.5%,0.05W	03888	PME50 G80R00D
A26R622	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R624	325-0052-00			RES.,FXD,FILM:80 OHM,0.5%,0.05W	03888	PME50 G80R00D
A26R629	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A26R630	325-0045-00			RES.,FXD,FILM:46.4 OHM,0.5%,0.05W	03888	PME50 46.4 OHM
A26R631	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R632	321-0095-00			RES.,FXD,FILM:95.3 OHM,1%,0.125W	91637	MFF1816G95R30F
A26R633	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R634	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R635	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R636	311-0978-00	B010100	B010139	RES.,VAR,NONWIR:250 OHM,10%,0.50W	73138	82-4-2
A26R636	311-0634-00	B010140		RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	32997	3329H-G48-501
A26R637	321-0112-00			RES.,FXD,FILM:143 OHM,1%,0.125W	91637	MFF1816G143R0F
A26R641	323-0704-01			RES.,FXD,FILM:146 OHM,0.5%,0.5W	91637	MFF1226G146ROD
A26R643	321-0093-01			RES.,FXD,FILM:90.9 OHM,0.5%,0.125W	91637	MFF1816G90R90D
A26R644	321-0093-01			RES.,FXD,FILM:90.9 OHM,0.5%,0.125W	91637	MFF1816G90R90D
A26R646	325-0052-00			RES.,FXD,FILM:80 OHM,0.5%,0.05W	03888	PME50 G80R00D
A26R647	325-0052-00			RES.,FXD,FILM:80 OHM,0.5%,0.05W	03888	PME50 G80R00D
A26R648	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R700	321-0191-00	B010100	B019999	RES.,FXD,FILM:953 OHM,1%,0.125W	91637	MFF1816G953R0F
A26R700	321-0113-00	B020000		RES.,FXD,FILM:147 OHM,1%,0.125W	91637	MFF1816G147R0F
A26R708	325-0117-00			RES.,FXD,FILM:52.1 OHM,0.5%,0.05W	03888	PME50 52.1 OHM
A26R710	317-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.125W	01121	BB6805
A26R711	317-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.125W	01121	BB3005
A26R712	325-0047-00			RES.,FXD,FILM:25 OHM,0.5%,0.5W	03888	PME50
A26R714	317-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.125W	01121	BB6805
A26R715	317-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.125W	01121	BB3005
A26R717	311-1259-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3329P-L58-101
A26R718	325-0117-00			RES.,FXD,FILM:52.1 OHM,0.5%,0.05W	03888	PME50 52.1 OHM
A26R719	325-0053-00			RES.,FXD,FILM:50 OHM,1%,0.05W	03888	PME50C50R00F
A26R720	323-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.50W	91637	MFF1226G69R80F
A26R721	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A26R722	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A26R724	317-0820-00	B020000		RES.,FXD,CMPSN:82 OHM,5%,0.125W	01121	BB8205
A26R730	321-0248-00			RES.,FXD,FILM:3.74K OHM,1%,0.125W	91637	MFF1816G37400F
A26R732	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A26R733	317-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.125W	01121	BB3005
A26R734	321-0158-00	B010100	B019999	RES.,FXD,FILM:432 OHM,1%,0.125W	91637	MFF1816G432R0F
A26R734	321-0226-00	B020000		RES.,FXD,FILM:2.21K OHM,1%,0.125W	91637	MFF1816G22100F
A26R735	321-0191-00	B010100	B019999	RES.,FXD,FILM:953 OHM,1%,0.125W	91637	MFF1816G953R0F
A26R735	321-0113-00	B020000		RES.,FXD,FILM:147 OHM,1%,0.125W	91637	MFF1816G147R0F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26R736	317-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.125W	01121	BB6805
A26R737	325-0047-00			RES.,FXD,FILM:25 OHM,0.5%,0.5W	03888	PME50
A26R738	311-1259-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3329P-L58-101
A26R739	325-0053-00			RES.,FXD,FILM:50 OHM,1%,0.05W	03888	PME50C50R00F
A26R742	317-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.125W	01121	BB6805
A26R743	317-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.125W	01121	BB3005
A26R746	323-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.50W	91637	MFF1226G69R80F
A26R748	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A26R800	323-0147-01			RES.,FXD,FILM:332 OHM,1%,0.5W	91637	MFF126G332ROD
A26R802	323-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.50W	91637	MFF1226G69R80F
A26R810	323-0147-01			RES.,FXD,FILM:332 OHM,1%,0.5W	91637	MFF126G332ROD
A26R814	315-0107-00	B010100	B029999	RES.,FXD,CMPSN:100M OHM,5%,0.25W	01121	CB1075
A26R814	315-0475-00	B030000		RES.,FXD,CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
A26R816	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R830	325-0117-00			RES.,FXD,FILM:52.1 OHM,0.5%,0.05W	03888	PME50 52.1 OHM
A26R832	323-0147-01			RES.,FXD,FILM:332 OHM,1%,0.5W	91637	MFF126G332ROD
A26R833	323-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.50W	91637	MFF1226G69R80F
A26R834	321-0486-00			RES.,FXD,FILM:1.13M OHM,1%,0.125W	91637	HMF188G11303F
A26R840	325-0117-00			RES.,FXD,FILM:52.1 OHM,0.5%,0.05W	03888	PME50 52.1 OHM
A26R844	323-0147-01			RES.,FXD,FILM:332 OHM,1%,0.5W	91637	MFF126G332ROD
A26R846	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A26R900	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A26R901	315-0103-00	B010100	B029999	RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R901	315-0512-00	B030000		RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A26R906	321-0452-00			RES.,FXD,FILM:499K OHM,1%,0.125W	91637	MFF1816G49902F
A26R912	315-0152-00	B010100	B019999	RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A26R912	308-0077-00	B020000	B029999	RES.,FXD,WW:1K OHM,5%,3W	91637	CW2B-10000J-TR
A26R912	308-0304-00	B030000		RES.,FXD,WW:1.5K OHM,1%,3W	91637	RS2B-B15000F
A26R914	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R916	321-0790-00	B010100	B01013	RES.,FXD,FILM:990K OHM,1%,0.125W	14298	AME55D9903F
A26R916	321-0790-01	B010140		RES.,FXD,FILM:990K OHM,0.5%,0.125W	91637	HFF1104G99002D
A26R921	315-0566-00			RES.,FXD,CMPSN:56M OHM,5%,0.25W	01121	CB5665
A26R922	315-0566-00			RES.,FXD,CMPSN:56M OHM,5%,0.25W	01121	CB5665
A26R924	321-0440-00			RES.,FXD,FILM:374K OHM,1%,0.125W	91637	MFF1816G37402F
A26R926	321-0440-00			RES.,FXD,FILM:374K OHM,1%,0.125W	91637	MFF1816G37402F
A26R928	301-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.50W	01121	EB5625
A26R930	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A26R933	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A26R935	321-0486-00			RES.,FXD,FILM:1.13M OHM,1%,0.125W	91637	HMF188G11303F
A26R936	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A26R937	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A26R940	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045
A26R941	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A26R942	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045
A26R944	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R948	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26TP002	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP022	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP040	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP041	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP122	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP216	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP226	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP315	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26TP316	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP320	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP330	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP331	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP332	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP333	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP344	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP420	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP446	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP448	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP806	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP816	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP924	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP936	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26TP938	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A26U314	156-0846-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC7905CT
A26U808	156-0770-02			MICROCIRCUIT,LI:OPERATIONAL AMPL,CHK	80009	156-0770-02
A26U930	156-0158-04			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	01295	N99320JG
A26VR400	152-0514-00			SEMICOND DEVICE:ZENER,0.4W,10V,1%	80009	152-0514-00
A26VR432	152-0514-00			SEMICOND DEVICE:ZENER,0.4W,10V,1%	80009	152-0514-00
A26VR835	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	TD3810983
A26VR928	152-0241-00			SEMICOND DEVICE:ZENER,0.4W,33V,5%	04713	SZG35009K5
A26VR934	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	TD3810983
A26W800	131-0566-00	B030336		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A26W810	131-0566-00	B030336		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A44	----- -----			CKT BOARD ASSY:VERTICAL INTERCONNECT		
A44J020	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J100	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J110	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J120	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J200	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J210	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J220	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A44J320	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A46	----- -----			CKT BOARD ASSY:PLUG IN INTERFACE		
A46C002	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	59821	2DDH66J103Z
A46C036	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	59821	2DDH66J103Z
A46C300	290-0769-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	500D152
A46C346	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A46C410	290-0769-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	500D152
A46C414	290-0769-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	500D152
A46C418	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	1C10C0G221K200B
A46C420	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	1C10C0G221K200B
A46C448	283-0028-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	59660	0805585Y5SO222M
A46C500	290-0769-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	500D152
A46C510	290-0769-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	56289	500D152
A46C540	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	59821	2DDH66J103Z
A46CR016	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR018	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR024	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR028	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR110	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR112	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR114	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR116	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR118	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR122	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR124	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR126	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR128	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR144	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR146	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR210	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR212	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR214	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR216	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR218	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR224	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR225	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR226	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR227	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR228	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR229	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR248	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR316	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR324	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR326	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A46CR328	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR340	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR420	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR422	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR542	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR546	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46CR548	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A46L540	108-0325-00			COIL,RF:0.5UH	80009	108-0325-00
A46J100	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A46J520	131-1607-00			CONN,RCPT,ELEC:CKT BD MTG,36 CONTACT	22526	65000-22
A46Q010	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q012	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q014	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q016	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q018	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q020	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q022	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q024	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q025	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q026	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q028	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q030	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q034	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q110	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q112	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q122	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q124	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q326	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A46Q328	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A46Q448	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46Q544	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A46Q546	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A46R004	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A46R006	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A46R036	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A46R114	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A46R130	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A46R140	307-0606-00			RES NTWK,FXD FI:9.15K OHM,2%,0.15W	32997	4310R-101-154
A46R218	307-0606-00			RES NTWK,FXD FI:9.15K OHM,2%,0.15W	32997	4310R-101-154
A46R240	307-0503-00			RES NTWK,THK FI:(9)510 OHM,20%,0.125W	91637	MSP10A01-511G
A46R242	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R244	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R246	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R304	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A46R314	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A46R316	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A46R318	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A46R320	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A46R324	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A46R326	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A46R328	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A46R340	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R342	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A46R346	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A46R348	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A46R418	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A46R420	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A46R424	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R425	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R427	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R428	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A46R440	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A46R442	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A46R443	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A46R444	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A46R445	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A46R448	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A46R502	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A46R548	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A46R564	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A46U120	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164
A46U220	155-0017-00			MICROCIRCUIT,DI:ML,ZERO LOGIC COUNTER	80009	155-0017-00
A46U224	155-0017-00			MICROCIRCUIT,DI:ML,ZERO LOGIC COUNTER	80009	155-0017-00
A46VR242	152-0217-00			SEMICOND DEVICE:ZENER,0.4W,8.2V,5%	04713	SZG20

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A52	670-5772-00	B010100	B019999	CKT BOARD ASSY:MPU MEMORY	80009	670-5772-00
A52	670-5772-01	B020000		CKT BOARD ASSY:MPU MEMORY	80009	670-5772-01
A52C011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C211	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C301	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C311	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C331	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C401	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C411	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C423	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C531	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C533	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C601	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C603	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A52C621	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C623	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52U011	160-0456-01			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0456-01
A52U012	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A52U013	160-0457-02			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0457-02
A52U021	160-0455-01			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0455-01
A52U031	160-0454-02			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0454-02
A52U101	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A52U111	160-0452-01			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0452-01
A52U201	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A52U211	160-0453-02			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0453-02
A52U213	160-0450-03			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0450-03
A52U221	160-0451-01			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0451-01
A52U231	160-0448-01			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0448-01
A52U311	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A52U401	160-0449-02	B010100	B019999	MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0449-02
A52U401	160-0449-03	B020000		MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0449-03
A52U411	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A52U421	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A52U423	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A52U431	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A52U433	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A52U501	156-1028-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM W/3 ST	80009	156-1028-01
A52U511	156-1028-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM W/3 ST	80009	156-1028-01
A52U521	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A52U531	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A52U607	160-0447-02			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0447-02
A52U611	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A52U621	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A52U631	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A54	670-5771-00	B010100	B030221	CKT BOARD ASSY:MPU	80009	670-5771-00
A54	670-5771-01	B030222	B030389	CKT BOARD ASSY:MPU	80009	670-5771-01
A54	670-5771-02	B030390		CKT BOARD ASSY:MPU	80009	670-5771-02
A54C012	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C022	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A54C044	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C104	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C106	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A54C114	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A54C128	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C204	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	59660	835-515-Z5D0102K
A54C206	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C212	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A54C218	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C302	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C314	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C322	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A54C334	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C524	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C604	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C606	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C636	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C702	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C728	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C734	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	59660	835-515-Z5D0102K
A54C802	283-0051-00			CAP.,FXD,CER DI:0.0033UF,5%,100V	56289	1C20C0G332J100B
A54C844	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C912	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C914	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C926	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A54C932	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A54C934	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	59660	835-515-Z5D0102K
A54C942	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A54CR104	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A54CR106	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A54CR828	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A54F836	159-0116-00	B010100	B030221	FUSE,CARTRIDGE:1A,125V,0.4 SEC,0.17 LEADS	75915	273001
A54F836	159-0114-00	B030222		FUSE,CARTRIDGE:1A,125VAC,FAST-BLOW	71400	GFA 1
A54F844	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A54J012	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J012	----- -----			(QTY 3)		
A54J216	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J216	----- -----			(QTY 3)		
A54J224	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J224	----- -----			(QTY 3)		
A54J234	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J234	----- -----			(QTY 3)		
A54J712	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J712	----- -----			(QTY 3)		
A54J714	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J714	----- -----			(QTY 3)		
A54J716	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J716	----- -----			(QTY 3)		
A54J718	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J718	----- -----			(QTY 3)		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A54J720	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A54J720	----- -----			(QTY 3)		
A54L934	108-0858-00			COIL,RF:FIXED,3.2NH	80009	108-0858-00
A54Q212	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A54Q218	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A54Q728	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A54R106	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A54R112	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A54R114	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A54R122	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R123	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A54R124	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R126	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R127	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A54R204	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A54R206	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R212	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A54R213	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R214	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R216	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A54R304	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R602	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A54R728	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A54R802	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A54R814	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R824	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A54R832	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A54R834	321-0261-00			RES.,FXD,FILM:5.11K OHM,1%,0.125W	91637	MFF1816G51100F
A54R836	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A54R838	321-0264-00			RES.,FXD,FILM:5.49K OHM,1%,0.125W	91637	MFF1816G54900F
A54R844	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	MFF1816G82500F
A54R926	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R932	311-1224-00			RES.,VAR,NONWIR:500 OHM,20%,0.50W	32997	3386F-T04-501
A54R934	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A54R936	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A54R938	321-0373-00			RES.,FXD,FILM:75K OHM, 1%,0.125W	91637	MFF1816G75001F
A54TP104	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54TP112	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54TP222	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54TP702	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54TP734	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54TP834	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54TP838	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A54U001	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG FF	01295	SN74LS113NP3
A54U012	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A54U022	156-0078-02			MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A54U032	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A54U102	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A54U114	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	27014	DM8016
A54U122	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A54U132	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A54U204	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV,SCRN	04713	SN74LS221N/J
A54U206	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A54U222	156-0426-05			MICROCIRCUIT,DI:MICROPROCESSOR,SCREENED	80009	156-0426-05

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A54U234	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A54U312	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A54U314	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A54U322	156-1018-00			MICROCIRCUIT,DI:HEX THREE STATE BUFFER	04713	MC6885/MC8T95L
A54U332	156-1018-00			MICROCIRCUIT,DI:HEX THREE STATE BUFFER	04713	MC6885/MC8T95L
A54U334	156-1018-00			MICROCIRCUIT,DI:HEX THREE STATE BUFFER	04713	MC6885/MC8T95L
A54U402	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A54U412	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A54U424	156-0427-04			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A54U512	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A54U514	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A54U522	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A54U524	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A54U532	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A54U536	156-0730-02			MICROCIRCUIT,DI:QUAD 2-INP NOR BFR,BURN-IN	01295	SN74LS33
A54U538	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A54U606	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A54U612	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A54U614	156-0384-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS03
A54U626	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A54U636	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A54U638	156-0730-02			MICROCIRCUIT,DI:QUAD 2-INP NOR BFR,BURN-IN	01295	SN74LS33
A54U702	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A54U712	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A54U722	156-0384-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS03
A54U728	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A54U732	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A54U734	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A54U814	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A54U822	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A54U832	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A54U836	156-0096-01	B010100	B030221	MICROCIRCUIT,LI:VOLTAGE COMPARATOR,CHK	80009	156-0096-01
A54U836	156-1126-01	B030222		MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A54U912	156-0347-02			MICROCIRCUIT,DI:10 TO 4 LINE ENCDR,SCRN	80009	156-0347-02
A54U926	155-0014-01			MICROCIRCUIT,DI:ML,ANALOG TO DECIMAL CONV	80009	155-0014-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A56	670-5773-00	B010100	B029999	CKT BOARD ASSY:IEEE 488 INTERFACE	80009	670-5773-00
A56	670-5773-02	B030000		CKT BOARD ASSY:IEEE 488 INTERFACE	80009	670-5773-02
A56C112	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C120	283-0077-00			CAP.,FXD,CER DI:330PF,5%,500V	59660	831-500B331J
A56C122	283-0065-01			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835582Z5E00102J
A56C130	283-0620-00			CAP.,FXD,MICA D:470PF,1%,300V	00853	D155F4771FO
A56C132	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C134	283-0649-00			CAP.,FXD,MICA D:105PF,1%,300V	00853	D155F1050F0
A56C136	281-0786-00	B010100	B029999	CAP.,FXD,CER DI:150PF,10%,100V	51642	G1710100NP0151K
A56C200	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C202	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C206	281-0580-00			CAP.,FXD,CER DI:470PF,10%,500V	04222	7001-1374
A56C212	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C230	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C300	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C302	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C306	281-0580-00			CAP.,FXD,CER DI:470PF,10%,500V	04222	7001-1374
A56C310	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C312	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C330	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C331	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C332	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C334	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A56C410	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C420	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C432	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C502	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C512	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C520	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C532	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C602	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56C604	281-0536-00			CAP.,FXD,CER DI:1000PF,10%,500V	72982	301000 X 5P0102K
A56C620	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A56CR312	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A56CR332	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A56J030	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A56J030	----- -----			(QTY 3)		
A56J300	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A56J300	----- -----			(QTY 3)		
A56J402	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A56J500	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A56J502	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A56J602	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A56J602	----- -----			(QTY 3)		
A56Q600	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A56R010	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A56R020	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R030	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A56R104	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A56R120	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A56R122	321-0305-00			RES.,FXD,FILM:14.7K OHM,1%,0.125W	91637	MFF1816G14701F
A56R130	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R132	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A56R134	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A56R200	311-1917-00			RES.,VAR,NONWIR:TRMR,5K OHM,10%,0.5W	73138	72-198-0
A56R202	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A56R204	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R206	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	MFF1816G249R0F
A56R208	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A56R210	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R212	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A56R232	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R300	311-1917-00			RES.,VAR,NONWIR:TRMR,5K OHM,10%,0.5W	73138	72-198-0
A56R302	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R304	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	MFF1816G249R0F
A56R306	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A56R308	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A56R310	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A56R312	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A56R330	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A56R332	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A56R400	307-0502-00			RES NTWK,FXD,FI:(9) 1.8K OHM,20%,0.125W	91637	MSP10A01-182M
A56R420	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A56R510	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R530	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A56R600	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A56R610	321-0173-00			RES.,FXD,FILM:619 OHM,1%,0.125W	91637	MFF1816G619R0F
A56R611	321-0237-00			RES.,FXD,FILM:2.87K OHM,1%,0.125W	91637	MFF1816G28700F
A56R612	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A56R614	321-0213-00			RES.,FXD,FILM:1.62K OHM,1%,0.125W	91637	MFF1816G16200F
A56S400	260-1827-00			SWITCH,ROCKER:5,SPST	81073	76SB05S
A56S402	260-1827-00			SWITCH,ROCKER:5,SPST	81073	76SB05S
A56TP002	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56TP004	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56TP012	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56TP232	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56TP322	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56TP500	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56TP600	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A56U012	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A56U022	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A56U030	156-0652-02			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL NOR GATE	01295	SN74LS266
A56U032	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A56U102	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A56U110	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A56U112	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A56U120	156-0405-03			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602
A56U122	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A56U130	156-0405-03			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602
A56U132	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A56U200	156-0770-02			MICROCIRCUIT,LI:OPERATIONAL AMPL,CHK	80009	156-0770-02
A56U202	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A56U210	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A56U212	156-0617-02			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,SCRN	01295	SN74393NP3
A56U220	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A56U222	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A56U230	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A56U232	156-0419-02			MICROCIRCUIT,DI:DUAL 4 INP NAND LINE DRVR	07263	74S140

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A56U300	156-0770-02			MICROCIRCUIT,LI:OPERATIONAL AMPL,CHK	80009	156-0770-02
A56U302	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A56U310	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	04713	MC3410CLD
A56U312	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A56U320	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A56U322	156-0652-02			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL NOR GATE	01295	SN74LS266
A56U330	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A56U332	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	04713	MC3410CLD
A56U400	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A56U410	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A56U412	156-0427-04			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A56U420	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A56U430	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A56U500	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A56U502	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A56U510	156-1025-02			MICROCIRCUIT,DI:INVERTING QUAD BUS XCVR	01295	SN74LS242
A56U512	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A56U520	156-1025-02			MICROCIRCUIT,DI:INVERTING QUAD BUS XCVR	01295	SN74LS242
A56U522	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A56U530	156-1133-01			MICROCKT,INTFC:QUAD 3-STATE XCVR,CHK	80009	156-1133-01
A56U532	156-1133-01			MICROCKT,INTFC:QUAD 3-STATE XCVR,CHK	80009	156-1133-01
A56U600	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A56U602	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A56U610	156-0851-02			MICROCIRCUIT,DI:QUAD TO BUS DRIVER,SCREENED	18324	N8509A(NB OR FB)
A56U612	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A56U620	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A56U622	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A56U630	156-0600-01			MICROCIRCUIT,DI:QUAD BUS XSVR,CHK	80009	156-0600-01
A56U632	156-0600-01			MICROCIRCUIT,DI:QUAD BUS XSVR,CHK	80009	156-0600-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62	670-4958-00	B010100	B030221	CKT BOARD ASSY:TRIGGER	80009	670-4958-00
A62	670-4958-01	B030222	B030368	CKT BOARD ASSY:TRIGGER	80009	670-4958-01
A62	670-4958-02	B030369		CKT BOARD ASSY:TRIGGER	80009	670-4958-02
A62C006	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C012	283-0625-00			CAP.,FXD,MICA D:220PF,1%,500V	00853	D105F221F0
A62C014	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C016	283-0785-00			CAP.,FXD,MICA D:250PF,1%,500V	09023	CD15FD251F03
A62C020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C022	290-0283-00			CAP.,FXD,ELCTLT:0.47UF,10%,35V	56289	162D474X9035BC2
A62C114	283-0641-00			CAP.,FXD,MICA D:180PF,1%,100V	00853	DD155F181F0
A62C116	283-0786-00			CAP.,FXD,MICA D:745PF,1%,500V	09023	CD19FD(745)F03
A62C122	283-0051-00			CAP.,FXD,CER DI:0.0033UF,5%,100V	56289	1C20C0G332J100B
A62C126	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0
A62C132	283-0629-00			CAP.,FXD,MICA D:62PF,1%,500V	00853	D105E620F0
A62C146	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C202	281-0659-00			CAP.,FXD,CER DI:4.3PF,+/-0.25PF,500V	59660	301-000C0H0439C
A62C204	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C206	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C217	281-0547-00			CAP.,FXD,CER DI:2.7PF,10%,500V	04222	7001--COJ-2R7C
A62C222	283-0637-00			CAP.,FXD,MICA D:20PF,2.5%,100V	00853	D151E200D0
A62C224	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C226	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C228	283-0605-00			CAP.,FXD,MICA D:678PF,1%,300V	00853	D153F6780F0
A62C229	283-0605-00			CAP.,FXD,MICA D:678PF,1%,300V	00853	D153F6780F0
A62C234	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131M058Z5U0474M
A62C238	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	20932	201-E0-100AT820J
A62C244	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
A62C305	281-0513-00			CAP.,FXD,CER DI:27PF,+/-5.4PF,500V	59660	301-055P2G0270M
A62C314	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C316	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C322	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A62C326	283-0065-01			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835582Z5E00102J
A62C328	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C329	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131M058Z5U0474M
A62C332	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A62C342	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C410	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C412	283-0625-00			CAP.,FXD,MICA D:220PF,1%,500V	00853	D105F221F0
A62C414	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C422	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	51642	G1710100NP0151K
A62C426	290-0283-00			CAP.,FXD,ELCTLT:0.47UF,10%,35V	56289	162D474X9035BC2
A62C432	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C436	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C438	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C439	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131M058Z5U0474M
A62C446	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C504	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C512	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C514	283-0785-00			CAP.,FXD,MICA D:250PF,1%,500V	09023	CD15FD251F03
A62C524	283-0051-00			CAP.,FXD,CER DI:0.0033UF,5%,100V	56289	1C20C0G332J100B
A62C604	281-0659-00			CAP.,FXD,CER DI:4.3PF,+/-0.25PF,500V	59660	301-000C0H0439C
A62C610	283-0641-00			CAP.,FXD,MICA D:180PF,1%,100V	00853	DD155F181F0
A62C612	283-0786-00			CAP.,FXD,MICA D:745PF,1%,500V	09023	CD19FD(745)F03
A62C622	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62C624	283-0637-00			CAP.,FXD,MICA D:20PF,2.5%,100V	00853	D151E200D0
A62C626	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C628	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C634	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131M058Z5U0474M
A62C638	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	20932	201-E0-100AT820J
A62C642	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
A62C644	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C702	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C704	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C706	281-0513-00			CAP.,FXD,CER DI:27PF,+/-5.4PF,500V	59660	301-055P2G0270M
A62C712	281-0547-00			CAP.,FXD,CER DI:2.7PF,10%,500V	04222	7001--COJ-2R7C
A62C716	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C718	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C724	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A62C736	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A62C742	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C816	283-0065-01			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835582Z5E00102J
A62C822	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131M058Z5U0474M
A62C824	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C826	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	51642	G1710100NP0151K
A62C834	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C836	283-0629-00			CAP.,FXD,MICA D:62PF,1%,500V	00853	D105E620F0
A62C840	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C844	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C912	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C914	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C916	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A62C918	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A62C926	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A62C936	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C938	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A62C939	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131M058Z5U0474M
A62CR012	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR012	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR014	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR014	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR112	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR112	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR113	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR113	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR113	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR114	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR116	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR122	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR124	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR126	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR128	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR132	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR242	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR402	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR404	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR414	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR414	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR416	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR416	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62CR514	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR514	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR516	152-0141-02	B010100	B01013	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR516	152-0075-00	B010140		SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR526	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR527	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR528	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR529	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR538	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR544	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR612	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR614	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR902	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62CR904	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A62E120	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E122	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E128	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E202	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E522	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E524	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E604	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62E624	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A62F938	159-0116-00	B010100	B030221	FUSE,CARTRIDGE:1A,125V,0.4 SEC,0.17 LEADS	75915	273001
A62F938	159-0114-00	B030222		FUSE,CARTRIDGE:1A,125VAC,FAST-BLOW	71400	GFA 1
A62J102	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A62J104	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A62J202	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A62J506	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A62J602	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A62J606	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A62L108	108-0682-00			COIL,RF:66NH	80009	108-0682-00
A62L604	108-0682-00			COIL,RF:66NH	80009	108-0682-00
A62L916	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A62L918	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A62L924	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A62Q042	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A62Q128	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A62Q144	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A62Q232	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A62Q234	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A62Q344	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A62Q624	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A62Q626	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A62Q628	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A62Q632	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A62Q634	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A62Q836	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A62R004	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A62R006	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R008	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	MFF1816G49R90F
A62R014	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A62R022	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A62R024	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A62R026	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62R028	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A62R102	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R106	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A62R108	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A62R112	321-0071-00			RES.,FXD,FILM:53.6 OHM,1%,0.125W	91637	MFF1816G53R60F
A62R126	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A62R128	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A62R130	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A62R132	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A62R134	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A62R135	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A62R136	321-0166-00			RES.,FXD,FILM:523 OHM,1%,0.125W	91637	MFF1816G523R0F
A62R138	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A62R140	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R141	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R142	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A62R144	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R202	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A62R204	311-1240-00			RES.,VAR,NONWIR:25K OHM,10%,0.50W	73138	72-30-0
A62R210	301-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.50W	01121	EB2215
A62R211	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R212	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R213	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R214	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R215	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A62R216	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A62R217	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A62R218	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R219	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A62R222	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A62R224	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A62R226	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A62R232	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R234	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R236	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A62R238	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A62R242	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A62R302	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A62R304	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A62R305	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R306	311-1240-00			RES.,VAR,NONWIR:25K OHM,10%,0.50W	73138	72-30-0
A62R307	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R308	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A62R314	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A62R316	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A62R318	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A62R322	323-0155-00			RES.,FXD,FILM:402 OHM,1%,0.50W	75042	CECT0-4020F
A62R324	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A62R325	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R326	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A62R328	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A62R332	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R334	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R336	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62R337	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R338	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A62R339	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A62R342	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A62R344	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R346	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R408	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A62R412	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A62R422	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A62R424	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A62R502	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R504	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	MFF1816G49R90F
A62R506	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R512	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A62R518	321-0071-00			RES.,FXD,FILM:53.6 OHM,1%,0.125W	91637	MFF1816G53R60F
A62R522	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A62R524	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A62R526	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A62R530	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A62R532	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A62R534	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A62R535	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A62R536	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A62R537	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R538	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A62R539	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A62R602	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A62R604	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A62R606	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A62R610	301-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.50W	01121	EB2215
A62R612	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R614	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R615	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R616	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R617	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A62R618	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A62R620	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A62R622	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A62R624	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A62R626	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A62R628	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A62R630	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A62R632	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A62R635	321-0166-00			RES.,FXD,FILM:523 OHM,1%,0.125W	91637	MFF1816G523R0F
A62R636	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R637	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R638	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A62R639	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A62R702	311-1240-00			RES.,VAR,NONWIR:25K OHM,10%,0.50W	73138	72-30-0
A62R703	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A62R704	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A62R706	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A62R712	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A62R714	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62R716	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A62R718	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A62R724	323-0155-00			RES.,FXD,FILM:402 OHM,1%,0.50W	75042	CECT0-4020F
A62R726	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A62R728	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A62R736	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R738	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R739	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A62R802	311-1240-00			RES.,VAR,NONWIR:25K OHM,10%,0.50W	73138	72-30-0
A62R804	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R806	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A62R810	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A62R814	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A62R816	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A62R822	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A62R824	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A62R832	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R834	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	MFF1816G24R90F
A62R836	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R838	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R922	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A62R924	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A62T104	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A62T508	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A62U002	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A62U022	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A62U204	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A62U226	155-0126-00			MICROCIRCUIT,LI:TRIGGER AMPLIFIER	80009	155-0126-00
A62U236	155-0109-01			MICROCIRCUIT,LI:MONOLITHIC TRIGGER	80009	155-0109-01
A62U242	156-0172-02			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	01295	SN74123
A62U246	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A62U312	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A62U346	156-0368-03			MICROCIRCUIT,DI:TTL TO ECL QUAD TRANS	04713	MC10124LD
A62U402	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A62U412	156-0067-12			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	UA741CJG
A62U422	156-1255-01			MICROCIRCUIT,LI:D/A CONVERTER,BURN-IN	04713	DAC-08HQDS
A62U442	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A62U502	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A62U522	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A62U532	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A62U542	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A62U544	156-0172-02			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	01295	SN74123
A62U608	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A62U644	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A62U716	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A62U722	155-0126-00			MICROCIRCUIT,LI:TRIGGER AMPLIFIER	80009	155-0126-00
A62U732	155-0109-01			MICROCIRCUIT,LI:MONOLITHIC TRIGGER	80009	155-0109-01
A62U742	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A62U746	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A62U816	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A62U818	156-0067-12			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	UA741CJG
A62U828	156-1255-01			MICROCIRCUIT,LI:D/A CONVERTER,BURN-IN	04713	DAC-08HQDS
A62U844	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A62U848	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A62VR325	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A68	670-4940-00	B010100	B030658	CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-4940-00
A68	670-4940-01	B030659		CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-4940-01
A68C320	290-0773-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A68C420	290-0773-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A68C458	290-0283-00			CAP.,FXD,ELCTLT:0.47UF,10%,35V	56289	162D474X9035BC2
A68CR458	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A68J006	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J006	----- -----			(QTY 2)		
A68J006	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J100	131-1658-00			CONNECTOR,RCPT,:CKT CD EDGE,36-72 CONTACT	05574	000231-3601
A68J104	131-1658-00			CONNECTOR,RCPT,:CKT CD EDGE,36-72 CONTACT	05574	000231-3601
A68J108	131-2168-00			CONN,RCPT,ELEC:CKT CD,50/100 FEM CONTACTS	05574	000231-3606
A68J118	131-2171-00			TERM. SET,PIN:40/80,0.025 SQ	00779	4-87422-0
A68J332	131-2437-00			CONN,RCPT,ELEC:CKT BD,36/72 CONTACT	95238	60012172DDGDF50
A68J334	131-2437-00			CONN,RCPT,ELEC:CKT BD,36/72 CONTACT	95238	60012172DDGDF50
A68J340	131-0931-00			CONN,RCPT,ELEC:CKT BD,50/100 CONTACT	05574	3VH50/1JV3
A68J430	131-2437-00			CONN,RCPT,ELEC:CKT BD,36/72 CONTACT	95238	60012172DDGDF50
A68J436	131-2437-00			CONN,RCPT,ELEC:CKT BD,36/72 CONTACT	95238	60012172DDGDF50
A68J438	131-2437-00			CONN,RCPT,ELEC:CKT BD,36/72 CONTACT	95238	60012172DDGDF50
A68J500	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A68J520	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J520	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J522	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J522	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J524	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J524	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J526	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J526	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J528	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J528	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J530	131-2437-00	B010100	B030658	CONN,RCPT,ELEC:CKT BD,36/72 CONTACT	95238	60012172DDGDF50
A68J530	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J531	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J531	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J532	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J532	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J534	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J534	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J536	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J536	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J546	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J546	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J548	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J548	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J550	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J550	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J552	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J552	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J554	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J554	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J556	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J556	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A68J558	131-1857-00	B010100	B030658	TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A68J558	131-1343-00	B030659		TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A68J559	131-1425-00			CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
A68R340	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A68R344	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A68R540	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A68R546	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A76	670-4949-00	B010100	B029999	CKT BOARD ASSY:HIGH VOLTAGE OSCILLATOR	80009	670-4949-00
A76	670-4949-01	B030000	B030405	CKT BOARD ASSY:HIGH VOLTAGE OSCILLATOR	80009	670-4949-01
A76	670-4949-02	B030406		CKT BOARD ASSY:HIGH VOLTAGE OSCILLATOR	80009	670-4949-02
A76C002	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A76C004	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A76C100	285-0882-00	B010100	B029999	CAP.,FXD,PLSTC:0.047UF,10%,100V	56289	LP66A1B473K001
A76C100	285-0674-00	B030000		CAP.,FXD,PLSTC:0.01UF,10%,100V	56289	192P10392
A76C106	285-1073-00			CAP.,FXD,PLSTC:0.0033UF,5%,400V	14752	230B1E332J
A76C108	290-0768-00	B010100	B030405	CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A76C108	290-0880-00	B030406		CAP.,FXD,ELCTLT:10UF,+50-10%,160V	55680	UHU2C100TEA
A76C110	285-1075-00	B030000		CAP.,FXD,PLSTC:0.1UF,5%,100V	14752	230B1B104J
A76C112	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A76C114	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A76C308	290-0816-00			CAP.,FXD,ELCTLT:400UF,+75-10%,50V	56289	39D985
A76C310	290-0816-00			CAP.,FXD,ELCTLT:400UF,+75-10%,50V	56289	39D985
A76CR006	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A76CR007	152-0141-02	B030000		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A76CR302	152-0414-00	B030000		SEMICOND DEVICE:SILICON,200V,0.75A	12969	UTR308
A76J001	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A76J001	----- -----			(QTY 6)		
A76L010	108-0473-00			COIL,RF:150UH	80009	108-0473-00
A76L206	108-0473-00			COIL,RF:150UH	80009	108-0473-00
A76R106	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A76R108	315-0101-00	B010100	B029999	RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A76R108	301-0101-00	B030000		RES.,FXD,CMPSN:100 OHM,5%,0.50W	01121	EB1015
A76R202	301-0224-00	B010100	B010174	RES.,FXD,CMPSN:220K OHM,5%,0.50W	01121	EB2245
A76R202	301-0184-00	B010175		RES.,FXD,CMPSN:180K OHM,5%,0.50W	01121	EB1845
A76R204	301-0224-00	B010100	B010174	RES.,FXD,CMPSN:220K OHM,5%,0.50W	01121	EB2245
A76R204	301-0184-00	B010175		RES.,FXD,CMPSN:180K OHM,5%,0.50W	01121	EB1845
A76R302	308-0793-00			RES.,FXD,WW:0.51 OHM,5%,0.50W	75042	BW20 .51 OHM 5%
A76T110	120-1271-00	B010100	B029999	XFMR,PWR,STU:HV	80009	120-1271-00
A76T110	120-1271-01	B030000		XFMR,PWR,STU:HV	80009	120-1271-01
A76VR110	152-0520-00	B030000		SEMICOND DEVICE:ZENER,1W,12V,5%	15238	Z6033

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80	670-5442-00	B010100	B030174	CKT BOARD ASSY:LINE POWER	80009	670-5442-00
A80	670-5442-01	B030175		CKT BOARD ASSY:LINE POWER	80009	670-5442-01
A80C001	290-0535-00			CAP.,FXD,ELCTLT:33UF,20%,10V	56289	196D336X0010KA1
A80C021	290-0535-00			CAP.,FXD,ELCTLT:33UF,20%,10V	56289	196D336X0010KA1
A80C031	290-0535-00			CAP.,FXD,ELCTLT:33UF,20%,10V	56289	196D336X0010KA1
A80C051	290-0535-00			CAP.,FXD,ELCTLT:33UF,20%,10V	56289	196D336X0010KA1
A80C061	283-0261-00			CAP.,FXD,CER DI:0.01UF,20%,4000V	04222	5742-0001
A80C111	283-0078-00			CAP.,FXD,CER DI:0.001UF,20%,500V	59660	0801 547X5F0102M
A80C121	285-1164-00			CAP.,FXD,PLSTC:5UF,10%,400V	84411	TRW-35-50594
A80C161	290-0829-00			CAP.,FXD,ELCTLT:750UF,+100-10%,200V	90201	PFP751SR2J3P2
A80C211	283-0351-00			CAP.,FXD,CER DI:5000PF,20%,3000V	59660	848-562Z5U0502M
A80C221	285-1164-00			CAP.,FXD,PLSTC:5UF,10%,400V	84411	TRW-35-50594
A80C241	290-0829-00			CAP.,FXD,ELCTLT:750UF,+100-10%,200V	90201	PFP751SR2J3P2
A80C261	285-1082-00			CAP.,FXD,PLSTC:0.47UF,20%,200V	14752	230B1C474
A80C311	283-0008-00			CAP.,FXD,CER DI:0.1UF,20%,500V	56289	3C37X7R104M500B
A80C341	290-0829-00			CAP.,FXD,ELCTLT:750UF,+100-10%,200V	90201	PFP751SR2J3P2
A80C361	290-0829-00			CAP.,FXD,ELCTLT:750UF,+100-10%,200V	90201	PFP751SR2J3P2
A80C401	283-0008-00			CAP.,FXD,CER DI:0.1UF,20%,500V	56289	3C37X7R104M500B
A80C402	283-0134-00			CAP.,FXD,CER DI:0.47UF,+80-20%,50V	72982	8131N087Z5U0474Z
A80C403	283-0060-00	B010100	B030174	CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A80C403	283-0054-00	B030175		CAP.,FXD,CER DI:150PF,5%,200V	59660	855-535U2J0 151J
A80C413	290-0767-00	B010100	B030174	CAP.,FXD,ELCTLT:4.7UF,+75-10%,160V	56289	5020228
A80C413	290-0880-00	B030175		CAP.,FXD,ELCTLT:10UF,+50-10%,160V	55680	UHU2C100TEA
A80C414	290-0767-00	B010100	B030174	CAP.,FXD,ELCTLT:4.7UF,+75-10%,160V	56289	5020228
A80C414	290-0880-00	B030175		CAP.,FXD,ELCTLT:10UF,+50-10%,160V	55680	UHU2C100TEA
A80C461	290-0829-00			CAP.,FXD,ELCTLT:750UF,+100-10%,200V	90201	PFP751SR2J3P2
A80C501	283-0084-00			CAP.,FXD,CER DI:270PF,5%,1000V	59660	838 533X5F0 2715
A80C521	290-0758-00			CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227
A80C522	283-0084-00			CAP.,FXD,CER DI:270PF,5%,1000V	59660	838 533X5F0 2715
A80C531	283-0006-00			CAP.,FXD,CER DI:0.02UF,+80-20%,500V	59660	0841545Z5V00203Z
A80C541	283-0006-00			CAP.,FXD,CER DI:0.02UF,+80-20%,500V	59660	0841545Z5V00203Z
A80C542	290-0829-00			CAP.,FXD,ELCTLT:750UF,+100-10%,200V	90201	PFP751SR2J3P2
A80C601	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	59660	0831085Z5E00471J
A80C611	285-1050-00			CAP.,FXD,PLSTC:0.1UF,1%,200V	14752	230B1C104F
A80C711	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A80C721	285-1050-00			CAP.,FXD,PLSTC:0.1UF,1%,200V	14752	230B1C104F
A80C731	283-0006-00			CAP.,FXD,CER DI:0.02UF,+80-20%,500V	59660	0841545Z5V00203Z
A80CR011	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A80CR012	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A80CR013	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A80CR021	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A80CR031	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A80CR032	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A80CR041	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A80CR051	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A80CR241	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A80CR311	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR312	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR313	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR314	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR315	152-0141-02	B010100	B030174	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR321	152-0585-00			SEMICOND DEVICE:SILICON,BRIDGE,200V,1A	80009	152-0585-00
A80CR411	152-0141-02	B010100	B030174	SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR501	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80CR511	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A80CR531	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A80CR532	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A80CR533	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A80CR534	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A80CR601	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR611	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR612	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR701	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR702	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR703	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80CR711	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A80DS261	150-0035-00			LAMP,GLOW:90V,0.3MA,AID-T,WIRE LD	000LI	JH005/3011JA
A80E641	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	74276	CG230L
A80E721	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	74276	CG230L
A80J2	131-2182-00			TERM. SET,PIN:1 X 5,0.156 SPACING,RTANG	27264	09-47-1052
A80J3	131-2387-00			TERM SET,FEEDTH:3 PIN,INSULATED	27264	09-88-2031
A80J4	131-2250-00			CONN,RCPT,ELEC:CKT BD,5 MALE	27264	09-61-1053
A80L261	108-0995-00			COIL,RF:FIXED,30UH	80009	108-0995-00
A80L301	108-0691-00			COIL,RF:1.8MH	76493	02279
A80L302	108-0691-00			COIL,RF:1.8MH	76493	02279
A80L321	108-0995-00			COIL,RF:FIXED,30UH	80009	108-0995-00
A80L331	108-0995-00			COIL,RF:FIXED,30UH	80009	108-0995-00
A80L451	108-0995-00			COIL,RF:FIXED,30UH	80009	108-0995-00
A80L521	108-0691-00			COIL,RF:1.8MH	76493	02279
A80Q011	151-0632-00			TRANSISTOR:SILICON,NPN	04713	SJE1946
A80Q012	151-0632-00			TRANSISTOR:SILICON,NPN	04713	SJE1946
A80Q031	151-0632-00			TRANSISTOR:SILICON,NPN	04713	SJE1946
A80Q041	151-0632-00			TRANSISTOR:SILICON,NPN	04713	SJE1946
A80Q411	151-0443-00			TRANSISTOR:SILICON,PNP	04713	SPS7950
A80Q412	151-0292-00			TRANSISTOR:SILICON,NPN	01295	A5T5058
A80Q501	151-0678-00			TRANSISTOR:SILICON,NPN	04713	MJE13005
A80Q521	151-0678-00			TRANSISTOR:SILICON,NPN	04713	MJE13005
A80R011	308-0703-00			RES.,FXD,WW:1.8 OHM,5%,2W	75042	BWH-1R800J
A80R021	308-0703-00			RES.,FXD,WW:1.8 OHM,5%,2W	75042	BWH-1R800J
A80R031	308-0703-00			RES.,FXD,WW:1.8 OHM,5%,2W	75042	BWH-1R800J
A80R041	308-0703-00			RES.,FXD,WW:1.8 OHM,5%,2W	75042	BWH-1R800J
A80R211	306-0121-00			RES.,FXD,CMPSN:120 OHM,10%,2W	01121	HB1211
A80R251	305-0473-00	B010100	B030174	RES.,FXD,CMPSN:47K OHM,5%,2W	01121	HB4735
A80R251	305-0363-00	B030175		RES.,FXD,CMPSN:36K OHM,5%,2W	01121	HB3635
A80R315	315-0242-00	B030175		RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A80R321	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A80R341	305-0473-00	B010100	B030174	RES.,FXD,CMPSN:47K OHM,5%,2W	01121	HB4735
A80R341	305-0363-00	B030175		RES.,FXD,CMPSN:36K OHM,5%,2W	01121	HB3635
A80R361	315-0475-00			RES.,FXD,CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
A80R401	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A80R402	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A80R403	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R404	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R405	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R411	315-0242-00	B030175		RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A80R421	305-0223-00			RES.,FXD,CMPSN:22K OHM,5%,2W	01121	HB2235
A80R431	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A80R601	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80R602	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R603	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R604	321-0340-00			RES.,FXD,FILM:34K OHM,1%,0.125W	91637	MFF1816G34001F
A80R605	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A80R606	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R611	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A80R612	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A80R621	321-0436-00			RES.,FXD,FILM:340K OHM,1%,0.125W	91637	MFF1816G34002F
A80R622	308-0708-00			RES.,FXD,WW:5.5K OHM,3%,7W	91637	RS7-B55000H
A80R651	307-0350-00			RES.,THERMAL:7.5 OHM,10%,3.9%/DEG C	15454	75DJ7R5R0220SS
A80R661	307-0350-00			RES.,THERMAL:7.5 OHM,10%,3.9%/DEG C	15454	75DJ7R5R0220SS
A80R701	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R702	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R703	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A80R704	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R705	315-0914-00			RES.,FXD,CMPSN:910K OHM,5%,0.25W	01121	CB9145
A80R706	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A80R711	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A80R712	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A80R713	321-0438-00			RES.,FXD,FILM:357K OHM,1%,0.125W	91637	MFF1816G35702F
A80R714	321-0438-00			RES.,FXD,FILM:357K OHM,1%,0.125W	91637	MFF1816G35702F
A80R721	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A80T101	120-1267-00			TRANSFORMER,RF:BASE DRIVE	80009	120-1267-00
A80T301	120-1268-00			XFMR,PWR,STPDN:HF	80009	120-1268-00
A80T421	120-1165-00			TRANSFORMER,RF:TOROID,COMMON MODE REJECT	80009	120-1165-00
A80T511	120-1164-00			TRANSFORMER,RF:FAN BASE DRIVE	80009	120-1164-00
A80U405	156-0105-02			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER,SEL	01295	LM301AJG4
A80U611	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A80VR411	152-0282-00			SEMICOND DEVICE:ZENER,0.4W,30V,5%	14552	1N972B
A80VR601	152-0304-00			SEMICOND DEVICE:ZENER,0.4W,20V,5%	15238	Z5411
A80VR602	152-0514-00			SEMICOND DEVICE:ZENER,0.4W,10V,1%	80009	152-0514-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A82	670-4956-00	B010100	B030174	CKT BOARD ASSY:MAIN	80009	670-4956-00
A82	670-4956-03	B030175		CKT BOARD ASSY:MAIN	80009	670-4956-03
A82C011	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A82C021	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A82C031	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A82C051	290-0183-00			CAP.,FXD,ELCTLT:1UF,10%,35V	90201	TAC105K035P02
A82C061	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A82C121	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A82C122	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A82C131	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A82C132	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A82C161	283-0065-00	B010100	B030174	CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5EO102J
A82C161	283-0001-00	B030175		CAP.,FXD,CER DI:0.005UF,+100-0%,500V	59821	2DDH61L502P
A82C251	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A82C252	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A82C262	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5EO102J
A82C311	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A82C312	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A82C321	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A82C341	290-0183-00			CAP.,FXD,ELCTLT:1UF,10%,35V	90201	TAC105K035P02
A82C351	283-0267-00	B010100	B020729	CAP.,FXD,CER DI:0.01UF,20%,500V	60705	562CBD501AL103MA
A82C351	283-0008-00	B030730		CAP.,FXD,CER DI:0.1UF,20%,500V	56289	3C37X7R104M500B
A82C361	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A82C441	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A82C442	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A82C451	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A82C452	283-0267-00			CAP.,FXD,CER DI:0.01UF,20%,500V	60705	562CBD501AL103MA
A82C453	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A82C454	283-0267-00			CAP.,FXD,CER DI:0.01UF,20%,500V	60705	562CBD501AL103MA
A82C461	283-0594-00			CAP.,FXD,MICA D:0.001UF,1%,100V	00853	D151F102F0
A82C462	283-0001-00			CAP.,FXD,CER DI:0.005UF,+100-0%,500V	59821	2DDH61L502P
A82C541	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A82CR021	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A82CR022	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A82CR031	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A82CR032	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A82CR051	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR061	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A82CR121	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR122	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR221	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR222	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR241	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR321	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR341	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR342	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR351	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82CR361	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A82L341	108-0691-00			COIL,RF:1.8MH	76493	02279
A82L421	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A82L452	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A82P020	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A82P040	131-1792-00			CONTACT ASSY,EL:12 MALE CONTACT,FLAT WAFER	27264	09-70-2121
A82P060	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A82P320	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A82Q021	151-0622-00			TRANSISTOR:SILICON,PNP	27014	92PU51A
A82Q022	151-0622-00			TRANSISTOR:SILICON,PNP	27014	92PU51A
A82Q023	151-0260-00			TRANSISTOR:SILICON,NPN	80009	151-0260-00
A82Q024	151-0260-00			TRANSISTOR:SILICON,NPN	80009	151-0260-00
A82Q061	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A82Q062	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A82Q121	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A82Q122	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A82Q151	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A82Q161	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A82Q301	151-0478-01			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0478-01
A82Q311	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A82Q411	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A82Q412	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A82Q413	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A82R051	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R061	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R062	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R063	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R064	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R121	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A82R122	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A82R123	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A82R124	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A82R131	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A82R132	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A82R151	315-0184-00			RES.,FXD,CMPSN:180K OHM,5%,0.25W	01121	CB1845
A82R152	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A82R153	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A82R154	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R155	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A82R161	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R162	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R163	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R164	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R165	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A82R242	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A82R321	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A82R322	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A82R323	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A82R331	321-0365-00			RES.,FXD,FILM:61.9K OHM,1%,0.125W	91637	MFF1816G61901F
A82R332	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R333	321-0388-00			RES.,FXD,FILM:107K OHM,1%,0.125W	91637	MFF1816G10702F
A82R334	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R335	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R336	321-0379-00			RES.,FXD,FILM:86.6K OHM,1%,0.125W	91637	MFF1816G86601F
A82R341	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A82R342	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A82R351	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R352	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A82R353	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A82R354	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A82R355	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A82R361	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A82R362	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R363	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A82R364	321-0326-00			RES.,FXD,FILM:24.3K OHM,1%,0.125W	91637	MFF1816G24301F
A82R365	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A82R366	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A82R411	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A82R412	321-0463-00			RES.,FXD,FILM:649K OHM,1%,0.125W	91637	MFF1816G64902F
A82R421	321-0170-00			RES.,FXD,FILM:576 OHM,1%,0.125W	91637	MFF1816G576R0F
A82R422	321-0928-07			RES.,FXD,FILM:250 OHM,0.1%,0.125W	91637	MFF1816C250R0B
A82R423	321-0815-07			RES.,FXD,FILM:4.1K OHM,0.1%,0.125W	91637	MFF1816C41000B
A82R431	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A82R432	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A82R433	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R434	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A82R435	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A82R441	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R442	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A82R451	321-0966-03			RES.,FXD,FILM:40K OHM,0.25%,0.125W	91637	MFF1816D40001C
A82R452	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A82R453	321-0445-00	B010100	B010174	RES.,FXD,FILM:422K OHM,1%,0.125W	91637	MFF1816G42202F
A82R453	321-0452-00	B010175		RES.,FXD,FILM:499K OHM,1%,0.125W	91637	MFF1816G49902F
A82R461	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A82R511	321-0451-00			RES.,FXD,FILM:487K OHM,1%,0.125W	91637	MFF1816G48702F
A82R512	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A82R513	321-0450-00			RES.,FXD,FILM:475K OHM,1%,0.125W	91637	MFF1816G47502F
A82R514	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A82R521	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72-23-0
A82R531	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A82TP141	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A82TP252	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A82TP253	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A82TP311	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A82TP431	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A82U141	156-0366-02			MICROCIRCUIT,DI:DUAL D FLIP-FLOP,CHK	80009	156-0366-02
A82U231	156-0350-02			MICROCIRCUIT,DI:QUAD 2 INPUT NAND GATE,SEL	80009	156-0350-02
A82U251	156-0577-02			MICROCIRCUIT,DI:QUAD 2-INP AND GATE,SEL	27014	DM74C08
A82U261	156-0876-01			MICROCIRCUIT,DI:HEX SCHMITT TRIGGER,SCRN	80009	156-0876-01
A82U331	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A82U451	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A82VR411	153-0058-00			SEMICOND DVC,SE:ZENER,SEL,6.2V,5%,10MA	80009	153-0058-00
A82VR412	152-0236-00			SEMICOND,DEVICE:ZENER,0.4W,12.5V,4%	14552	TD333881
A82VR421	152-0317-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	04713	SZG20012

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A86	670-4955-00	B010100	B030254	CKT BOARD ASSY:RECTIFIER FILTER	80009	670-4955-00
A86	670-4955-01	B030255		CKT BOARD ASSY:RECTIFIER FILTER	80009	670-4955-01
A86C011	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A86C021	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A86C031	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A86C041	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A86C042	283-0002-00			CAP.,FXD,CER DI:0.01UF,+80-20%,500V	59821	SDDH69L103Z
A86C061	290-0798-00			CAP.,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187HO4ODM5C
A86C062	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A86C101	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A86C112	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A86C113	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A86C141	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A86C151	283-0002-00			CAP.,FXD,CER DI:0.01UF,+80-20%,500V	59821	SDDH69L103Z
A86C161	290-0758-00			CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227
A86C162	290-0798-00			CAP.,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187HO4ODM5C
A86C351	283-0267-00			CAP.,FXD,CER DI:0.01UF,20%,500V	60705	562CBD501AL103MA
A86C361	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A86C362	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A86C411	283-0267-00			CAP.,FXD,CER DI:0.01UF,20%,500V	60705	562CBD501AL103MA
A86C461	290-0798-00			CAP.,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187HO4ODM5C
A86C501	283-0267-00	B010100	B030729	CAP.,FXD,CER DI:0.01UF,20%,500V	60705	562CBD501AL103MA
A86C501	283-0083-00	B030730		CAP.,FXD,CER DI:0.0047UF,20%,500V	72982	811-565C471J
A86C511	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A86C512	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A86C513	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A86C611	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5EO102J
A86C612	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A86C621	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A86C111	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A86CR041	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	03508	A115AX39
A86CR042	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	03508	A115AX39
A86CR043	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	03508	A115AX39
A86CR101	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A86CR102	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A86CR103	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A86CR141	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	03508	A115AX39
A86CR142	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	03508	A115AX39
A86CR143	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	03508	A115AX39
A86CR161	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR162	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR201	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A86CR202	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A86CR203	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A86CR261	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR262	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR311	152-0642-00			SEMICOND DEVICE:RECT,SI,35V,40A,DO-5	01281	SD5218
A86CR351	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR352	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR353	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR451	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR501	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A86CR561	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A86CR562	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A86CR611	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A86L001	108-0950-00			COIL,RF:5.5UH	80009	108-0950-00
A86L011	108-0974-00			COIL,RF:FIXED,4UH	80009	108-0974-00
A86L051	108-0909-00			COIL,RF:FIXED,1.6MH	80009	108-0909-00
A86L121	108-0911-00			COIL,RF:FIXED,65UH	80009	108-0911-00
A86L141	108-0950-00			COIL,RF:5.5UH	80009	108-0950-00
A86L151	108-0900-00			COIL,RF:FXD,300MH,POT CORE	80009	108-0900-00
A86L221	108-0911-00			COIL,RF:FIXED,65UH	80009	108-0911-00
A86L251	108-0909-00			COIL,RF:FIXED,1.6MH	80009	108-0909-00
A86L261	108-0909-00			COIL,RF:FIXED,1.6MH	80009	108-0909-00
A86L421	108-0911-00			COIL,RF:FIXED,65UH	80009	108-0911-00
A86L521	108-0911-00			COIL,RF:FIXED,65UH	80009	108-0911-00
A86Q411	151-0391-00			TRANSISTOR:SILICON,PNP	80009	151-0391-00
A86Q501	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A86Q502	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A86R041	303-0100-00			RES.,FXD,CMPSN:10 OHM,5%,1W	01121	GB1005
A86R141	303-0100-00			RES.,FXD,CMPSN:10 OHM,5%,1W	01121	GB1005
A86R201	308-0802-00			RES.,FXD,WW:0.01 OHM,5%,5W	91637	LVR5 .01 OHM 5%
A86R211	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A86R301	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A86R401	301-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.50W	01121	EB6815
A86R402	321-0926-07			RES.,FXD,FILM:4K OHM,0.1%,0.125W	91637	MFF1816C40000B
A86R403	321-0926-07			RES.,FXD,FILM:4K OHM,0.1%,0.125W	91637	MFF1816C40000B
A86R404	321-0319-02			RES.,FXD,FILM:20.5K OHM,0.5%,0.125W	24546	NC55C2052D
A86R411	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A86R501	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A86R502	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A86R503	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A86R504	321-0365-00			RES.,FXD,FILM:61.9K OHM,1%,0.125W	91637	MFF1816G61901F
A86R511	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A86R512	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A86R513	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A86R514	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A86R515	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A86R516	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A86R517	307-0106-00			RES.,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB47G5
A86R531	308-0778-00	B010100	B030729	RES.,FXD,WW:3 OHM,5%,5W	91637	CW-5-3R000J
A86R531	308-0803-00	B030730		RES.,FXD,WW:4 OHM,5%,5W	91637	RS5-K4R000J
A86R532	308-0802-00			RES.,FXD,WW:0.01 OHM,5%,5W	91637	LVR5 .01 OHM 5%
A86R611	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A86R612	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A86R613	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	24546	NA4D1004F
A86R614	321-0358-00			RES.,FXD,FILM:52.3K OHM,1%,0.125W	91637	MFF1816G52301F
A86T051	120-1266-00			TRANSFORMER,RF:TOROID,2 WINDINGS	80009	120-1266-00
A86T211	120-1272-00			XFMR,PWR,STU:HF	80009	120-1272-00
A86T241	120-1270-00	B010100	B030244	XFMR,PWR,STPDN:HF	80009	120-1270-00
A86T241	120-1270-01	B030245		XFMR,PWR,STPDN:HF ANALOG PWR	80009	120-1270-01
A86T551	120-1269-00			XFMR,PWR,STPDN:HF	80009	120-1269-00
A86TP002	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A86U501	156-1126-01			MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A86U511	156-1126-01			MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A86U601	156-1225-00			MICROCIRCUIT,LI:DUAL COMPARATOR,8 DIP	27014	LM393N

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A88	670-4954-00	B010100	B030174	CKT BOARD ASSY:REGULATOR	80009	670-4954-00
A88	670-4954-02	B030175		CKT BOARD ASSY:REGULATOR	80009	670-4954-02
A88C002	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C004	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
A88C014	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C028	283-0057-00			CAP.,FXD,CER DI:0.1UF,+80-20%,200V	56289	2C20Z5U104Z200B
A88C040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C044	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A88C102	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C104	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5EO102J
A88C124	285-0598-00			CAP.,FXD,PLSTC:0.01UF,5%,100V	19396	DU490B103J
A88C134	285-0862-00			CAP.,FXD,PLSTC:0.001,10%,100V	56289	192P10292
A88C144	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5EO102J
A88C148	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C200	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A88C202	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C210	285-0862-00			CAP.,FXD,PLSTC:0.001,10%,100V	56289	192P10292
A88C214	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C218	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C220	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C222	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C226	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C228	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A88C232	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C236	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A88C240	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C246	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C248	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C252	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C304	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C316	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A88C326	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A88C334	285-1101-00			CAP.,FXD,PLSTC:0.022UF,10%,20OV	19396	223K02PT485
A88C336	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C338	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C344	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A88C346	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A88C348	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C352	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A88C410	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A88C442	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A88C506	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A88C520	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A88C526	285-0918-00			CAP.,FXD,PLSTC:0.001UF,5%,200 V	56289	LP66A1C102J002
A88C530	285-1101-00			CAP.,FXD,PLSTC:0.022UF,10%,20OV	19396	223K02PT485
A88C542	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A88C544	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A88C602	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A88C642	290-0806-00			CAP.,FXD,ELCTLT:3.3UF,+75-10%,350VDC	55680	UHU2V3RTEA
A88C652	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A88CR004	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A88CR042	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A88CR118	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR128	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A88CR130	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR142	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR144	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A88CR156	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR200	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A88CR204	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR206	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR216	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A88CR248	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A88CR256	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A88CR350	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A88CR352	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A88CR520	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A88CR522	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A88CR530	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A88J420	131-1857-00			TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
A88J420	----- -----			(QTY 2)		
A88J450	131-1792-00			CONTACT ASSY,EL:12 MALE CONTACT,FLAT WAFER	27264	09-70-2121
A88L356	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A88L446	108-0858-00			COIL,RF:FIXED,3.2NH	80009	108-0858-00
A88L448	108-0858-00			COIL,RF:FIXED,3.2NH	80009	108-0858-00
A88L548	108-0858-00			COIL,RF:FIXED,3.2NH	80009	108-0858-00
A88L554	108-0858-00			COIL,RF:FIXED,3.2NH	80009	108-0858-00
A88L556	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A88L558	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A88L652	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A88Q010	151-0476-00			TRANSISTOR:SILICON,NPN	02735	68430
A88Q012	151-0407-01			TRANSISTOR:SILICON,NPN	80009	151-0407-01
A88Q014	151-0656-00			TRANSISTOR:SILICON,NPN	04713	SJE1972
A88Q018	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A88Q030	151-0224-02			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0224-02
A88Q034	151-0656-00			TRANSISTOR:SILICON,NPN	04713	SJE1972
A88Q040	151-0657-00			TRANSISTOR:SILICON,PNP	04713	SJE1973
A88Q042	151-0453-00			TRANSISTOR:SILICON,PNP	80009	151-0453-00
A88Q044	151-0482-00			TRANSISTOR:SILICON,PNP	80009	151-0482-00
A88Q050	151-0406-01			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0406-01
A88Q106	151-0232-00			TRANSISTOR:SILICON,NPN,DUAL	07263	SP12141
A88Q148	151-0354-00			TRANSISTOR:SILICON,PNP,DUAL	32293	ITS1200A
A88Q152	151-0347-01			TRANSISTOR:SILICON,NPN,PRESTRESSED	80009	151-0347-01
A88Q202	151-0350-01			TRANSISTOR:PNP,SI PRESTRESSED & TESTED	80009	151-0350-01
A88Q414	151-0103-02			TRANSISTOR:SILICON,NPN,SEL	04713	OBD
A88Q436	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A88Q446	151-0134-00			TRANSISTOR:SILICON,PNP	80009	151-0134-00
A88Q524	151-0292-00			TRANSISTOR:SILICON,NPN	01295	A5T5058
A88Q532	151-0292-00			TRANSISTOR:SILICON,NPN	01295	A5T5058
A88Q620	151-0232-00			TRANSISTOR:SILICON,NPN,DUAL	07263	SP12141
A88Q636	151-0497-01			TRANSISTOR:SILICON,NPN	80009	151-0497-01
A88R002	321-0691-07			RES.,FXD,FILM:42.7K OHM,0.1%,0.125W	91637	MFF1816C42701B
A88R004	321-1709-01			RES.,FXD,FILM:800 OHM,0.5%,0.125W	91637	MFF1816G800R0D
A88R006	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A88R008	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A88R014	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A88R020	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A88R028	321-0126-00			RES.,FXD,FILM:200 OHM,1%,0.125W	91637	MFF1816G200R0F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A88R030	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A88R032	321-0266-00			RES.,FXD,FILM:5.76K OHM,1%,0.125W	91637	MFF1816G57600F
A88R034	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A88R042	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A88R044	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A88R050	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A88R056	308-0799-00			RES.,FXD,WW:1 OHM,1%,4W	91637	NS21R000F
A88R058	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A88R100	321-1710-07			RES.,FXD,FILM:435K OHM,0.1%,0.125W	91637	MFF1816C43501B
A88R102	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A88R104	303-0243-00			RES.,FXD,CMPSN:24K OHM,5%,1W	01121	GB2435
A88R110	308-0799-00			RES.,FXD,WW:1 OHM,1%,4W	91637	NS21R000F
A88R112	308-0643-00			RES.,FXD,WW:0.1 OHM,3%,3W	91637	RS2B-ER1000H
A88R114	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	MFF1816G249R0F
A88R115	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A88R116	321-0339-00	B010100	B010174	RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A88R116	321-0336-00	B010175		RES.,FXD,FILM:30.9K OHM,1%,0.125W	91637	MFF1816G30901F
A88R117	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A88R118	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A88R122	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A88R126	308-0643-00			RES.,FXD,WW:0.1 OHM,3%,3W	91637	RS2B-ER1000H
A88R128	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A88R130	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	01121	CB1345
A88R134	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A88R136	308-0643-00			RES.,FXD,WW:0.1 OHM,3%,3W	91637	RS2B-ER1000H
A88R140	321-0126-00			RES.,FXD,FILM:200 OHM,1%,0.125W	91637	MFF1816G200R0F
A88R142	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A88R143	321-0325-00	B010100	B010174	RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A88R143	321-0297-00	B010175		RES.,FXD,FILM:12.1K OHM,1%,0.125W	91637	MFF1816G12101F
A88R144	303-0243-00			RES.,FXD,CMPSN:24K OHM,5%,1W	01121	GB2435
A88R146	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A88R147	321-0385-00	B010100	B010174	RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A88R147	321-0373-00	B010175		RES.,FXD,FILM:75K OHM, 1%,0.125W	91637	MFF1816G75001F
A88R148	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A88R151	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A88R152	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A88R154	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A88R156	321-0264-07			RES.,FXD,FILM:5.49K OHM,0.1%,0.125W	91637	MFF1816C54900B
A88R204	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A88R207	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A88R208	321-0720-03	B010100	B010174	RES.,FXD,FILM:60K OHM,0.25%,0.125W	91637	MFF1816D60001C
A88R208	321-0359-00	B010175		RES.,FXD,FILM:53.6K OHM,1%,0.125W	91637	MFF1816G53601F
A88R210	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A88R211	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A88R212	321-0964-07			RES.,FXD,FILM:49.31K OHM,0.1%,0.125W	91637	MFF1816C49311B
A88R214	321-0178-00			RES.,FXD,FILM:698 OHM,1%,0.125W	91637	MFF1816G698R0F
A88R224	321-0815-07			RES.,FXD,FILM:4.1K OHM,0.1%,0.125W	91637	MFF1816C41000B
A88R226	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A88R234	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A88R242	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A88R252	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A88R254	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A88R255	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72-23-0
A88R256	323-0266-00			RES.,FXD,FILM:5.76K OHM,1%,0.5W	91637	MFF1226G57600F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A88R304	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A88R306	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A88R312	303-0102-00			RES.,FXD,CMPSN:1K OHM,5%,1W	01121	GB1025
A88R314	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
A88R316	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A88R322	301-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.50W	01121	EB5615
A88R326	321-0193-03			RES.,FXD,FILM:1K OHM,0.25%,0.125W	91637	MFF1816D10000C
A88R338	321-1296-07			RES.,FXD,FILM:12K OHM,0.1%,0.125W	91637	MFF1816C12001B
A88R340	321-0332-07			RES.,FXD,FILM:28K OHM,0.1%,0.125W	91637	MFF1816C28001B
A88R344	301-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.50W	01121	EB4315
A88R348	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A88R352	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A88R413	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	24546	NA4D1004F
A88R420	315-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.25W	01121	CB1505
A88R428	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A88R436	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A88R443	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A88R456	303-0102-00			RES.,FXD,CMPSN:1K OHM,5%,1W	01121	GB1025
A88R504	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A88R506	321-0617-00			RES.,FXD,FILM:111K OHM,1%,0.125W	91637	MFF1816G11102F
A88R508	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A88R510	321-0756-00			RES.,FXD,FILM:50K OHM,1%,0.125W	24546	NA55D5002F
A88R511	321-0431-00			RES.,FXD,FILM:301K OHM,1%,0.125W	91637	MFF1816G30102F
A88R512	321-0452-00			RES.,FXD,FILM:499K OHM,1%,0.125W	91637	MFF1816G49902F
A88R514	321-0402-00			RES.,FXD,FILM:150K OHM,1%,0.125W	24546	NA55D1503F
A88R516	321-0267-00			RES.,FXD,FILM:5.9K OHM,1%,0.125W	91637	MFF1816G59000F
A88R518	321-1623-02			RES.,FXD,FILM:55.5K OHM,0.5%,0.125W	91637	MFF1816D55501D
A88R520	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A88R524	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A88R526	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A88R528	321-0414-03			RES.,FXD,FILM:200K OHM,0.25%,0.125W	24546	NC55C2003C
A88R532	301-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.50W	01121	EB1015
A88R534	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A88R536	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A88R538	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A88R612	315-0135-00			RES.,FXD,CMPSN:1.3M OHM,5%,0.25W	01121	CB1355
A88R613	321-0402-00			RES.,FXD,FILM:150K OHM,1%,0.125W	24546	NA55D1503F
A88R614	321-0756-00			RES.,FXD,FILM:50K OHM,1%,0.125W	24546	NA55D5002F
A88R616	321-0452-00			RES.,FXD,FILM:499K OHM,1%,0.125W	91637	MFF1816G49902F
A88R617	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A88R618	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A88R620	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A88R622	321-0373-04			RES.,FXD,FILM:75K OHM,0.1%,0.125W	91637	MFF1816D75001B
A88TP328	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A88U100	156-0158-04			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	01295	N99320JG
A88U216	156-0158-04			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	01295	N99320JG
A88U224	156-0158-04			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	01295	N99320JG
A88U234	156-0158-04			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	01295	N99320JG
A88U244	156-0158-04			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	01295	N99320JG
A88U510	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A88VR250	152-0283-00			SEMICOND DEVICE:ZENER,0.4W,43V,5%	12954	DZ750903B1N976B
A88VR256	152-0486-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	80009	152-0486-00
A88VR302	152-0283-00			SEMICOND DEVICE:ZENER,0.4W,43V,5%	12954	DZ750903B1N976B
A88VR316	152-0281-00			SEMICOND DEVICE:ZENER,0.4W,22V,5%	12954	1N969B

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A88VR324	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
A88VR344	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
A88VR348	152-0281-00			SEMICOND DEVICE:ZENER,0.4W,22V,5%	12954	1N969B
A88VR504	152-0514-00			SEMICOND DEVICE:ZENER,0.4W,10V,1%	80009	152-0514-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B5020	119-1188-00			FAN,TUBEAXIAL:90V,3100 RPM,115 CFM	82877	MX70A3028648
C533	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
C534	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	56289	273C11
C5001	285-1184-00	B010100	B029999	CAP.,FXD,MTLZD:0.01 UF,20%,4000V	84411	TEK-183103040
C5009	283-0189-00			CAP.,FXD,CER DI:0.1UF,20%,400V	56289	5C40X5R104M400B
C5010	283-0189-00			CAP.,FXD,CER DI:0.1UF,20%,400V	56289	5C40X5R104M400B
CR002	152-0141-02	B030000		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
CR231	152-0721-00			SEMICOND DEVICE:RECT,SI,100V,12A,FAST REC	25403	BYW30-100U
CR321	152-0642-00			SEMICOND DEVICE:RECT,SI,35V,40A,DO-5	01281	SD5218
CR331	152-0721-00			SEMICOND DEVICE:RECT,SI,100V,12A,FAST REC	25403	BYW30-100U
CR531	152-0642-00			SEMICOND DEVICE:RECT,SI,35V,40A,DO-5	01281	SD5218
CR631	152-0642-00			SEMICOND DEVICE:RECT,SI,35V,40A,DO-5	01281	SD5218
CR5001	152-0408-00	B010100	B029999	SEMICOND DEVICE:SILICON,10KV,5MA	83003	H345
DS5114	150-1014-00			LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
DS5115	150-1014-00			LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
E5009	119-0429-00			SURGE VOLTAGE P:145V,GAS FILLED	80009	119-0429-00
E5010	119-0429-00			SURGE VOLTAGE P:145V,GAS FILLED	80009	119-0429-00
F5020	159-0165-00			FUSE,CARTRIDGE:1A,125V,0.4 SEC,0.17 LEADS	75915	273001
FL5020	119-1298-00			FILTER,RFI:10A,250V,50-400HZ	23880	F14317-10
J13	131-0346-01			CONN,RCPT,ELEC:24 CONTACT,FEMALE	71785	222-22-24-242
Q002	151-0678-01			TRANSISTOR:SI,MJE13005,TO-220	80009	151-0678-01
Q211	151-0477-00			TRANSISTOR:SILICON,NPN	04713	SJE374
Q421	151-0603-00			TRANSISTOR:SILICON,NPN	02735	68303
Q511	151-0482-00			TRANSISTOR:SILICON,PNP	80009	151-0482-00
R111	308-0818-00			RES.,FXD,WW:0.005 OHM,3%,10W	91637	RH10-89/.005 3%
R533	303-0100-00			RES.,FXD,CMPSN:10 OHM,5%,1W	01121	GB1005
R534	303-0100-00			RES.,FXD,CMPSN:10 OHM,5%,1W	01121	GB1005
R5001	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R5002	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R5003	325-0082-03	B010100	B029999	RES.,FXD,FILM:33.51M OHM,0.25%,1W	91637	HFF1-D33514C
R5003	325-0332-00	B030000		RES.,FXD,FILM:9M OHM,1%,1.25W,4000V	19647	MG7169M
R5004	325-0332-00	B030000		RES.,FXD,FILM:9M OHM,1%,1.25W,4000V	19647	MG7169M
R5005	325-0081-00	B010100	B029999	RES.,FXD,FILM:11.17M OHM,0.1%,0.5W	03888	PME70-C11174B
R5005	325-0073-00	B030000		RES.,FXD,FILM:3.57M OHM,1%,0.50W	03888	PME70-G35703F
R5006	311-1698-00	B010100	B029999	RES.,VAR,NONWIR:PNL,10M OHM,2W	12697	380-CM40396
R5006	311-0397-01	B030000		RES.,VAR,NONWIR:2M OHM,10%,0.50W	71590	BA147-044UV3
R5007	311-1698-00	B010100	B029999	RES.,VAR,NONWIR:PNL,10M OHM,2W	12697	380-CM40396
R5007	311-0397-01	B030000		RES.,VAR,NONWIR:2M OHM,10%,0.50W	71590	BA147-044UV3
R5008	325-0073-00	B030000		RES.,FXD,FILM:3.57M OHM,1%,0.50W	03888	PME70-G35703F
R5009	307-0024-00			RES.,FXD,CMPSN:2.7 OHM,10%,0.50W	01121	EB27G1
R5010	307-0024-00			RES.,FXD,CMPSN:2.7 OHM,10%,0.50W	01121	EB27G1
R5011	325-0081-00	B030000		RES.,FXD,FILM:11.17M OHM,0.1%,0.5W	03888	PME70-C11174B
R5012	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R5013	325-0081-00	B030000		RES.,FXD,FILM:11.17M OHM,0.1%,0.5W	03888	PME70-C11174B
R5014	325-0073-00	B030000		RES.,FXD,FILM:3.57M OHM,1%,0.50W	03888	PME70-G35703F
R5015	325-0073-00	B030000		RES.,FXD,FILM:3.57M OHM,1%,0.50W	03888	PME70-G35703F
S5020	260-1198-00			SWITCH,TOGGLE:DPST,15A,125VAC	27193	OBD
S5021	260-1967-00			SWITCH,SLIDE:DPDT,5A/250V	000FJ	4021.0512
S5022	260-0638-00			SW,THERMOSTATIC:10A,240V,OPEN 75 DEG C	93410	430-364

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
T5020	120-1288-00			TRANSFORMER,RF:COMMON MODE	80009	120-1288-00
U5015	307-0292-22			RES.,FXD,FILM:2,160 OHM	80009	307-0292-22
U5040	307-0292-22			RES.,FXD,FILM:2,160 OHM	80009	307-0292-22
U5559	156-0872-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC7912C
V5201	154-0784-00			ELECTRON TUBE:CRT,T7610	80009	154-0784-00
V5202	154-0784-00			ELECTRON TUBE:CRT,T7610	80009	154-0784-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it goes to the low state.

Abbreviations are based on ANSI Y1.1-1972.

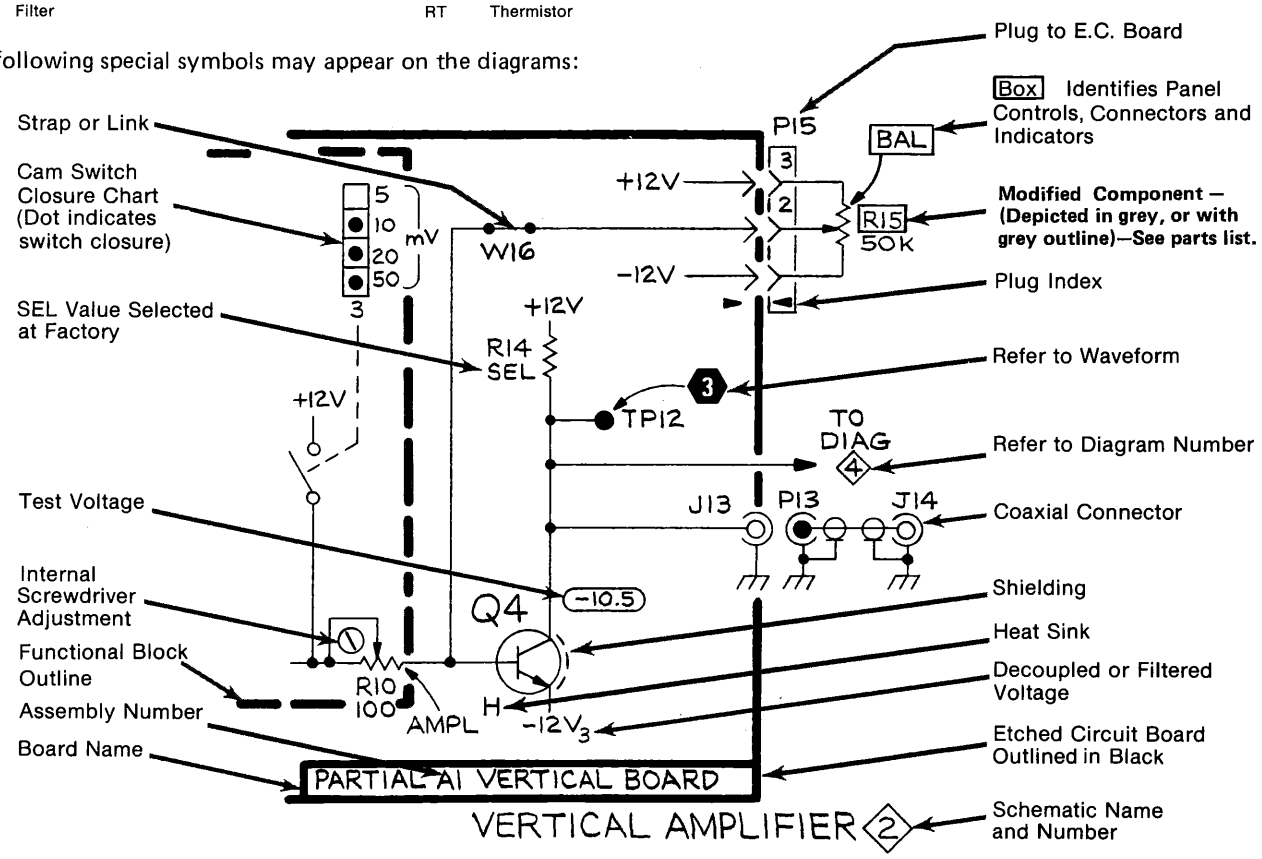
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

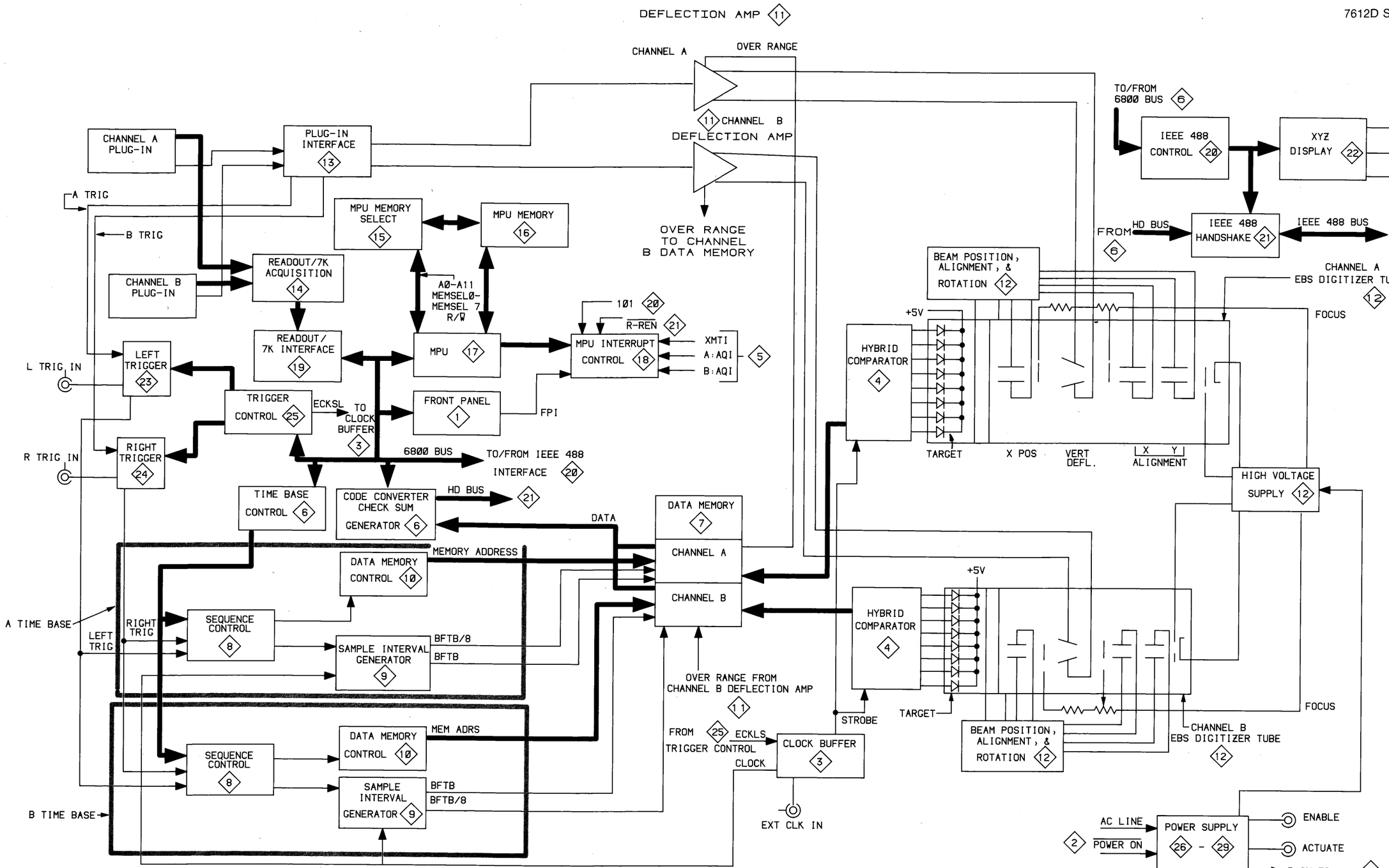
Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)	H	Heat dissipating device (heat sink, heat radiator, etc)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:





NOTE:

HEAVY LINES DENOTE BUSES

FIG. 8-1. 7612D BLOCK DIAGRAM

2387-801

P/O A10 ASSY							FRONT PANEL DISPLAY ◇1	
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C858	A6	J5*	R302	D1	D0	U226A	D3	C2
C954	B6	K5	R302	D2	D0	U226F	D1	C2
DS006	E2	A0	R303	D2	D0	U328A	D2	C2
DS008	F2	A0	R304	D1	D0	U328B	D1	C2
DS102	G2	B0	R306	D1	D0	U328C	D1	C2
DS106	G2	B0	R308	D1	D1	U328D	D1	C2
DS204	H2	C0	R436B	B2	E4*	U328E	D1	C2
DS306	F3	D0	R436C	B3	E4	U328F	D2	C2
DS308	F3	D0	R436D	B3	E4	U338	D1	D3
DS402	G3	E0	R436E	B4	E4	U358	B3	D5
DS406	H3	E0	R436G	B4	E4	U424	D3	E2
DS506	F4	F0	R436H	B4	E4	U426A	D3	E2
DS508	F4	F1	R436J	B4	E4	U426B	D4	E2
DS524	F6	F2	R510	D3	F1	U426C	D4	E2
DS526	G6	F2	R511	D3	F1	U426D	D4	E2
DS602	F4	G0	R512	D4	F1	U426E	D4	E2
DS606	G4	G0	R514	D4	F1	U426F	D3	E2
DS620	G6	G2	R516	D4	F1	U436	B2	E3
DS702	H4	H0	R520	D4	F1	U452	B4	E5
DS704	H4	H0	R528	D4	F1	U624A	D4	G2
DS804	F5	J0	R700	D5	H0	U624F	D5	G2
DS808	F5	J0	R702	D5	H0	U724	D5	H2
DS902	G5	K0	R703	D5	H0	U726A	D5	H2
DS906	H5	K0	R704	D6	H0	U726B	D5	H2
P550	A2	G4*	R706	D5	H0	U726B	D5	H2
P552	A1	G5	R708	D5	H1	U726C	D5	H2
P554	A1	F4*	R710	D5	H1	U726D	D5	H2
P554	A2	F4	R820	C5	J2	U726E	D5	H2
P554	A4	F4	R821	C5	J2	U726F	D6	H2
P554	C6	F4	R823	C5	J2	U746A	B1	H4
P556	A3	F5	R824	C5	J2	U746B	B1	H4
Q716	C5	H1*	R826	C6	J2	U746C	C1	H4
Q718	C5	H1*	R828	C5	J2	U746F	B2	H4
Q914	C5	J1*	R828	C5	J2	U756B	B2	H5
Q916	C5	J1*	R828	C5	J2	U756C	B6	H5
Q918	C5	J1*	R856	A6	J5	U756D	B6	H5
Q926	C6	K2*	R858	A6	J5	U838	C5	J3
R010	D2	A1	TP944	B6	K4*	U838A	C5	J3
R012	D2	A1	U114A	D2	B1	U838B	C5	J3
R014	D2	A1	U114B	D2	B1	U838C	C5	J3
R016	D3	A1	U114C	D3	B1	U838D	C6	J3
R018	D3	A1	U114D	D3	B1	U838F	C5	J3
R019	D3	A1	U114E	D3	B1	U848	B5	J4
R020	D3	A2	U114F	D2	B1	U858	B6	J5
R300	D1	D0	U210	D2	C1			

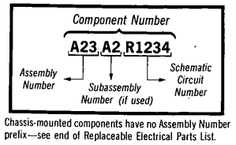
P/O A10 ASSY ALSO SHOWN ON ◇2

P/O A68 ASSY							FRONT PANEL DISPLAY ◇1	
P550	A2	G5	P554	A4	G5			
P552	A1	G5	P554	C6	G5			
P554	A1	G5	P556	A3	G5			
P554	A2	G5						

A68 ASSY SHOWN IN FIG. 8-31

* Back of Board

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

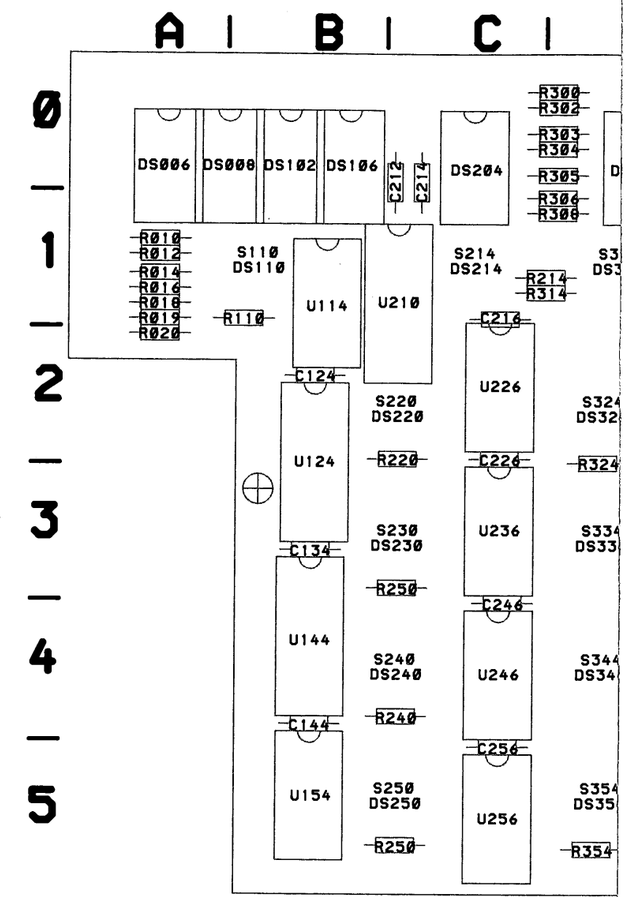


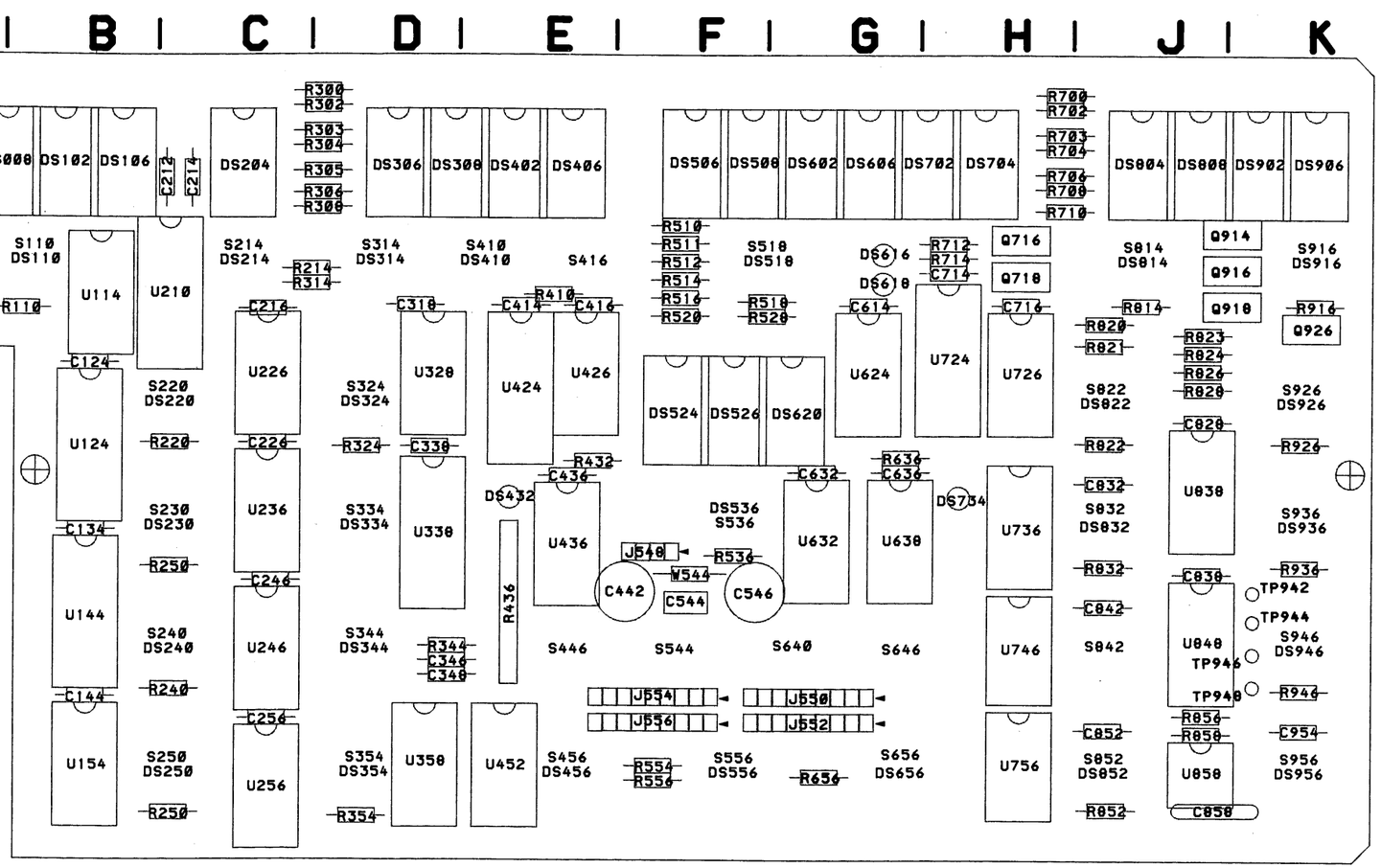
Fig. 8-2.

NEL DISPLAY (1)

hematic ocation	Board Location
D3	C2
D1	C2
D2	C2
D1	C2
D1	C2
D1	C2
D1	C2
D2	C2
D1	D3
B3	D5
D3	E2
D3	E2
D4	E2
D4	E2
D4	E2
D4	E2
D3	E2
B2	E3
B4	E5
D4	G2
D5	G2
D5	H2
D5	H2
D5	H2
D5	H2
D5	H2
D5	H2
D5	H2
D5	H2
D6	H2
B1	H4
B1	H4
C1	H4
B2	H4
B2	H5
B6	H5
B6	H5
C5	J3
C5	J3
C5	J3
C5	J3
C6	J3
C5	J3
B5	J4
B6	J5

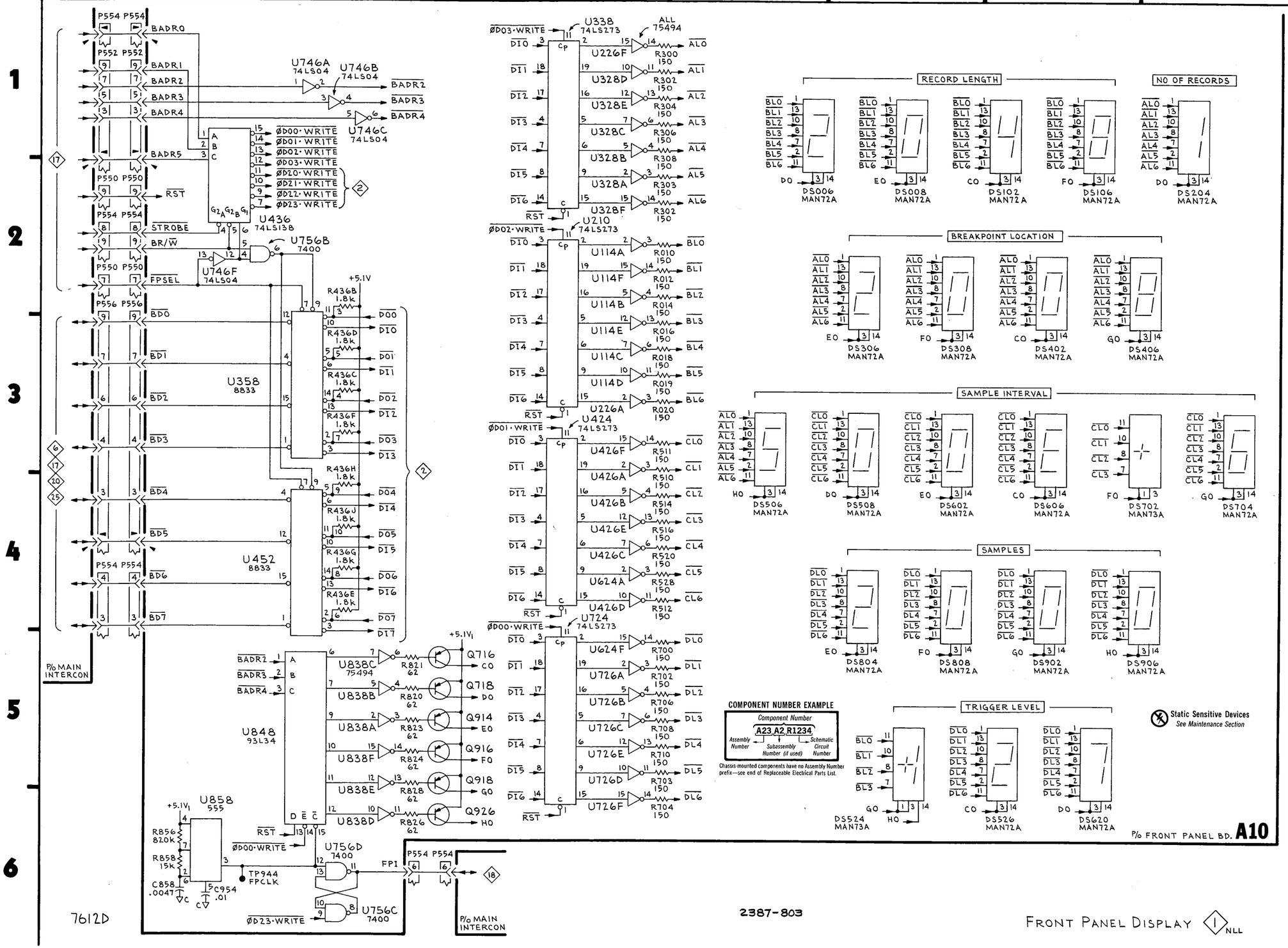
EL DISPLAY (1)

* Back of Board

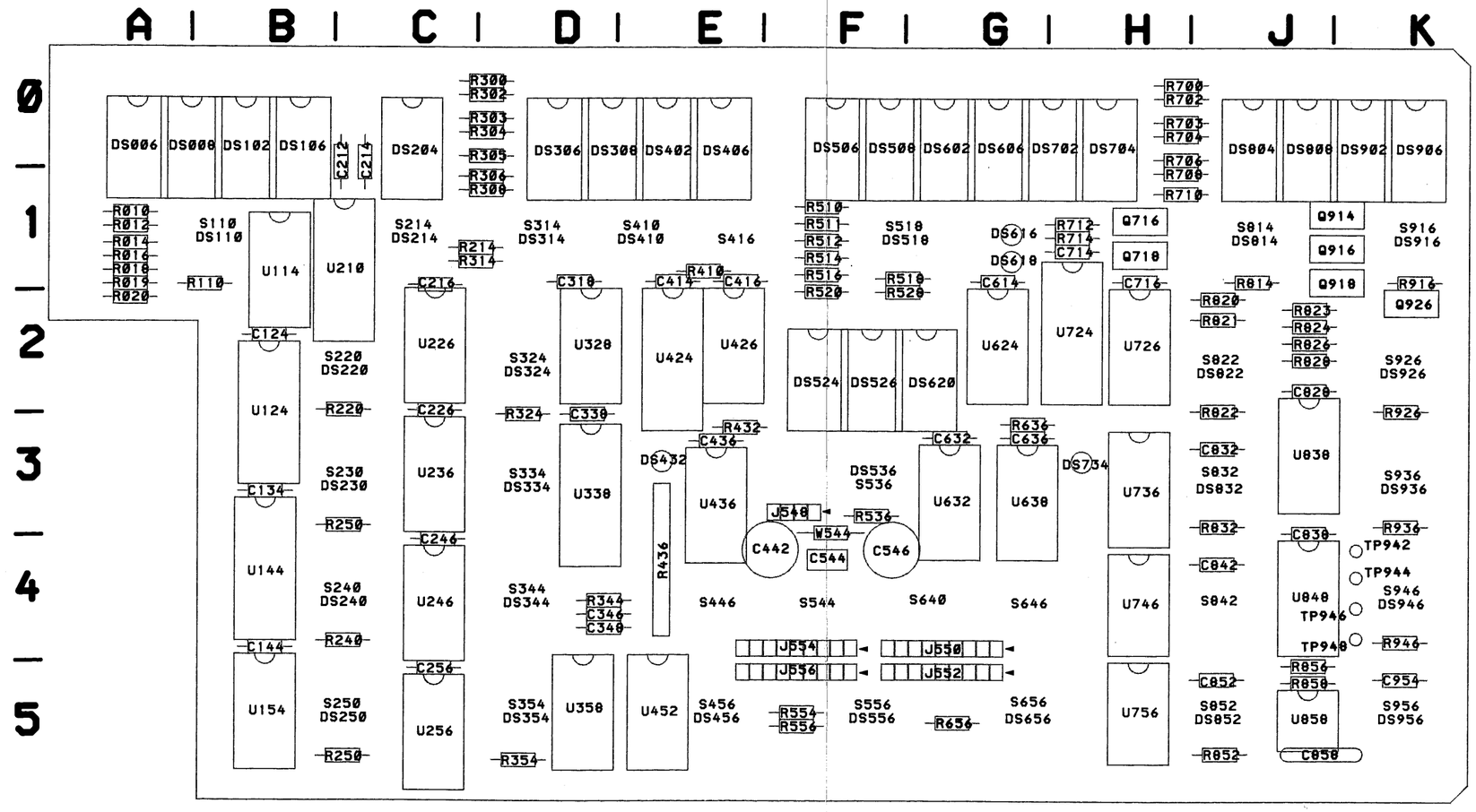


2387-802

Fig. 8-2. Front Panel circuit board, assembly A10.


A
B
C
D
E
F
G
H
1
2
3
4
5
6
P554 P554
BADR0
P552 P552
BADR1
BADR2
BADR3
BADR4
BADR5
P550 P550
RST
P554 P554
STROBE
BR/W
P550 P550
FPSEL
P556 P556
BD0
BD1
BD2
BD3
BD4
BD5
P554 P554
BD6
BD7
U746A 74LS04
U746B 74LS04
U746C 74LS04
U746F 74LS04
U436 74LS138
U756B 7400
U358 8833
U452 8833
+5.1V
R436B 1.8k
R436D 1.8k
R436C 1.8k
R436F 1.8k
R436H 1.8k
R436J 1.8k
R436G 1.8k
R436E 1.8k
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
ØD00·WRITE
ØD01·WRITE
ØD02·WRITE
ØD03·WRITE
ØD20·WRITE
ØD21·WRITE
ØD22·WRITE
ØD23·WRITE
P/O MAIN INTERCON
U848 93L34
U838C 75494
U838B
U838A
U838F
U838E
U838D
R821 62
R820 62
R823 62
R824 62
R828 62
R826 62
Q716
CO
Q718
DO
Q914
EO
Q916
FO
Q918
GO
Q926
HO
U858 555
R856 820K
R858 15K
C858 .004T
C954 .01
TP944 FPCLK
U756D 7400
U756C 7400
FPI
P554 P554
P/O MAIN INTERCON
U338 74LS273
U226F
U328D
U328E
U328C
U328B
U328A
U328F
ALL 75494
R300 150
R302 150
R304 150
R306 150
R308 150
R303 150
R302 150
AL0
AL1
AL2
AL3
AL4
AL5
AL6
U210 74LS273
U114A
U114F
U114B
U114E
U114C
U114D
U226A
R010 150
R012 150
R014 150
R016 150
R018 150
R019 150
R020 150
BL0
BL1
BL2
BL3
BL4
BL5
BL6
U424 74LS273
U426F
U426A
U426B
U426E
U426C
U624A
U426D
R511 150
R510 150
R514 150
R516 150
R520 150
R528 150
R512 150
CL0
CL1
CL2
CL3
CL4
CL5
CL6
U724 74LS273
U624F
U726A
U726B
U726C
U726E
U726D
U726F
R700 150
R702 150
R706 150
R708 150
R710 150
R703 150
R704 150
DL0
DL1
DL2
DL3
DL4
DL5
DL6
RECORD LENGTH
NO OF RECORDS
DS006 MAN72A
DS008 MAN72A
DS102 MAN72A
DS106 MAN72A
DS204 MAN72A
BREAKPOINT LOCATION
DS306 MAN72A
DS308 MAN72A
DS402 MAN72A
DS406 MAN72A
SAMPLE INTERVAL
DS506 MAN72A
DS508 MAN72A
DS602 MAN72A
DS606 MAN72A
DS702 MAN73A
DS704 MAN72A
SAMPLES
DS804 MAN72A
DS808 MAN72A
DS902 MAN72A
DS906 MAN72A
TRIGGER LEVEL
DS524 MAN73A
DS526 MAN72A
DS620 MAN72A
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
P/O FRONT PANEL BD. A10
7612D
2387-803
FRONT PANEL DISPLAY 1 NLL
FRONT PANEL DISPLAY 7

FRONT PANEL A10



2387-802

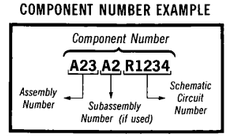
Fig. 8-3. Front Panel circuit board, assembly A10.

P/O A10 ASS
Circuit Number
C124
C134
C144
C212
C214
C216
C226
C246
C256
C318
C338
C346
C348
C414
C416
C436
C442
C544
C546
C614
C632
C636
C714
C716
C828
C832
C838
C852
C858
DS110
DS214
DS220
DS230
DS240
DS250
DS314
DS324
DS344
DS354
DS410
DS432
DS456
DS518
DS536
DS556
DS616
DS618
DS656
DS734
DS814
DS822
DS832
DS852
DS916
DS926

P/O A68 ASS
P548
P548
P550
P550

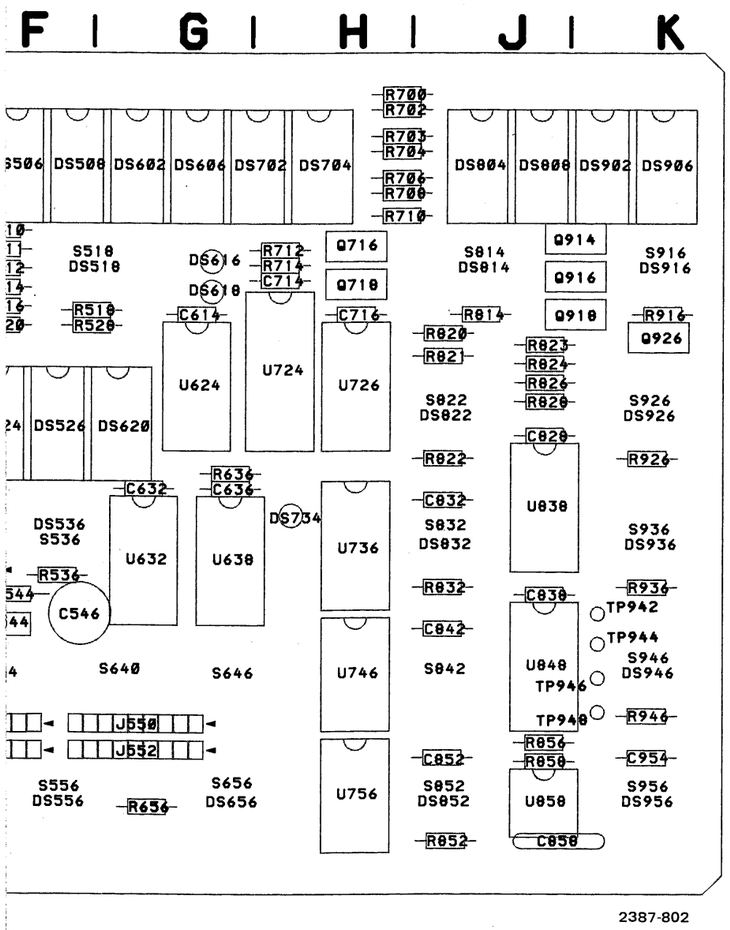
* Back of Board

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



2387-802

10.

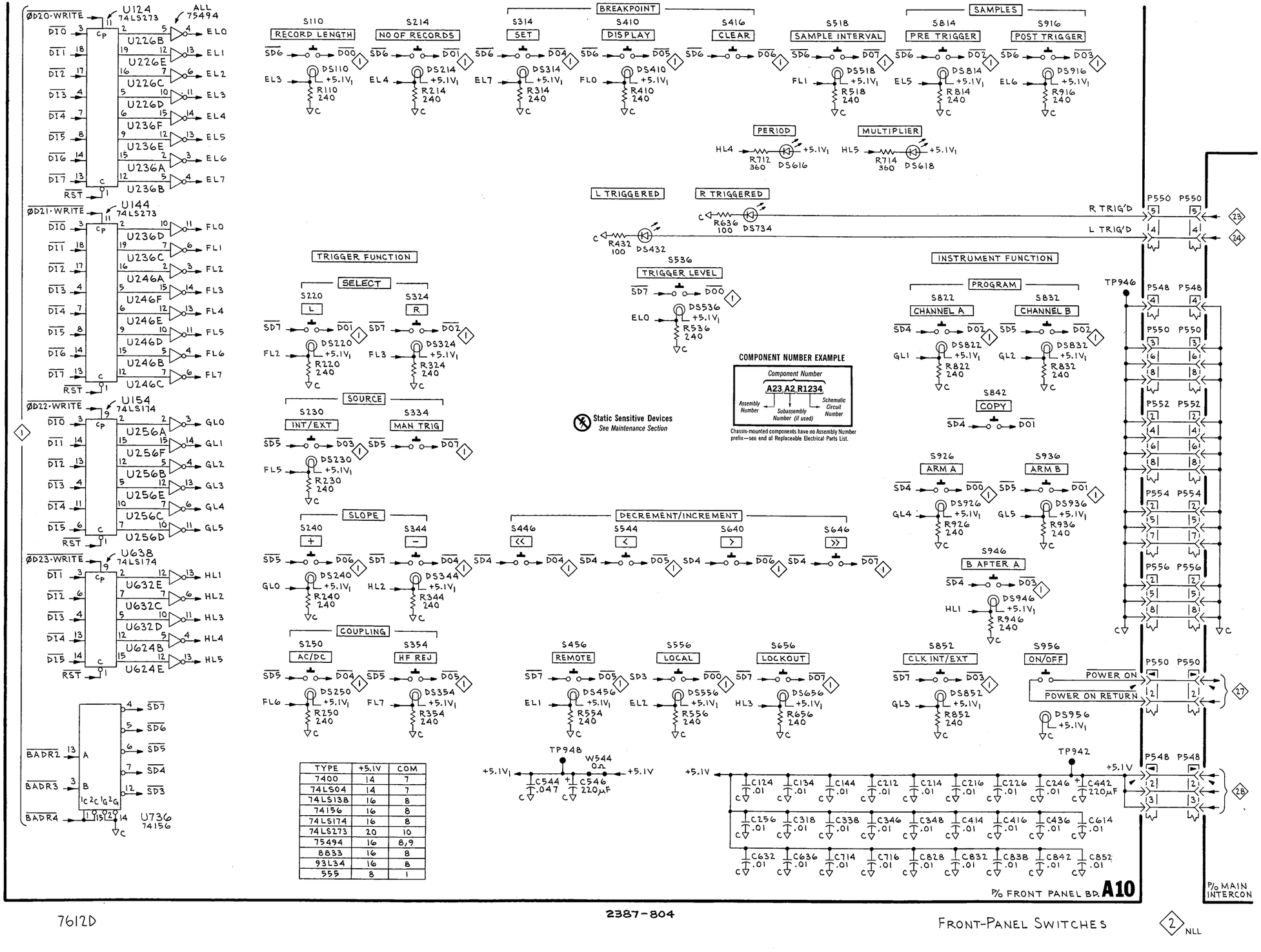
P/O A10 ASSY						FRONT PANEL SWITCHES ◇2		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C124	E6	B2	DS936	G4	K3	S536	E2	F3
C134	F6	B3	DS946	G4	K4	S544	D4	F4
C144	F6	B4	DS956	G5	K5	S556	E5	F5
C212	F6	C0	P548	H2	F3	S640	E4	G4
C214	F6	C0	P548	H5	F3*	S646	F4	G4
C216	G6	C1	P550	H2	G4	S656	E5	G5
C226	G6	C3	P550	H3	G4	S814	G1	J1
C246	G6	C4	P550	H5	G4	S822	F3	J2
C256	E6	C5	P552	H3	G5	S832	G3	J3
C318	F6	D1	P554	H4	F4	S842	G3	J4
C338	F6	D3	P556	H4	F5*	S852	F5	H5
C346	F6	D4	R110	B1	B1	S916	G1	K1
C348	F6	D3	R214	C1	C1	S926	F4	K2
C414	G6	E1	R220	B3	C2	S936	G4	K3
C416	G6	E1	R230	B4	C3	S946	G4	K4
C436	G6	E3	R240	B4	B2	S956	G5	K5
C442	G6	F4*	R250	B5	C5	TP942	G5	K4*
C544	D6	F4*	R314	D1	C1	TP946	H2	K4
C546	D6	F4*	R324	C3	D3	TP948	D5	K4*
C614	G6	G1	R344	C4	D4	U124	A1	B2
C632	E6	G3	R354	C5	D5	U144	A2	B4
C636	F6	G3	R410	D1	E1	U154	A3	B5
C714	F6	H1	R432	D2	E3	U226	B1	C2
C716	F6	H1	R518	F1	F1	U226C	B1	C2
C828	F6	J2	R536	E3	F3	U226D	B1	C2
C832	G6	J3	R554	D5	F5	U226E	B1	C2
C838	G6	J4	R556	E5	F5	U236A	B2	C3
C852	G6	J5	R636	E2	G3	U236B	B2	C3
C858	G6	J5	R656	E5	G5	U236C	B2	C3
DS110	C1	B1	R712	E2	H1	U236D	B2	C3
DS214	C1	C1	R714	F2	H1	U236E	B1	C3
DS220	B3	C2	R814	F1	J1	U236F	B1	C3
DS230	B3	C2	R822	F3	J3	U246A	B2	C4
DS240	B4	B2	R832	G3	J3	U246B	B3	C4
DS250	B5	C5	R852	F5	H5	U246C	B3	C4
DS314	D1	D1	R916	G1	K1	U246C	B3	C4
DS324	C3	D2	R926	F4	K2	U246D	B3	C4
DS344	C4	D4	R936	G4	K3	U246E	B3	C4
DS354	C5	D5	R946	G4	K4	U246F	B2	C4
DS410	D1	E1	S110	B1	B1	U256	B4	C5
DS432	E2	E3	S214	C1	C1	U256A	B3	C5
DS456	D5	E5	S220	C3	C2	U256A	B3	C5
DS518	F1	F1	S230	B3	C2	U256B	B3	C5
DS536	E3	F3	S240	B4	B2	U256C	B4	C5
DS556	E5	F5	S250	B5	C5	U256D	B4	C5
DS616	E2	G1	S314	D1	D1	U256F	B3	C5
DS618	F2	G1	S324	C3	D2	U624B	B5	G2
DS656	E5	G5	S334	C3	D3	U624E	B5	G2
DS734	E2	H3	S344	C4	D4	U632C	B4	G3
DS814	F1	J1	S354	C5	D5	U632D	B4	G3
DS822	F3	J2	S410	D1	E1	U632E	B4	G3
DS832	G3	J3	S416	E1	E1	U638	A4	G3
DS852	F5	H5	S446	D4	E4	U736	A6	H3
DS916	G1	K1	S456	D5	E5	W544	D5	F3
DS926	F4	K3	S518	F1	F1			

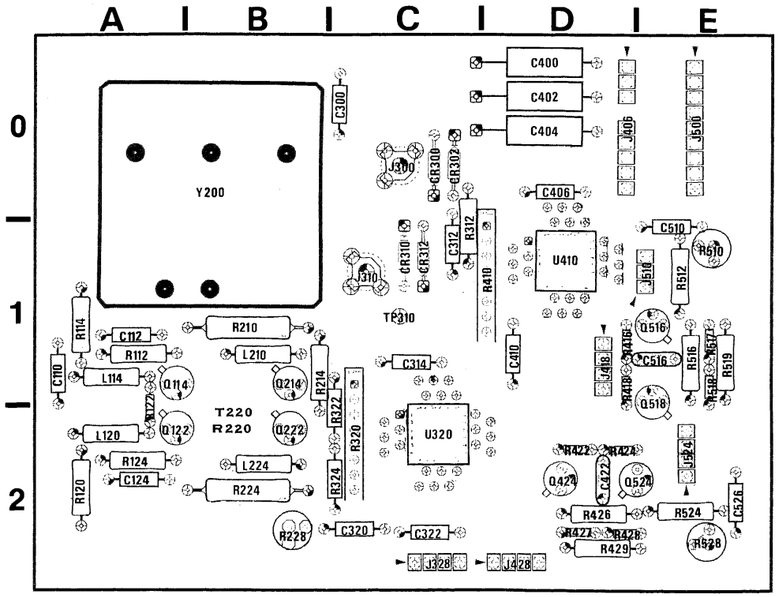
P/O A10 ASSY ALSO SHOWN ON ◇1

P/O A68 ASSY						FRONT PANEL SWITCHES ◇2		
P548	H2	G4	P550	H5	G4			
P548	H5	G4	P552	H3	G5			
P550	H2	G5	P554	H4	G5			
P550	H3	G5	P556	H4	G5			

A68 ASSY SHOWN IN FIG. 8-31

* Back of Board


ØD20·WRITE
U124 74LS273
ALL 75494
DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7
U226B U226E U226C U226D U236F U236E U236A U236B
EL0 EL1 EL2 EL3 EL4 EL5 EL6 EL7
RST
ØD21·WRITE
U144 74LS273
U236D U236C U246A U246F U246E U246D U246B U246C
FL0 FL1 FL2 FL3 FL4 FL5 FL6 FL7
ØD22·WRITE
U154 74LS174
U256A U256F U256B U256E U256C U256D
GL0 GL1 GL2 GL3 GL4 GL5
ØD23·WRITE
U638 74LS174
U632E U632C U632D U624B U624E
HL1 HL2 HL3 HL4 HL5
BADR2 BADR3 BADR4
U736 74156
SD7 SD6 SD5 SD4 SD3
BREAKPOINT
S110 RECORD LENGTH
S214 NO OF RECORDS
S314 SET
S410 DISPLAY
S416 CLEAR
DS110 DS214 DS314 DS410
R110 R214 R314 R410 240
SAMPLES
S518 SAMPLE INTERVAL
S814 PRE TRIGGER
S916 POST TRIGGER
DS518 DS814 DS916
R518 R814 R916 240
PERIOD
MULTIPLIER
HL4 R712 360 DS616
HL5 R714 360 DS618
L TRIGGERED
R TRIGGERED
R432 100 DS432
R636 100 DS734
R TRIG'D
L TRIG'D
P550 P550
TRIGGER FUNCTION
SELECT
S220 L
S324 R
DS220 DS324
R220 R324 240
SOURCE
S230 INT/EXT
S334 MAN TRIG
DS230
R230 240
S536 TRIGGER LEVEL
DS536
R536 240
INSTRUMENT FUNCTION
PROGRAM
S822 CHANNEL A
S832 CHANNEL B
DS822 DS832
R822 R832 240
S842 COPY
S926 ARM A
S936 ARM B
DS926 DS936
R926 R936 240
S946 B AFTER A
DS946
R946 240
TP946
P548 P548
P550 P550
P552 P552
P554 P554
P556 P556
SLOPE
S240 +
S344 −
DS240 DS344
R240 R344 240
DECREMENT/INCREMENT
S446 <<
S544 <
S640 >
S646 >>
COUPLING
S250 AC/DC
S354 HF REJ
DS250 DS354
R250 R354 240
S456 REMOTE
S556 LOCAL
S656 LOCKOUT
DS456 DS556 DS656
R554 R556 R656 240
S852 CLK INT/EXT
S956 ON/OFF
DS852 DS956
R852 240
POWER ON
POWER ON RETURN
TP948
W544 0Ω
C544 .047
C546 220µF
TP942
C442 220µF
C124 C134 C144 C212 C214 C216 C226 C246
C256 C318 C338 C346 C348 C414 C416 C436 C614
C632 C636 C714 C716 C828 C832 C838 C842 C852
.01
+5.1V
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
TYPE +5.1V COM
7400 14 7
74LS04 14 7
74LS138 16 8
74156 16 8
74LS174 16 8
74LS273 20 10
75494 16 8,9
8833 16 8
93L34 16 8
555 8 1
P/O FRONT PANEL BD. A10
P/O MAIN INTERCON
FRONT PANEL SWITCHES
2387-804
FRONT-PANEL SWITCHES
NLL



2387-805

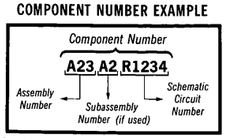
Fig 8-4. Clock Buffer circuit board, assembly A12.

P/O A12 ASSY				CLOCK BUFFER ◇3	
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C110	B4	A1			
C112	B4	A1	R120	C2	A2
C124	B3	A2	R122	C2	A2
C300	B2	C0	R124	B2	A2
C312	B4	C1	R210	D2	B1
C314	B4	C1	R212 *	D2	B1
C320	C4	C2	R214	D2	B1
C322	E2	C2	R220	D2	B2
C400	B4	D0	R222 *	D3	B2
C402	B4	D0	R224	D2	B2
C404	B3	D0	R228	E2	B2
C406	C4	D0	R312	B1	C1
C410	C4	D1	R320	B2	C2
C422	G4	D2	R320	E4	C2
C510	B4	E1	R322	D2	C2
C516	G3	E1	R324	D3	C2
C526	B4	E2	R410	D1	D1
CR220 *	C2	B2	R410	E2	D1
CR222 *	C2	B2	R410	E2	D1
CR300	C1	C0	R416	G3	D1
CR302	C1	C0	R418	G3	D1
CR310	G1	C1	R422	G4	D2
CR312	G2	C1	R424	G5	D2
L114	C2	A1	R426	G4	D2
L120	C3	B1	R427	F4	D2
L210	D2	B1	R428	F5	D2
L224	D3	B2	R429	G4	D2
P300	A1	C0	R510	G3	F1
P310	H1	C1	R512	G3	E1
P328	H3	C2	R516	G3	E1
P406	A2	D0	R517	F3	E1
P406	A5	D0	R518	F2	E1
P418	H2	D1	R519	G3	E1
P428	H2	D2	R524	G4	E2
P500	A2	E0	R528	G4	E2
P500	A3	E1	TP310	A5	C1
P510	E5	E1	U320A	D1	C2
P524	H4	E2	U320B	E2	C2
Q114	C2	A1	U320C	F4	C2
Q122	C3	A2	U320D	F4	C2
Q214	D2	B1	U320E	E4	C2
Q222	D3	B2	U410A	E1	D1
Q424	G4	D2	U410B	E1	D1
Q516	G3	E1	U410C	F3	D1
Q518	G2	E1	U410D	F2	D1
Q524	G5	E2	U410E	E2	D1
R112	B2	A1	Y200	B2	B0
R114	C2	A1			

P/O A68 ASSY				CLOCK BUFFER ◇3	
P546	A2	G4	P546	A3	G4
A68 ASSY SHOWN IN FIG. 8-31					

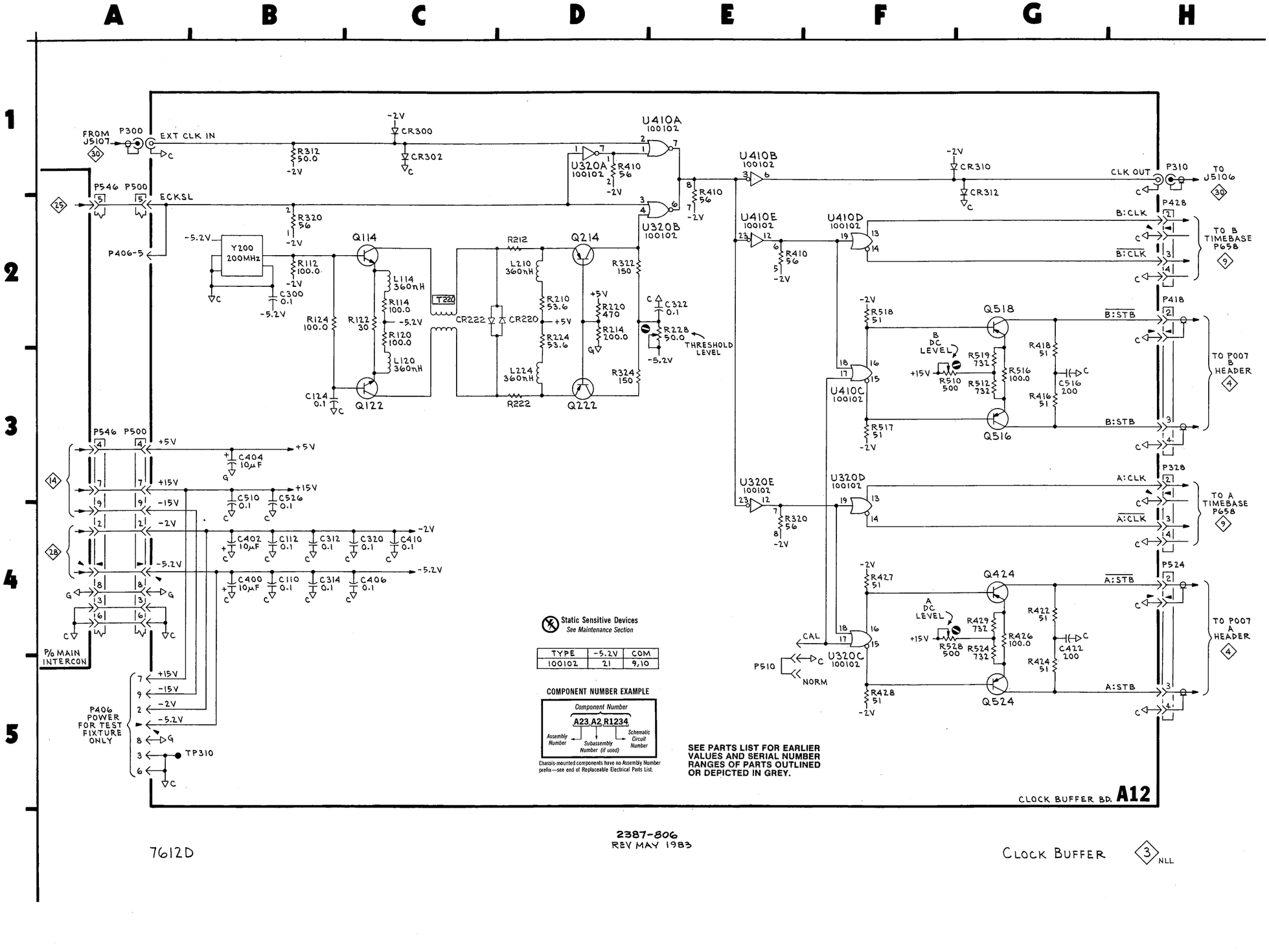
*See Parts List for serial number ranges.

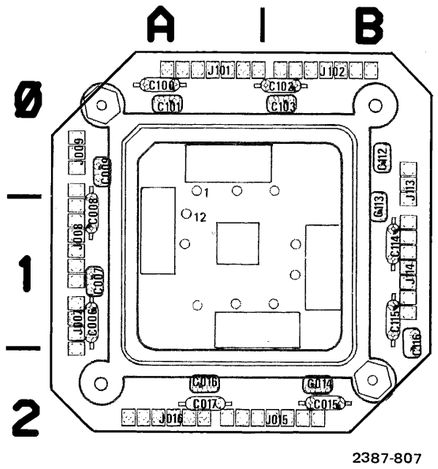
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section


A B C D E F G H
1 2 3 4 5
FROM J5107 30
P300
EXT CLK IN
R312 50.0
-2V
CR300
CR302
U410A 100102
U320A 100102
R410 56
U320B 100102
U410B 100102
CR310
CR312
CLK OUT
P310
TO J5106 30
P546 P500
25
ECKSL
P406-5
R320 56
Y200 200MHz
R112 100.0
C300 0.1
-5.2V
Q114
Q122
L114 360nH
R114 100.0
R120 100.0
L120 360nH
R124 100.0
R123 30
C124 0.1
T220
CR222
CR220
R212
L210 360nH
R210 53.6
R224 53.6
L224 360nH
R222
Q214
Q222
R322 150
R324 150
R220 470
R214 200.0
C322 0.1
R228 50.0
THRESHOLD LEVEL
+5V
U410E 100102
U410D 100102
P428
B:CLK
B:CLK
TO B TIMEBASE P658 9
P418
B:STB
TO P007 B HEADER 4
Q518
Q516
B DC LEVEL
R519 732
R512 732
R510 500
R516 100.0
R518 51
R517 51
R418 51
R416 51
C516 200
U410C 100102
P546 P500
+5V
C404 10µF
+15V
C510 0.1
C526 0.1
-15V
-2V
C402 10µF
C112 0.1
C312 0.1
C320 0.1
C410 0.1
C400 10µF
C110 0.1
C314 0.1
C406 0.1
14
28
P/O MAIN INTERCON
P406 POWER FOR TEST FIXTURE ONLY
TP310
U320E 100102
U320D 100102
P328
A:CLK
A:CLK
TO A TIMEBASE P658 9
P524
A:STB
A:STB
TO P007 A HEADER 4
Q424
Q524
A DC LEVEL
R429 732
R426 100.0
R524 732
R528 500
R422 51
R414 51
C422 200
R427 51
R428 51
U320C 100102
CAL
P510
NORM
Static Sensitive Devices
See Maintenance Section
TYPE | -5.2V | COM
100102 | 21 | 9,10
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2,R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
CLOCK BUFFER BD. A12

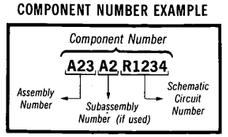


2387-807

Fig. 8-5. Header circuit board assembly A14.

HEADER A14

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A14 ASSY					HEADER ◇4
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C006	E2	A1	P016	B3	A2
C007	D3	A1	P016	B5	A2
C008	G2	A1	P016	D3	A2
C009	D3	A0	P016	D5	A2
C014	D5	B2	P016	E2	A2
C015	E2	B2	P016	G2	A2
C016	D5	A2	P016	H1	A2
C017	G2	A2	P016	H1	A2
C100	E2	A0	P101	A4	A0
C101	D4	A0	P101	H3	A0
C102	G2	B0	P102	B3	B0
C103	D4	B0	P102	B4	B0
C112	D6	B0	P102	B6	B0
C113	D6	B1	P102	D3	B0
C114	H2	B1	P102	D4	B0
C115	E2	B1	P102	D6	B0
C116	D6	B2	P102	F2	B0
P007	A2	A1	P102	G2	B0
P007	H2	A1	P102	H1	B0
P008	A3	A1	P102	H1	B0
P008	H3	A1	P113	B5	B0
P009	B3	A0	P113	D6	B0
P009	D3	A0	P113	F2	B0
P009	F2	A0	P113	H1	B0
P009	H1	A0	P114	A5	B1
P015	A4	A1	P114	H4	B1
P015	H4	B2			

P/O A26 ASSY					HEADER ◇4
C322	D1	D2	R112	C5	B1
C324	C1	D2	R114	C6	B1
C326	C1	D2	R116	C4	B2
CR316	C1	D1	R122	C5	B2
CR322	D1	D2	R123	C6	B2
CR330	C1	D2	R124	C6	B2
CR332	D1	D3	R126	C4	B2
P010	B3	A1	R212	C3	C2
P010	B4	A1	R214	C4	C2
P010	B6	A1	R216	C3	C2
P010	G1	A1	R218	C3	D2
P010	G1	A1	R222	C3	C2
P012	B3	A1	R224	C4	C2
P012	B6	A1	R226	C3	C2
P012	G1	A1	R228	C3	D2
P012	G1	A1	R320	C1	D2
P020	D3	A2	R322	C1	D2
P020	D4	A2	R330	C2	D3
P020	D6	A2	R332	C3	D3
P020	F2	A2	R334	C2	D3
P020	G2	A2	R336	C3	D3
P022	D3	A2	TP022	G1	A0
P022	D6	A2	TP122	G1	B2
P022	E2	A2	TP216	C6	C1
P022	G2	A2	TP226	C6	C3
P030	B1	A3	TP320	G1	D2
R016	C5	A1	TP330	D3	D3
R017	C6	A1	TP331	D2	D3
R018	C5	A2	TP332	B3	D3
R026	C5	A2	TP333	B2	D3
R028	C5	A2	U314	C1	D1

P/O A26 ASSY ALSO SHOWN ON ◇11 , ◇12

A14 ASSY — **HEADER** ◇4

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C006	E2	A1	P016	B3	A2
C007	D3	A1	P016	B5	A2
C008	G2	A1	P016	D3	A2
C009	D3	A0	P016	D5	A2
C014	D5	B2	P016	E2	A2
C015	E2	B2	P016	G2	A2
C016	D5	A2	P016	H1	A2
C017	G2	A2	P016	H1	A2
C100	E2	A0	P101	A4	A0
C101	D4	A0	P101	H3	A0
C102	G2	B0	P102	B3	B0
C103	D4	B0	P102	B4	B0
C112	D6	B0	P102	B6	B0
C113	D6	B1	P102	D3	B0
C114	H2	B1	P102	D4	B0
C115	E2	B1	P102	D6	B0
C116	D6	B2	P102	F2	B0
P007	A2	A1	P102	G2	B0
P007	H2	A1	P102	H1	B0
P008	A3	A1	P102	H1	B0
P008	H3	A1	P113	B5	B0
P009	B3	A0	P113	D6	B0
P009	D3	A0	P113	F2	B0
P009	F2	A0	P113	H1	B0
P009	H1	A0	P114	A5	B1
P015	A4	A1	P114	H4	B1
P015	H4	B2			

P/O A26 ASSY — **HEADER** ◇4

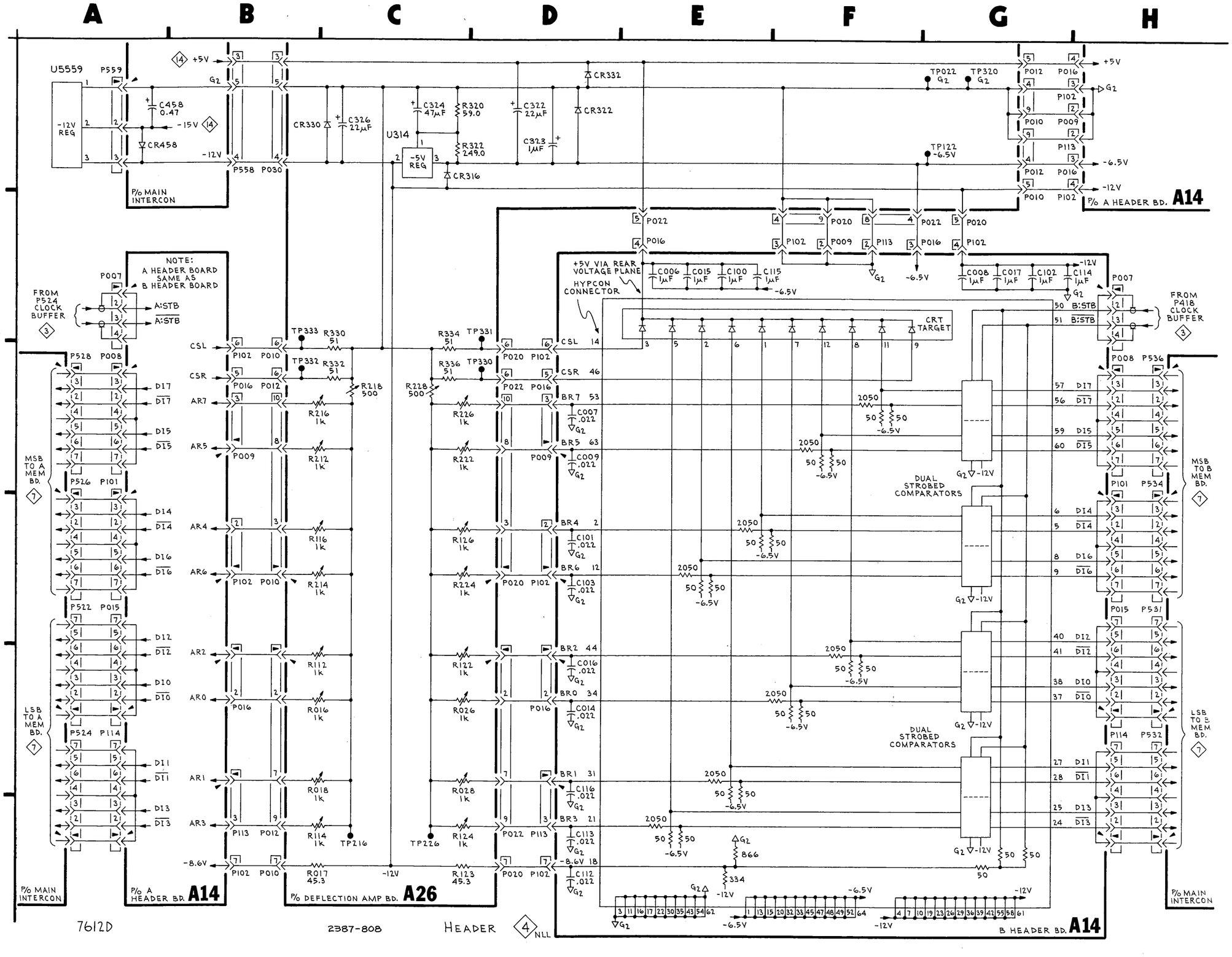
C322	D1	D2	R112	C5	B1
C324	C1	D2	R114	C6	B1
C326	C1	D2	R116	C4	B2
CR316	C1	D1	R122	C5	B2
CR322	D1	D2	R123	C6	B2
CR330	C1	D2	R124	C6	B2
CR332	D1	D3	R126	C4	B2
P010	B3	A1	R212	C3	C2
P010	B4	A1	R214	C4	C2
P010	B6	A1	R216	C3	C2
P010	G1	A1	R218	C3	D2
P010	G1	A1	R222	C3	C2
P012	B3	A1	R224	C4	C2
P012	B6	A1	R226	C3	C2
P012	G1	A1	R228	C3	D2
P012	G1	A1	R320	C1	D2
P020	D3	A2	R322	C1	D2
P020	D4	A2	R330	C2	D3
P020	D6	A2	R332	C3	D3
P020	F2	A2	R334	C2	D3
P020	G2	A2	R336	C3	D3
P022	D3	A2	TP022	G1	A0
P022	D6	A2	TP122	G1	B2
P022	E2	A2	TP216	C6	C1
P022	G2	A2	TP226	C6	C3
P030	B1	A3	TP320	G1	D2
R016	C5	A1	TP330	D3	D3
R017	C6	A1	TP331	D2	D3
R018	C5	A2	TP332	B3	D3
R026	C5	A2	TP333	B2	D3
R028	C5	A2	U314	C1	D1

P/O A26 ASSY ALSO SHOWN ON ◇11 , ◇12

P/O A68 ASSY — **HEADER** ◇4

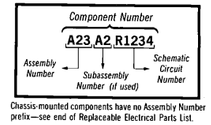
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C458	A1	E5	P534	H3	G3
CR458	A1	E5	P536	H3	G3
P524	A5	G2	P552	A4	G5
P526	A3	G2	P558	A1	G5
P528	A3	G3	P559	A1	G5
P530	H4	G3	U5559	A1	CHASSIS
P532	H5	G3			

A68 ASSY SHOWN IN FIG. 8-31



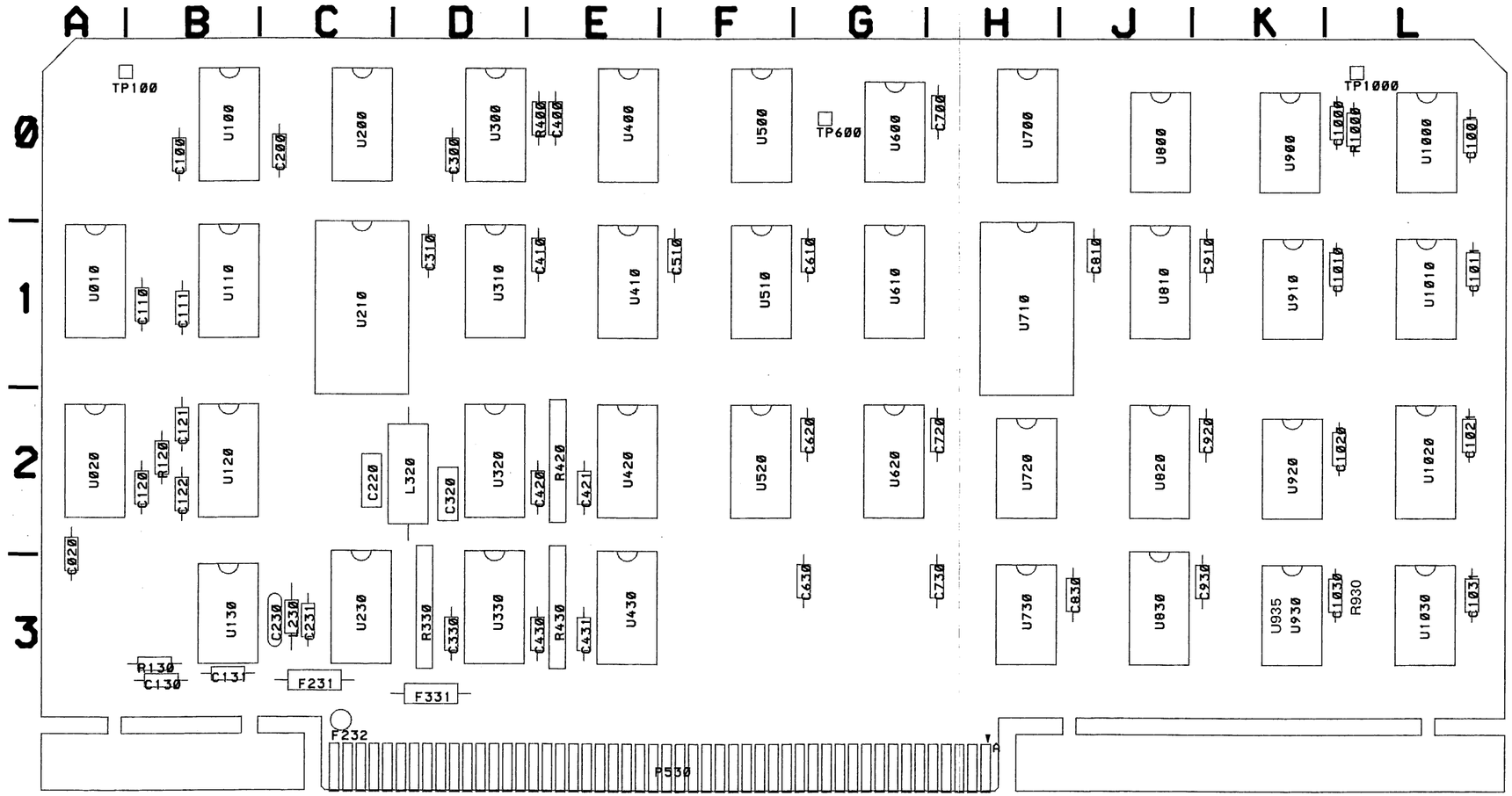
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TRANSLATOR A16



2387-809

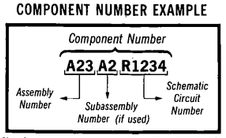
Fig. 8-6. Translator circuit board, assembly A16.

P/O A16 ASSY	
Circuit Number	**Schematic Location**
C130	F5
C131	E5
C230	E5
C231	E5
C400	B4
L230	E5
R130	E5
R330B	F5
R330D	E5
R330E	E5
R400	B4
R930*	E4
U010	C3
U100	C2
U110	C3
U130	E5
U200	C1
U210	B1
U230	F5
U300	C4
U400	C5
U500	C5
U600A	B2
U600B	B4
U600C	B2
U600D	H2
U700	E1
U710	B5
U720A	A2
U730B	G4
U730C	H4
U730D	H2
	P/O A1

P/O A68 ASSY	
J340	A2
J340	D1
	A

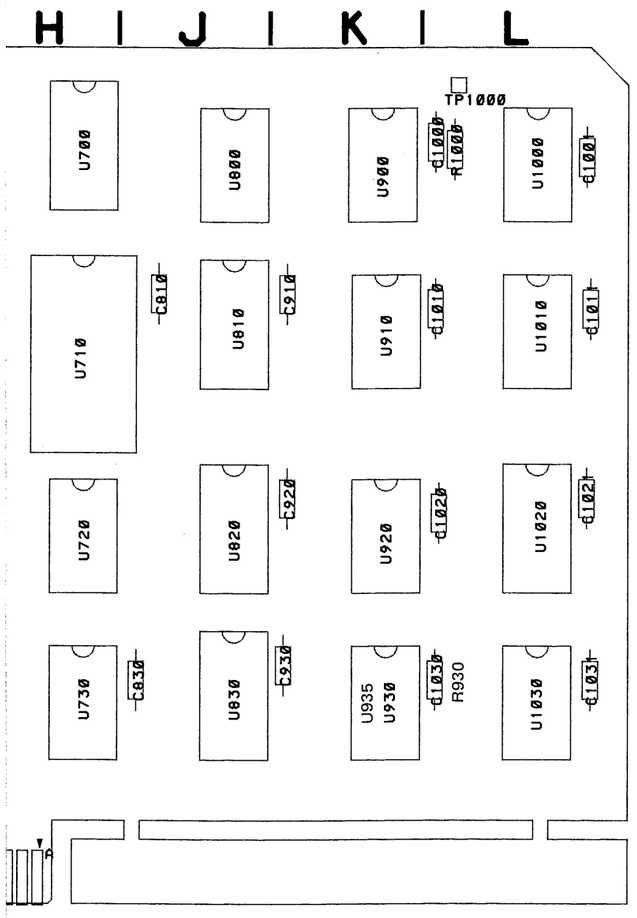
*See Parts List for serial number ranges.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



2387-809

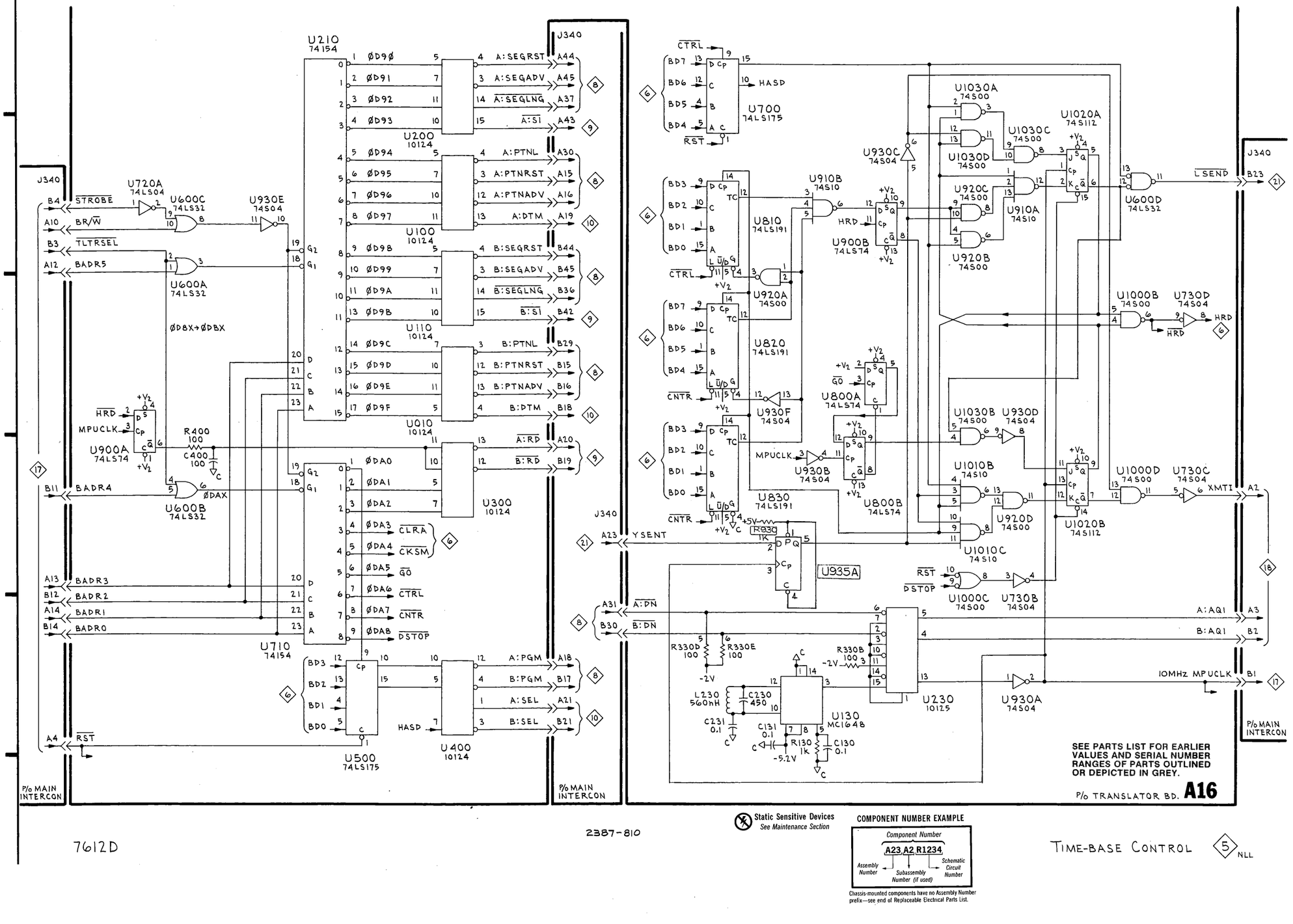
P/O A16 ASSY			TIMEBASE CONTROL ◇5		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C130	F5	B3	U800A	F3	J0
C131	E5	B3	U800B	F4	J0
C230	E5	C3	U810	E2	J1
C231	E5	C3	U820	E3	J2
C400	B4	E0	U830	E4	J3
L230	E5	C3	U900A	A4	K0
R130	E5	B3	U900B	F2	K0
R330B	F5	D3	U910A	G2	K1
R330D	E5	D3	U910B	F2	K1
R330E	E5	D3	U920A	E3	K2
R400	B4	E0	U920B	G2	K2
R930*	E4	L3	U920C	G2	K2
U010	C3	A1	U920D	G4	K2
U100	C2	B0	U930A	G5	K3
U110	C3	B1	U930B	F4	K3
U130	E5	B3	U930C	F2	K3
U200	C1	C0	U930C	G4	K3
U210	B1	C1	U930E	B2	K3
U230	F5	C3	U930F	E3	K3
U300	C4	D0	U935*	E4	K3
U400	C5	E0	U1000B	H2	L0
U500	C5	F0	U1000C	G4	L0
U600A	B2	G0	U1000D	H4	L0
U600B	B4	G0	U1010B	G4	L1
U600C	B2	G0	U1010C	G4	L1
U600D	H2	G0	U1020A	G2	L2
U700	E1	H0	U1020B	G4	L2
U710	B5	H1	U1030A	G1	L3
U720A	A2	H2	U1030B	G4	L3
U730B	G4	H3	U1030C	G2	L3
U730C	H4	H3	U1030D	G2	L3
U730D	H2	H3			

P/O A16 ASSY ALSO SHOWN ON ◇6

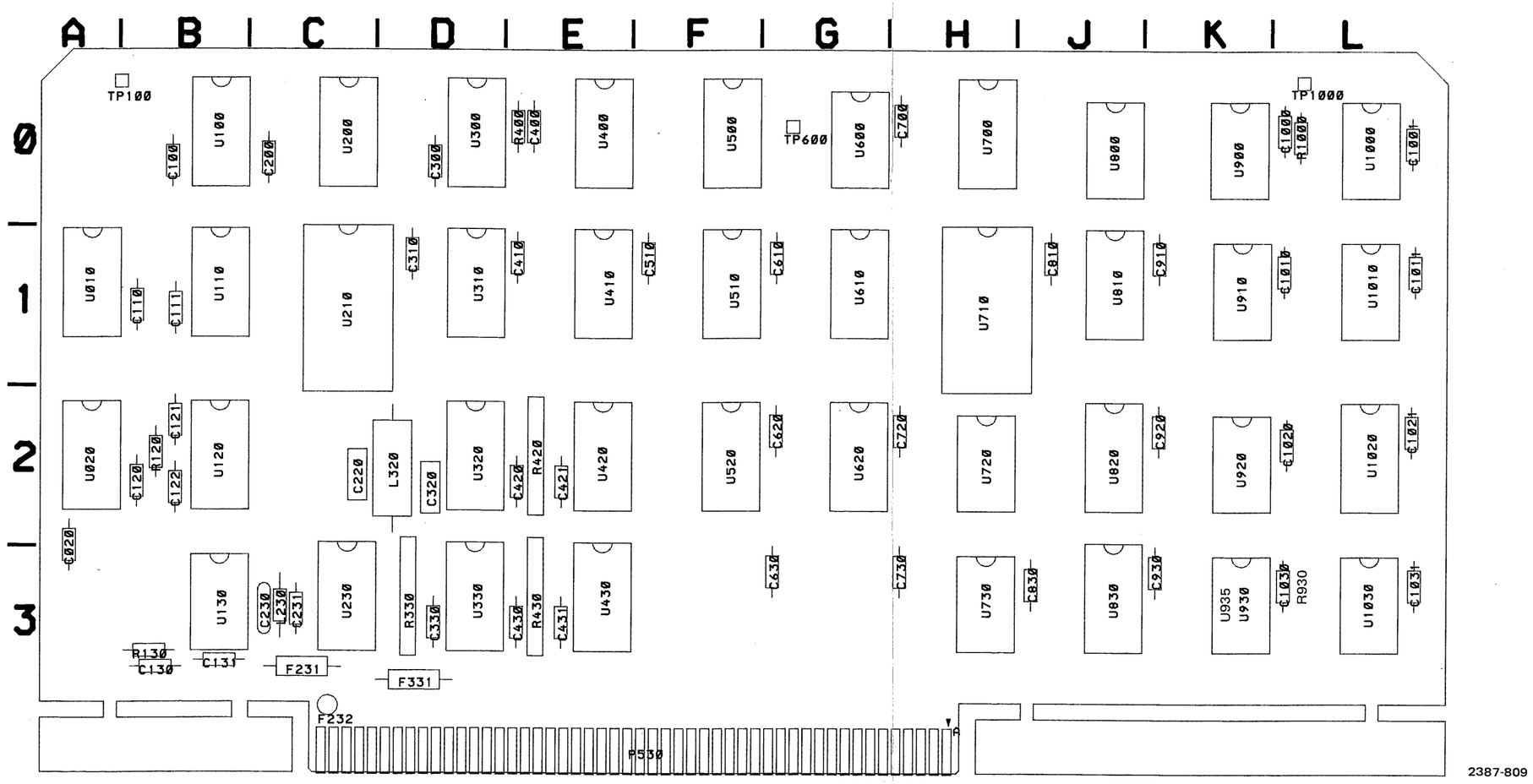
P/O A68 ASSY			TIMEBASE CONTROL ◇5		
J340	A2	D4	J340	D4	D4
J340	D1	D4	J340	H2	D4

A68 ASSY SHOWN IN FIG. 8-31

*See Parts List for serial number ranges.


U210 74154
U200 10124
U100 10124
U110 10124
U010 10124
U300 10124
U400 10124
U710 74154
U500 74LS175
U700 74LS175
U810 74LS191
U820 74LS191
U830 74LS191
U130 MC1648
U230 10125
U720A 74LS04
U600C 74LS32
U930E 74S04
U600A 74LS32
U900A 74LS74
U600B 74LS32
U910B 74S10
U900B 74LS74
U920A 74S00
U930F 74S04
U800A 74LS74
U930B 74S04
U800B 74LS74
U930C 74S04
U935A
U1030A 74S00
U1030C 74S00
U1030D 74S00
U920C 74S00
U920B 74S00
U1020A 74S112
U910A 74S10
U600D 74LS32
U1000B 74S00
U730D 74S04
U1030B 74S00
U930D 74S04
U1010B 74S10
U920D 74S00
U1010C 74S10
U1020B 74S112
U1000D 74S00
U730C 74S04
U1000C 74S00
U730B 74S04
U930A 74S04
J340
P/O MAIN INTERCON
P/O TRANSLATOR BD. A16
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
ØD8X→ØDBX
Static Sensitive Devices
See Maintenance Section
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
2387-810
7612D
TIME-BASE CONTROL 5 NLL
TIMEBASE CONTROL 5

TRANSLATOR A16



2387-809

Fig. 8-7. Translator circuit board, assembly A16.

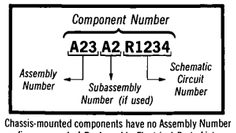
P/O A16 ASSY	
Circuit Number	**Schematic Location**
C020	B6
C100	B6
C110	B5
C111	B6
C120	C5
C121	D5
C122	B6
C200	C5
C220	B5
C300	B6
C310	C5
C320	B5
C330	C6
C410	C5
C420	D5
C421	C6
C430	B6
C431	C6
C510	D5
C610	D5
C620	D5
C630	B5
C700	B5
C720	C5
C730	C5
C810	C5
C830	C5
C910	D5
C920	D5
C930	D5
C1000	D5
C1001	B5
C1010	B5
C1011	C5
C1020	C5
C1021	C5
C1030	C5
C1031	D5
F231	B5
F232	B6
F331	B5
L320	B5
R120	D5
R330C	B2

P/O A16 A

P/O A68 ASSY	
J340	A1
J340	C1

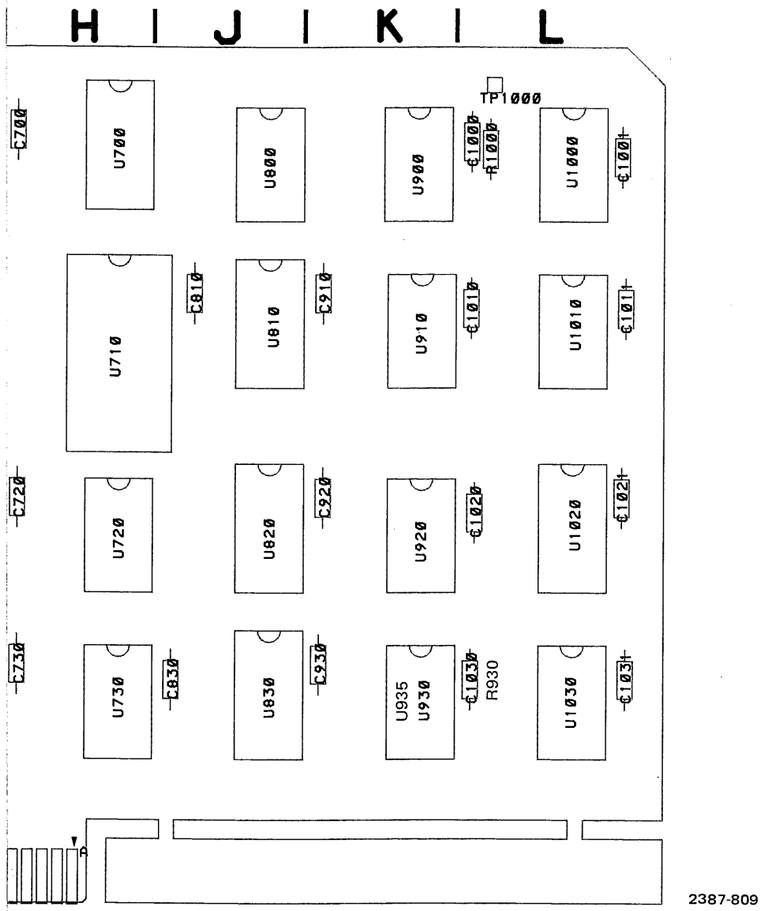
A6

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



2387-809

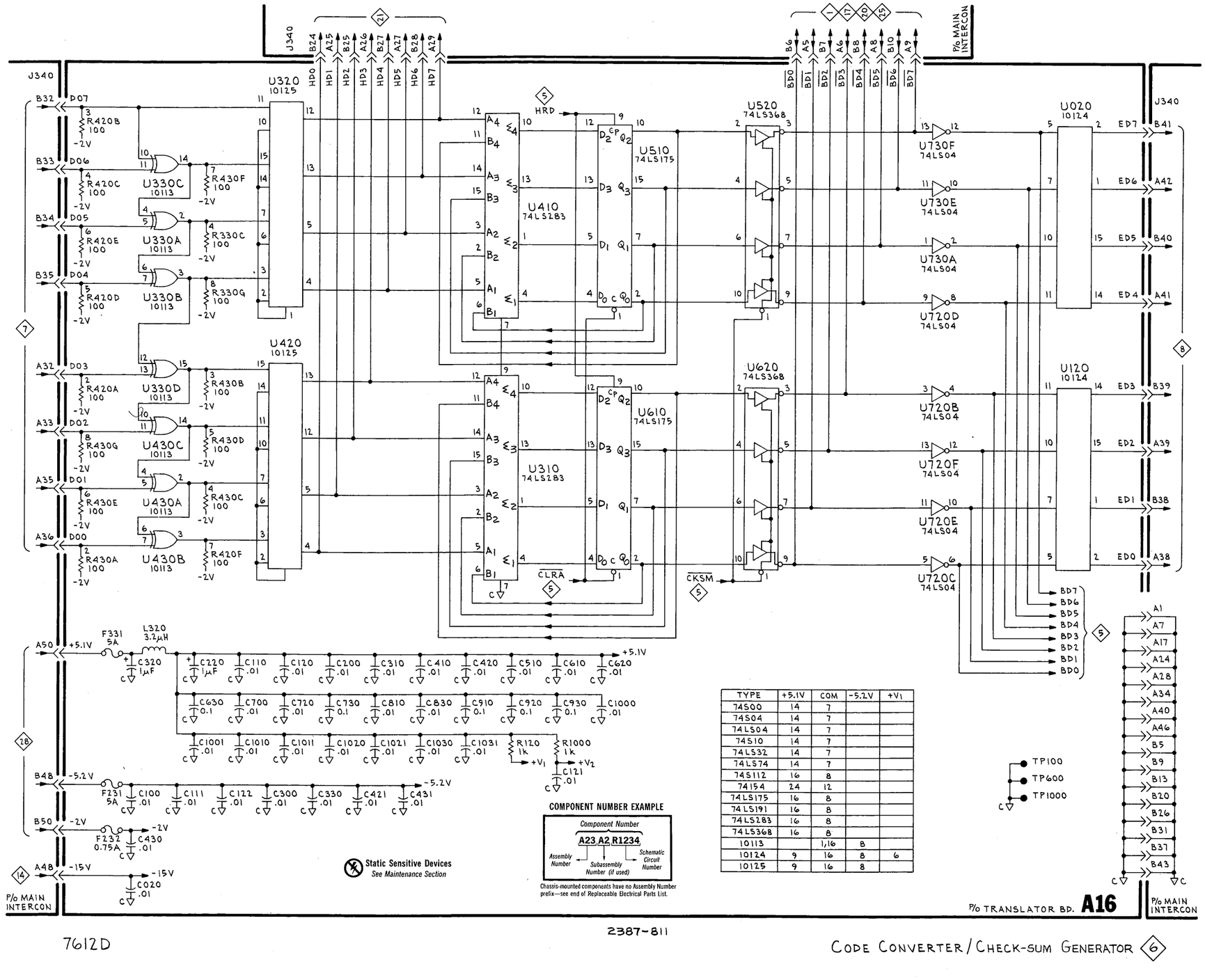
6.

P/O A16 ASSY			CODE CONVERTER/CHECKSUM GEN ◇6		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C020	B6	A3	R330G	B2	D2
C100	B6	B0	R420A	A3	E2
C110	B5	B1	R420B	A2	E2
C111	B6	B1	R420C	A2	E2
C120	C5	B2	R420D	A3	E2
C121	D5	B2	R420E	A2	E2
C122	B6	B2	R420F	B4	E2
C200	C5	C0	R430A	A4	E3
C220	B5	C2	R430B	B3	E3
C300	B6	D1	R430C	B4	E3
C310	C5	D1	R430D	B3	E3
C320	B5	D2	R430E	A4	E3
C330	C6	D3	R430F	B2	E3
C410	C5	E1	R430G	A3	E3
C420	D5	E2	R1000	D5	L0
C421	C6	E2	TP100	G5	B0
C430	B6	E3	TP600	G5	G0
C431	C6	E3	TP1000	G5	L0
C510	D5	F1	U020	G2	A2
C610	D5	G1	U120	G3	B2
C620	D5	G2	U230	A2	C2
C630	B5	G3	U310	D4	D1
C700	B5	H0	U330A	B2	D3
C720	C5	H2	U330B	B2	D3
C730	C5	H3	U330C	B2	D3
C810	C5	J1	U330D	B2	D3
C830	C5	J3	U410	D2	E1
C910	D5	K1	U420	B3	E2
C920	D5	K2	U430A	B4	E3
C930	D5	K3	U430B	B4	E3
C1000	D5	L0	U430C	B2	E3
C1001	B5	L0	U510	D2	F1
C1010	B5	L1	U520	E2	F2
C1011	C5	L1	U610	D3	G1
C1020	C5	L2	U620	E3	G2
C1021	C5	L2	U720B	F3	H2
C1030	C5	L3	U720C	F4	H2
C1031	D5	L3	U720D	F3	H2
F231	B5	C3	U720E	F4	H2
F232	B6	C3	U720F	F3	H2
F331	B5	D3	U730A	F2	H3
L320	B5	C3	U730E	F2	H3
R120	D5	B2	U730F	F2	H3
R330C	B2	D3			

P/O A16 ASSY ALSO SHOWN ON ◇5

P/O A68 ASSY			CODE CONVERTER/CHECKSUM GEN ◇6		
J340	A1	D4	J340	H1	D4
J340	C1	D4			

A68 ASSY SHOWN IN FIG. 8-31



TYPE	+5.1V	COM	-5.2V	+V1
74S00	14	7		
74S04	14	7		
74LS04	14	7		
74S10	14	7		
74LS32	14	7		
74LS74	14	7		
74S112	16	8		
74154	24	12		
74LS175	16	8		
74LS191	16	8		
74LS283	16	8		
74LS368	16	8		
10113		1,16	8	
10124	9	16	8	6
10125	9	16	8	

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number | Subassembly Number (if used) | Schematic Circuit Number

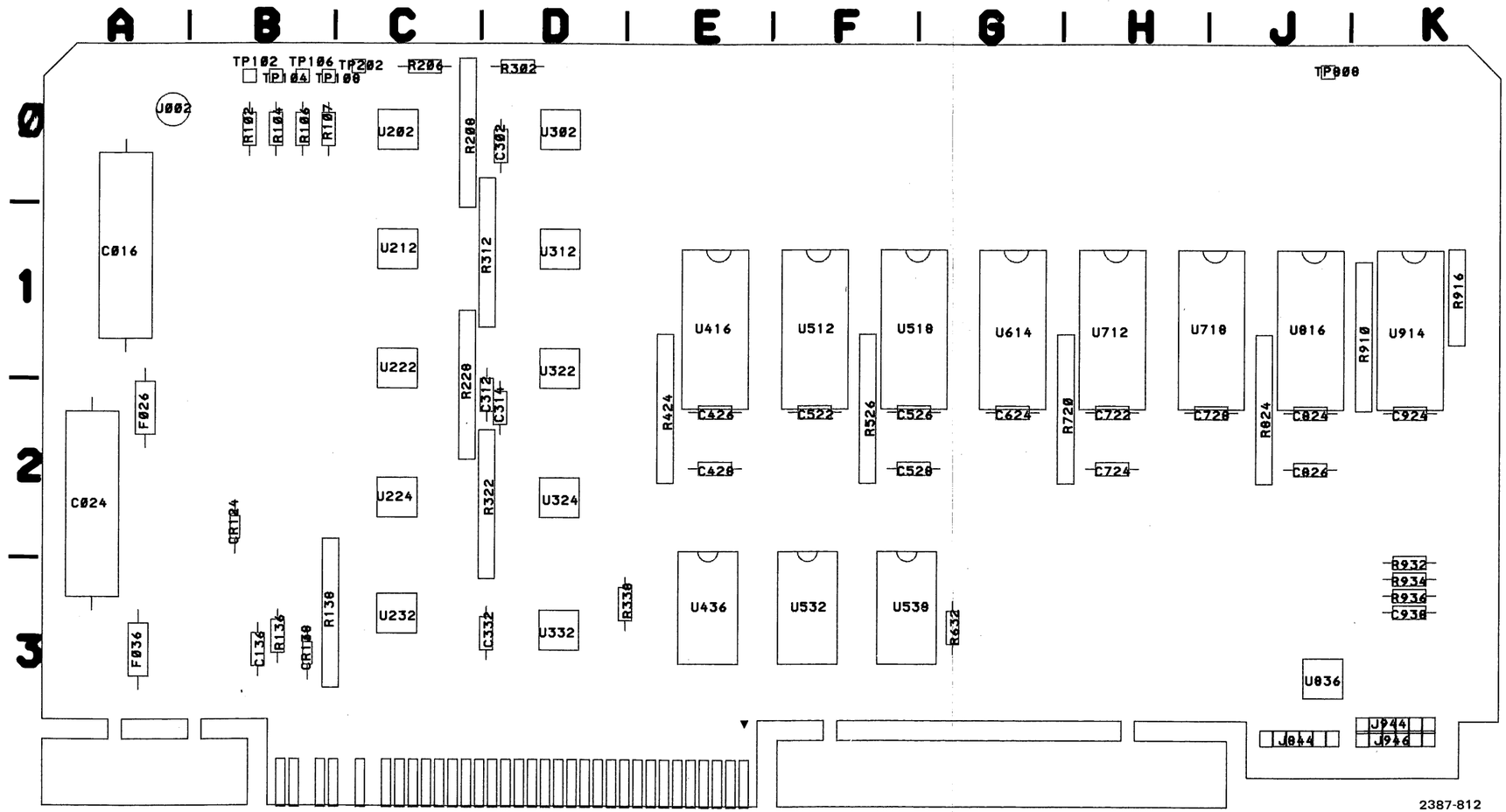
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

2387-811

7612D

CODE CONVERTER/CHECK-SUM GENERATOR 6

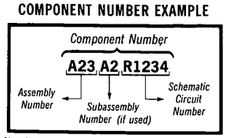


DATA STORAGE A18

Fig. 8-8. Data Storage circuit board, assembly A18.

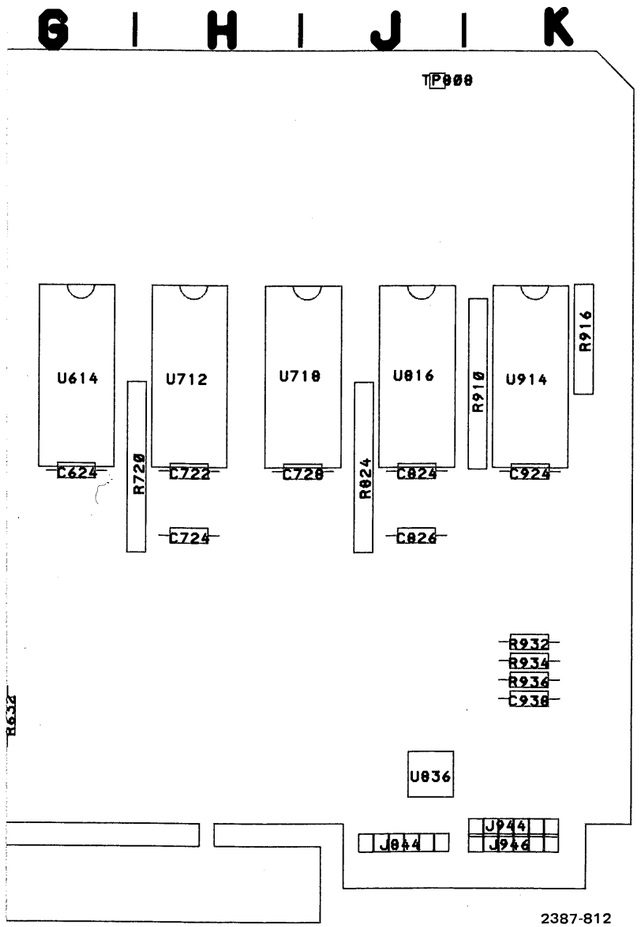
A18 ASSY		
Circuit Number	Schematic Location	Board Location
C016	D1	A1
C024	D1	A2
C136	C1	B3
C302	D1	D0
C312	D1	D2
C314	D1	D2
C332	D1	D3
C426	C1	E2
C428	C2	E2
C522	C1	F2
C526	D1	F2
C528	D2	F2
C624	D1	G2
C722	D1	H2
C724	D2	H2
C728	C1	H2
C824	D1	J2
C826	D2	J2
C924	D1	K2
C938	D2	K3
CR124	A6	B2
CR138	B2	B3
F026	E1	A2
F036	E1	A3
P002	A6	A0
P944	A1	K3
P944	F5	K3
P946	A1	K3
R102	B3	B0
R104	B4	B0
R106	B5	B0
R108	B5	B0
R108	B6	B0
R136	B6	B3
R138B	B2	B3
R138C	A3	B3
R138D	A4	B3
R138E	A3	B3
R138F	B1	B3
R138G	B5	B3
R138H	B5	B3
R138J	B6	B3
R206	B1	C0
R208A	D3	C0
R208B	D3	C0
R208C	D3	C0
R208D	D3	C0
R208E	C3	C0
R208F	C3	C0
R208G	C3	C0
R208H	C3	C0
R208J	B2	C0
R228A	D5	C2
R228B	D5	C2
R228C	D5	C2
R228D	D5	C2
R228E	C5	C2
R228F	C5	C2

COMPONENT NUMBER EXAMPLE



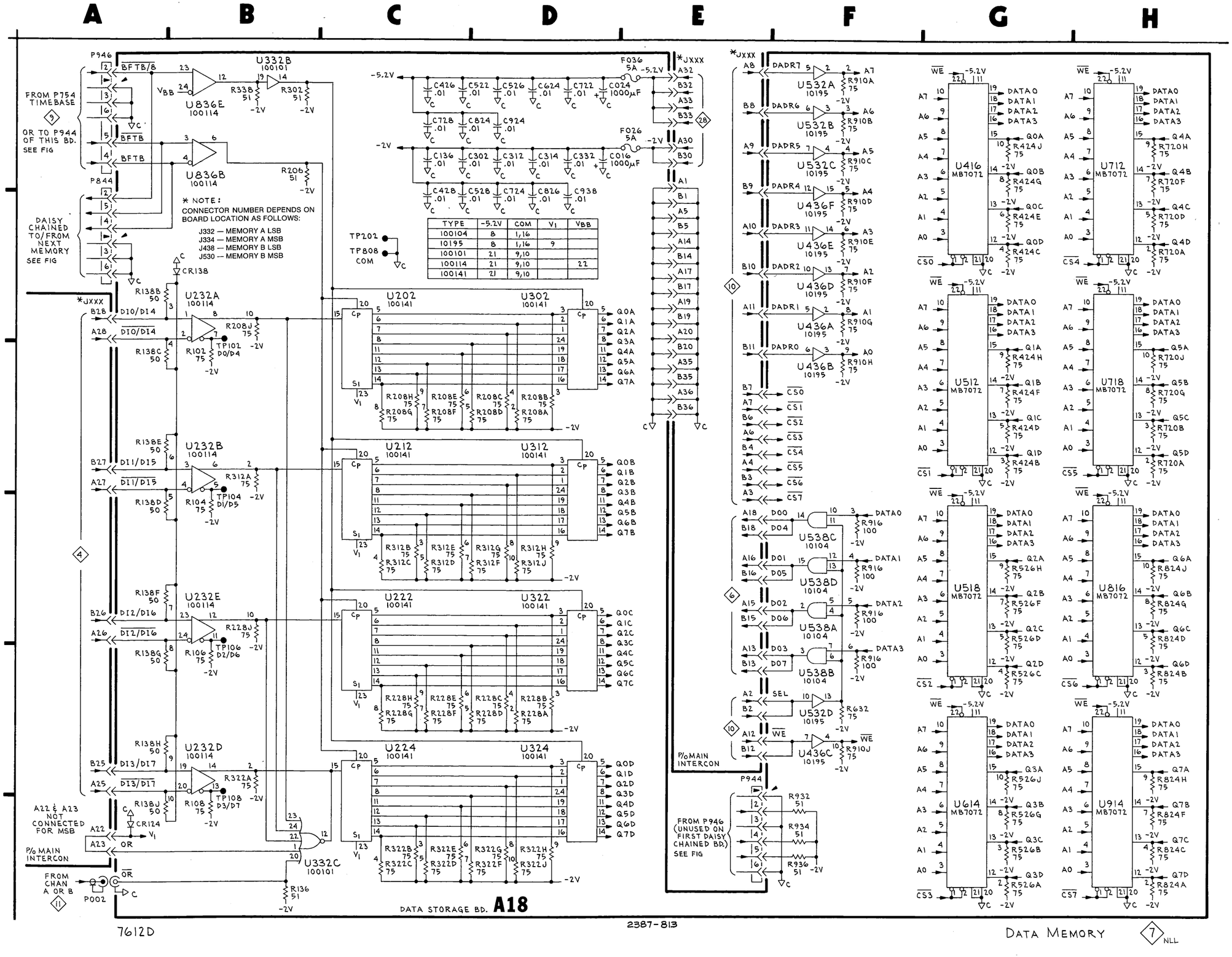
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



A18 ASSY — **DATA MEMORY** ◇7

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C016	D1	A1	R228G	C5	C2	R910C	F1	K1
C024	D1	A2	R228H	C5	C2	R910D	F2	K1
C136	C1	B3	R228J	B4	C2	R910E	F2	K1
C302	D1	D0	R302	B1	D0	R910F	F2	K2
C312	D1	D2	R312A	B3	D1	R910G	F2	K2
C314	D1	D2	R312B	C4	D1	R910H	F3	K1
C332	D1	D3	R312C	C4	D1	R910J	F5	K2
C426	C1	E2	R312D	C4	D1	R916	F4	K1
C428	C2	E2	R312E	C4	D1	R916	F5	K1
C522	C1	F2	R312F	D4	D1	R932	F6	K3
C526	D1	F2	R312G	D4	D1	R934	F6	K3
C528	D2	F2	R312H	D4	D1	R936	F6	K3
C624	D1	G2	R312J	D4	D1	TP102	B2	B0
C722	D1	H2	R322A	B5	D1	TP104	B3	B0
C724	D2	H2	R322B	C6	D2	TP106	B4	B0
C728	C1	H2	R322C	C6	D2	TP108	B5	B0
C824	D1	J2	R322D	D6	D2	TP202	C2	C0
C826	D2	J2	R322E	D6	D2	TP808	C2	J0
C924	D1	K2	R322F	D6	D2	U202	C2	C0
C938	D2	K3	R322G	D6	D2	U212	C3	C1
CR124	A6	B2	R322H	D6	D2	U222	C4	C1
CR138	B2	B3	R322J	D6	D2	U224	C5	C2
F026	E1	A2	R338	B1	D3	U232A	B2	C3
F036	E1	A3	R424B	G3	E2	U232B	B3	C3
P002	A6	A0	R424C	G2	E2	U232D	B5	C3
P944	A1	K3	R424D	G3	E2	U232E	B4	C3
P944	F5	K3	R424E	G2	E2	U302	D2	D0
P946	A1	K3	R424F	G3	E2	U312	D3	D1
R102	B3	B0	R424G	G1	E2	U322	D4	D1
R104	B4	B0	R424H	G3	E2	U322C	C6	D1
R106	B5	B0	R424J	G1	E2	U324	D5	D2
R108	B5	B0	R526	G6	F2	U332B	B1	D1
R108	B6	B0	R526A	G6	F2	U416	G1	E1
R136	B6	B3	R526B	G6	F2	U436A	F2	E3
R138B	B2	B3	R526C	G5	F2	U436B	F3	E3
R138C	A3	B3	R526D	G4	F2	U436C	F5	E3
R138D	A4	B3	R526F	G4	F2	U436D	F2	E3
R138E	A3	B3	R526H	G4	F2	U436E	F2	E3
R138F	B1	B3	R526J	G5	F2	U436F	F2	E3
R138G	B5	B3	R632	F5	G3	U512	G3	F1
R138H	B5	B3	R720A	H2	H2	U518	G4	F1
R138J	B6	B3	R720A	H3	H2	U532A	F1	F3
R206	B1	C0	R720B	H3	H2	U532B	F1	F3
R208A	D3	C0	R720D	H2	H2	U532C	F1	F3
R208B	D3	C0	R720F	H1	H2	U532D	F5	F3
R208C	D3	C0	R720G	H3	H2	U538A	F4	F3
R208D	D3	C0	R720H	H1	H2	U538B	F5	F3
R208E	C3	C0	R720J	H3	H2	U538C	F4	F3
R208F	C3	C0	R824A	G5	J2	U538D	F4	F3
R208G	C3	C0	R824A	H6	J2	U614	G6	G1
R208H	C3	C0	R824B	G5	J2	U712	H1	H1
R208J	B2	C0	R824C	H6	J2	U718	H3	H1
R228A	D5	C2	R824D	H4	J2	U816	H4	J1
R228B	D5	C2	R824F	H6	J2	U836B	B1	J3
R228C	D5	C2	R824G	H4	J2	U836E	B1	J3
R228D	D5	C2	R824J	H4	J2	U914	H6	K1
R228E	C5	C2	R910A	F1	K1			
R228F	C5	C2	R910B	F1	K1			


FROM P754 TIMEBASE
OR TO P944 OF THIS BD. SEE FIG
DAISY CHAINED TO/FROM NEXT MEMORY SEE FIG
* NOTE: CONNECTOR NUMBER DEPENDS ON BOARD LOCATION AS FOLLOWS:
J332 — MEMORY A LSB
J334 — MEMORY A MSB
J438 — MEMORY B LSB
J530 — MEMORY B MSB
TYPE | -5.2V | COM | V1 | VBB
100104 | 8 | 1,16 | |
10195 | 8 | 1,16 | 9 |
100101 | 21 | 9,10 | |
100114 | 21 | 9,10 | | 22
100141 | 21 | 9,10 |
A22 & A23 NOT CONNECTED FOR MSB
P/O MAIN INTERCON
FROM CHAN A OR B
P/O MAIN INTERCON
FROM P946 (UNUSED ON FIRST DAISY CHAINED BD.) SEE FIG
DATA STORAGE BD. A18
DATA MEMORY
7612D
2387-813
Static Sensitive Devices
See Maintenance Section
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
DATA MEMORY

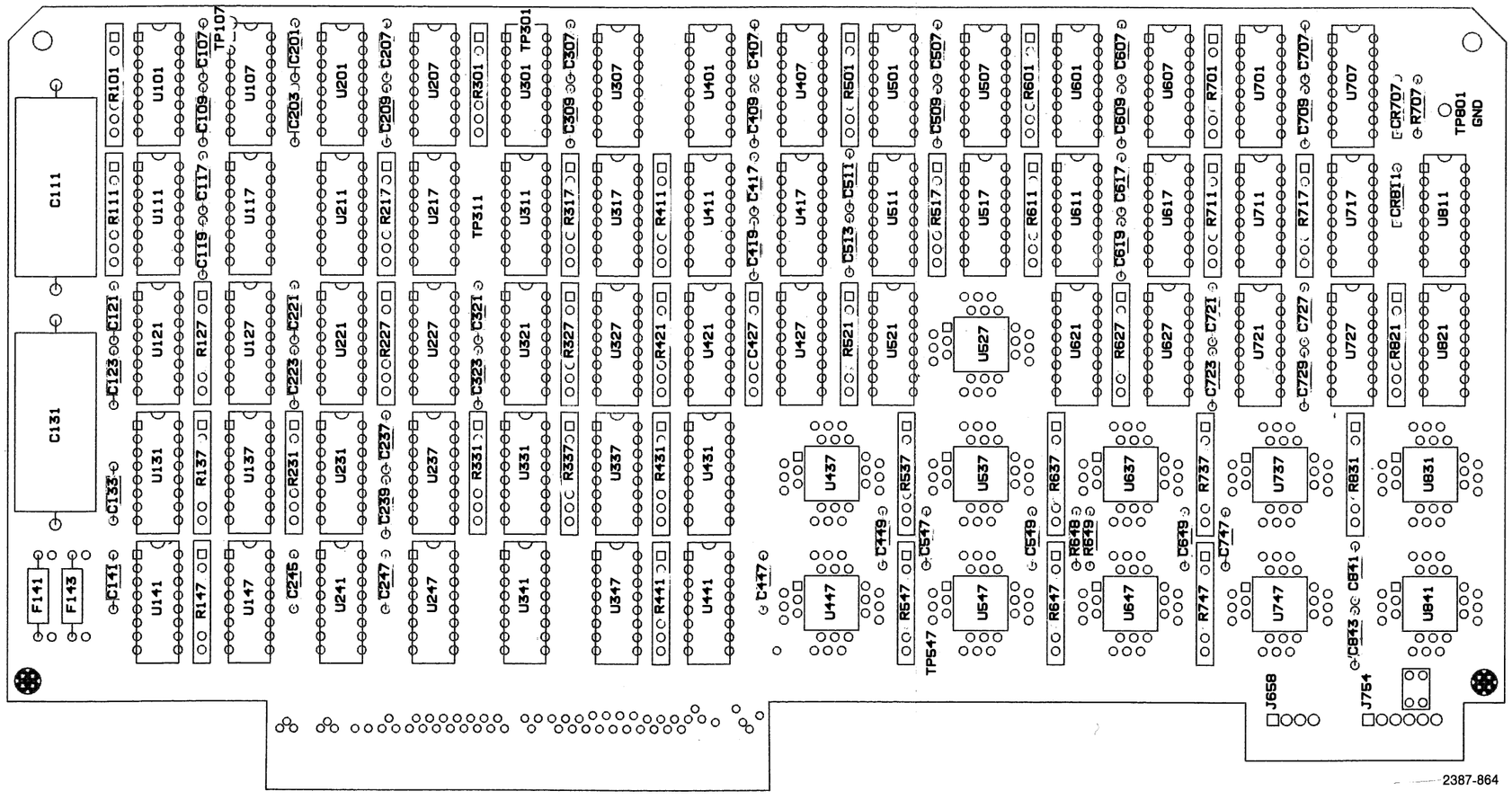
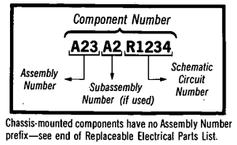


Fig. 8-9. Timebase circuit board, assembly A20 (SN B030708 & up).

P/O A20 ASSY (SN	
Circuit Number	Sche Loc
C107	G
C109	G
C111	H
C117	G
C119	G
C121	F
C123	F
C131	H
C133	F
C141	F
C201	G
C203	G
C207	F
C209	G
C221	G
C223	G
C237	F
C239	F
C247	G
C307	G
C309	G
C321	G
C323	F
C407	G
C409	G
C417	H
C419	G
C447	G
C507	F
C509	G
C511	H
C513	G
C547	F
C607	F
C609	F
C617	G
C619	F
C649	G
C707	G
C709	G
C721	G
C723	G
C727	G
C729	G
C747	H
C841	H
C843	H
CR707	F
F141	H
F143	H
R101A	D
R101B	D
R101C	D

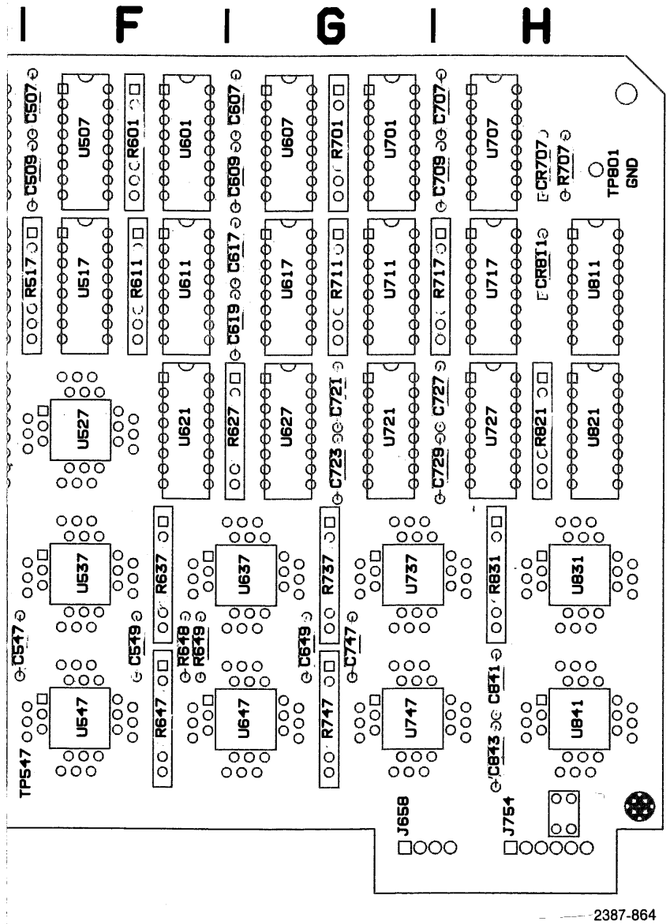
TIMEBASE A20
(SN B030708 & UP)

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

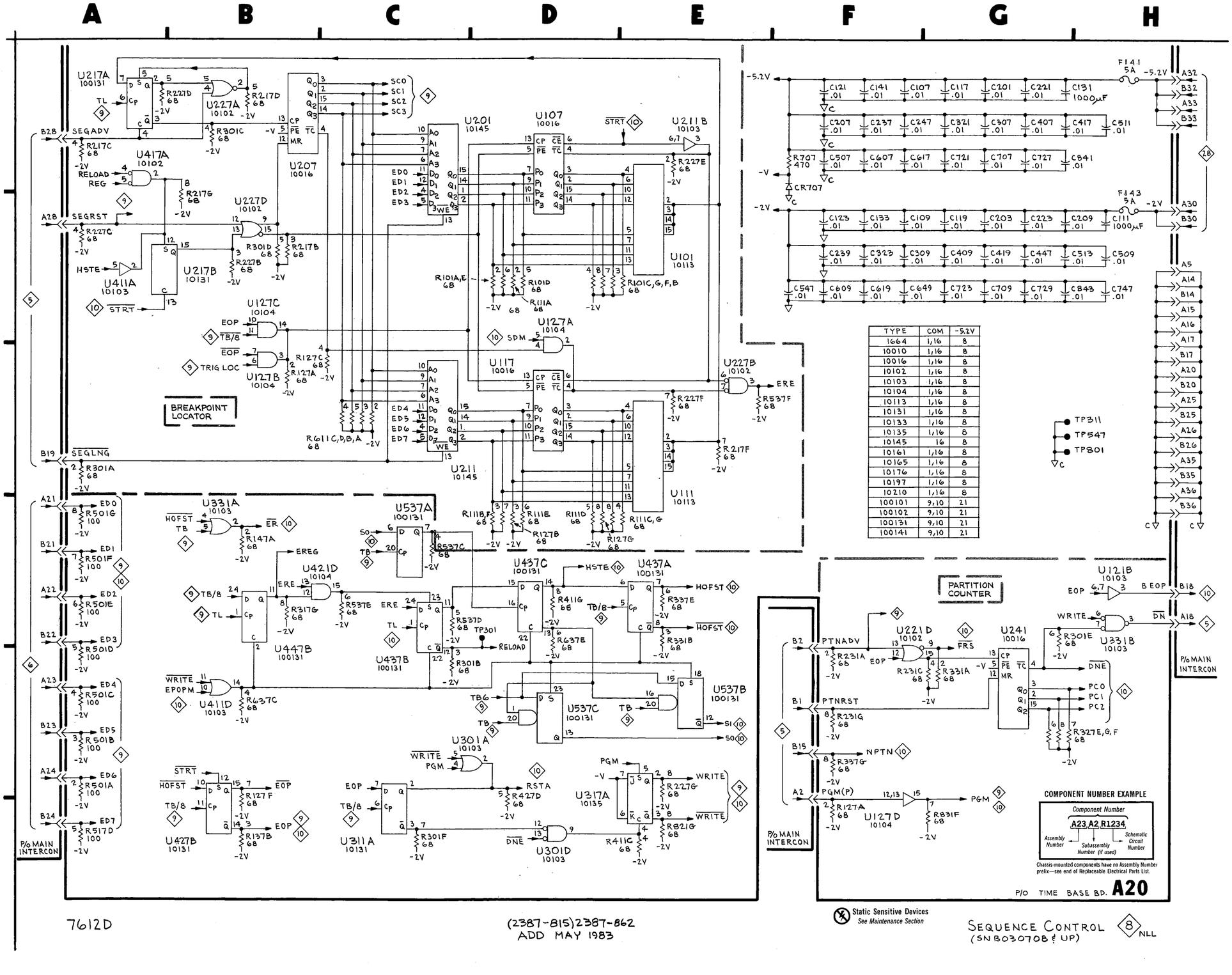


& up).

P/O A20 ASSY (SN B030708 & UP) — SEQUENCE CONTROL ◇8

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C107	G1	B0	R101D	D2	A0	R517D	A6	F1
C109	G2	B0	R101E	C2	A0	R537C	C4	E3
C111	H2	A1	R101F	E2	A0	R537D	D4	E3
C117	G1	B1	R101G	E2	A0	R537E	C4	E3
C119	G2	B1	R111A	D2	A1	R537F	F3	E3
C121	F1	A2	R111B	D4	A1	R611A	C3	F1
C123	F2	A2	R111C	E4	A1	R611B	C3	F1
C131	H1	A3	R111D	D4	A1	R611C	C3	F1
C133	F2	A3	R111E	D4	A1	R611D	C3	F1
C141	F1	A4	R111F	D4	A1	R637E	D4	F3
C201	G1	B0	R111G	E4	A1	R707	F1	H0
C203	G2	B0	R127A	F6	B2	R821G	E6	H2
C207	F1	C0	R127B	D4	B2	R831F	G6	H3
C209	G2	C0	R127C	B3	B2			
C221	G1	B2	R127D	B3	B2	TP301	D4	C0
C223	G2	B2	R127F	B5	B2	TP311	H3	C1
C237	F1	C3	R127G	E4	B2	TP547	H3	F4
C239	F2	C3	R137B	B6	B3	TP801	H3	H0
C247	G1	C4	R147A	B4	B4			
C307	G1	D0	R217A	B2	C1	U101	E2	A0
C309	G2	D0	R217B	B2	C1	U107	D1	B0
C321	G1	C2	R217C	A1	C1	U111	E3	A1
C323	F2	C2	R217D	B1	C1	U117	D3	B1
C407	G1	E0	R217F	E3	C1	U121B	H4	A2
C409	G2	E0	R227B	B2	C2	U127B	B3	B2
C417	H1	E1	R227C	A2	C2	U127C	B2	B2
C419	G2	E1	R227D	B1	C2	U127D	F6	B2
C447	G2	E4	R227E	E1	C2	U201	D1	B0
C507	F1	F0	R227F	E3	C2	U207	B1	C0
C509	G2	F0	R227G	E5	C2	U211	C3	B1
C511	H1	E1	R231A	F5	B3	U211B	E1	B1
C513	G2	E1	R231C	G5	B3	U217A	A1	C1
C547	F2	E3	R231G	F5	B3	U217B	B2	C1
C607	F1	G0	R301A	A3	C0	U221D	F4	B2
C609	F2	G0	R301B	D5	C0	U227A	B1	C2
C617	G1	G1	R301C	B1	C0	U227B	E3	C2
C619	F2	G1	R301D	B2	C0	U227D	B2	C2
C649	G2	G3	R301E	H4	C0	U241	G4	B4
C707	G1	H0	R301F	C6	C0	U301A	D5	C0
C709	G2	H0	R317G	B4	D1	U301D	D6	C0
C721	G1	G2	R327E	H5	D2	U311A	C6	C1
C723	G2	G2	R327F	H5	D2	U317A	D5	D1
C727	G1	G2	R327G	H5	D2	U331A	B4	C3
C729	G2	H2	R331A	G5	C3	U331B	H4	C3
C747	H2	G3	R331B	E4	C3	U411A	A2	D1
C841	H1	H4	R337G	F5	D3	U411C	B5	D1
C843	H2	H4	R411C	E6	D1	U417A	A1	E1
			R411G	D4	D1	U421D	C4	D2
CR707	F1	H0	R427D	D5	E2	U427B	B6	E2
			R501A	A5	E0	U437A	E4	E3
F141	H1	A4	R501B	A5	E0	U437B	B5	E3
F143	H2	H4	R501C	A5	E0	U437C	D4	E3
			R501D	A5	E0	U447B	B5	E4
R101A	D2	A0	R501E	A4	E0	U537A	C4	F3
R101B	D2	A0	R501F	A4	E0	U537B	E5	F3
R101C	D2	A0	R501G	A4	E0	U537C	D5	F3

P/O A20 ASSY ALSO SHOWN ON ◇9 , ◇10


A
B
C
D
E
F
G
H
1
2
3
4
5
6
U217A 100131
U227A 10102
U207 10016
U201 10145
U107 10016
U211B 10103
U417A 10102
U227D 10102
U217B 10131
U411A 10103
U127C 10104
U127A 10104
U127B 10104
U117 10016
U227B 10102
U211 10145
U111 10113
U101 10113
U331A 10103
U537A 100131
U421D 10104
U437C 100131
U437A 100131
U447B 100131
U437B 100131
U411D 10103
U537C 100131
U537B 100131
U301A 10103
U427B 10131
U311A 10131
U301D 10103
U317A 10135
U127D 10104
U221D 10102
U241 10016
U121B 10103
U331B 10103
SEGADV
SEGRST
SEGLNG
RELOAD REG
HSTE
STRT
TL
TB/8
TRIG LOC
EOP
SDM
ERE
BREAKPOINT LOCATOR
HOFST
TB
WRITE
EPOPM
PGM
RSTA
DNE
EREG
RELOAD
TP301
SCO
SC1
SC2
SC3
ED0
ED1
ED2
ED3
ED4
ED5
ED6
ED7
SO
SI
PTNADV
PTNRST
NPTN
PGM(P)
FRS
DNE
PCO
PC1
PC2
B EOP
DN
-5.2V
-2V
-V
F141 5A
F143 5A
C121 .01
C141 .01
C107 .01
C117 .01
C201 .01
C221 .01
C131 1000µF
C207 .01
C237 .01
C247 .01
C321 .01
C307 .01
C407 .01
C417 .01
C511 .01
R707 470
C507 .01
C607 .01
C617 .01
C721 .01
C707 .01
C727 .01
C841 .01
CR707
C123 .01
C133 .01
C109 .01
C119 .01
C203 .01
C223 .01
C209 .01
C111 1000µF
C239 .01
C323 .01
C309 .01
C409 .01
C419 .01
C447 .01
C513 .01
C509 .01
C547 .01
C609 .01
C619 .01
C649 .01
C723 .01
C709 .01
C729 .01
C843 .01
C747 .01
TP311
TP547
TP801
TYPE | COM | -5.2V
1664 | 1,16 | 8
10010 | 1,16 | 8
10016 | 1,16 | 8
10102 | 1,16 | 8
10103 | 1,16 | 8
10104 | 1,16 | 8
10113 | 1,16 | 8
10131 | 1,16 | 8
10133 | 1,16 | 8
10135 | 1,16 | 8
10145 | 16 | 8
10161 | 1,16 | 8
10165 | 1,16 | 8
10176 | 1,16 | 8
10197 | 1,16 | 8
10210 | 1,16 | 8
100101 | 9,10 | 21
100102 | 9,10 | 21
100131 | 9,10 | 21
100141 | 9,10 | 21
PARTITION COUNTER
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
P/O TIME BASE BD. A20
P/O MAIN INTERCON
Static Sensitive Devices
See Maintenance Section
7612D
(2387-815)2387-862
ADD MAY 1983
SEQUENCE CONTROL
(SN B030708 & UP)
8 NLL

TIMEBASE A20
(SN B030707 & BELOW)

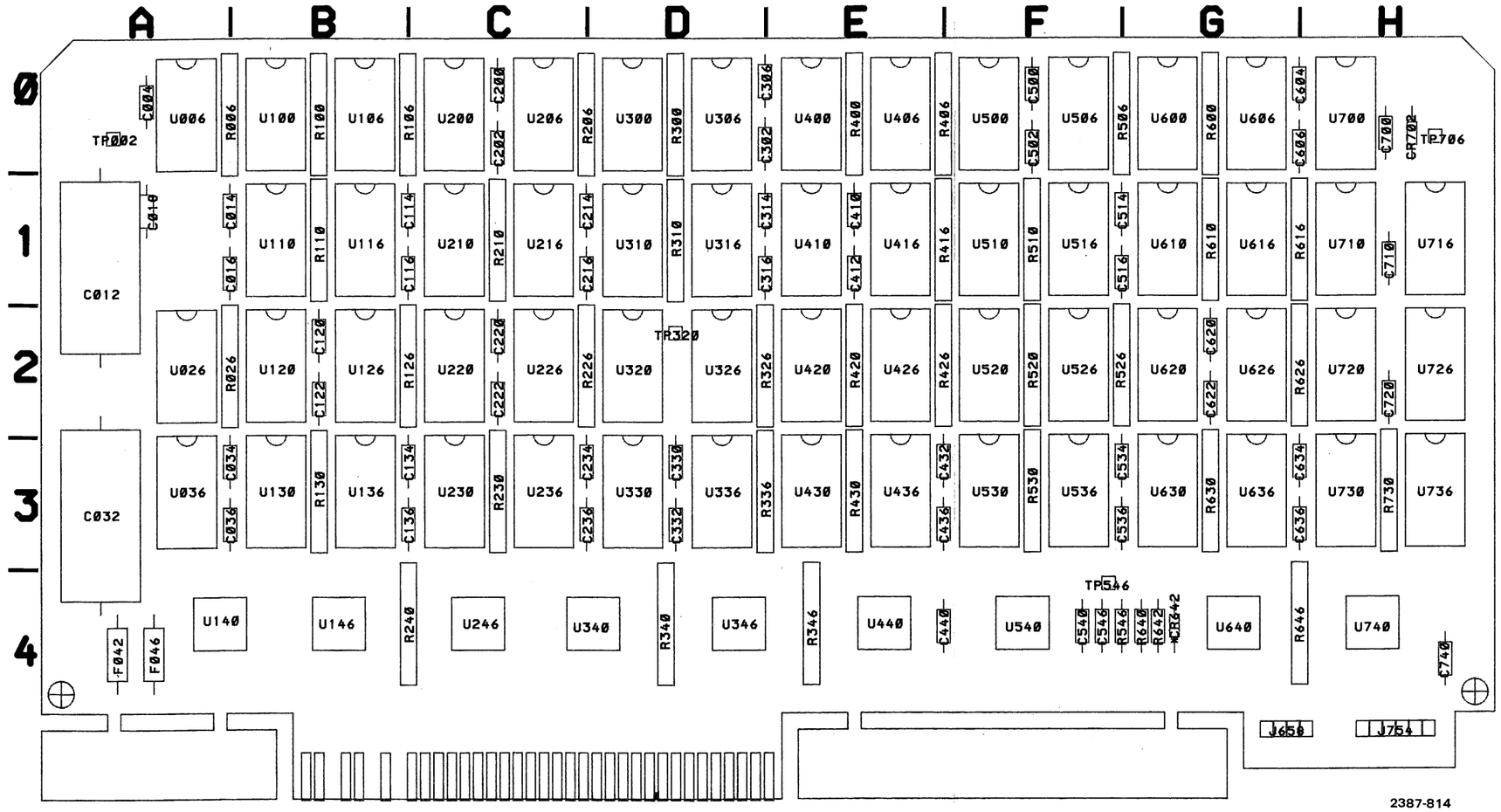
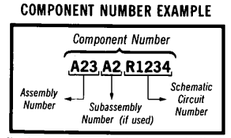


Fig. 8-9A. Timebase circuit board, assembly A20 (SN B030707 & below).

P/O A20 ASSY (SN B030707 & below)		
Circuit Number	**Schematic Location**	**Board Location**
U126	B1	B2
C004	F2	A0
C012	H1	A1
C014	F1	A1
C016	F2	A1
C032	H2	A3
C034	F1	A3
C036	F1	A3
C114	G1	B1
C116	F2	B1
C120	G1	B2
C122	G2	B2
C134	G1	B3
C136	G1	B3
C200	G2	C0
C202	G2	C0
C214	F1	C1
C216	G2	C1
C220	F1	C2
C222	F2	C2
C234	F1	C3
C236	F2	C3
C302	F2	D0
C306	G2	D0
C314	G1	D1
C316	G2	D1
C330	G1	D3
C332	G2	D3
C410	G1	E1
C412	G2	E1
C432	H2	E3
C436	G1	E3
C440	H1	E4
C500	F2	F0
C502	F2	F0
C514	F1	F1
C516	F2	F1
C534	F2	F3
C536	F1	F3
C540	F1	F4
C604	G2	G0
C606	G2	G0
C620	G1	G2
C622	G2	G2
C634	G1	G3
C636	G2	G3
C700	G1	H0
C710	G1	H1
C720	H2	H2
C740	H1	H4
CR642	F1	G4
F042	H2	A4
F046	H1	A4
R006C	C3	A0
R006D	G5	A0
R006E	E3	A0
R026	B5	A2

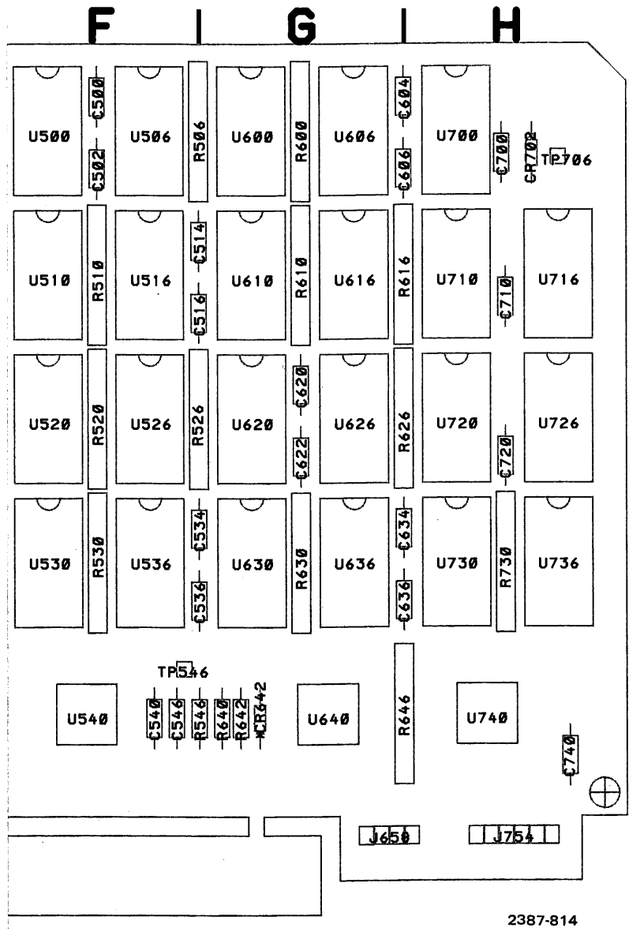
P/O A20

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



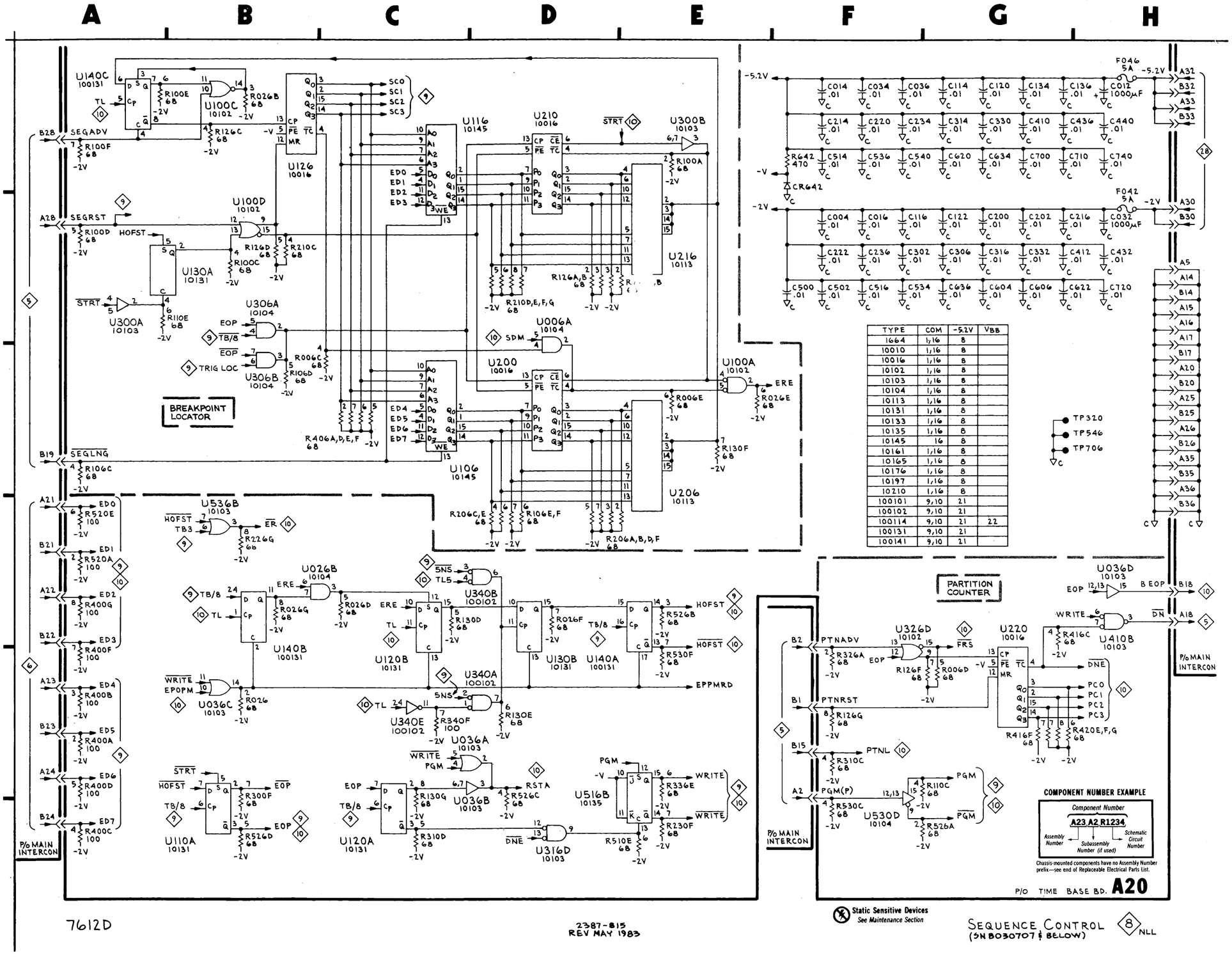
w).

Y 1983

P/O A20 ASSY (SN B030707 & below) — SEQUENCE CONTROL ◇8

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
U126	B1	B2	R026B	B1	A2	R416C	G4	E1
C004	F2	A0	R026E	E3	A2	R416F	G5	E1
C012	H1	A1	R026G	B4	A2	R420E	G5	E2
C014	F1	A1	R026G	C4	A2	R420F	G5	E2
C016	F2	A1	R100A	E1	B0	R420G	H5	E2
C032	H2	A3	R100C	B2	B0	R510E	E6	F1
C034	F1	A3	R100D	A2	B0	R520A	A4	F2
C036	F1	A3	R100E	A1	B0	R520E	A4	F2
C114	G1	B1	R100F	A1	B0	R526A	G6	F2
C116	F2	B1	R106C	A3	B0	R526B	E4	F2
C120	G1	B2	R106D	B3	D0	R526C	D6	F2
C122	G2	B2	R106E	D4	B0	R526D	B6	F2
C134	G1	B3	R106F	D4	B0	R530C	F6	F3
C136	G1	B3	R110C	G5	B1	R530F	E5	F3
C200	G2	C0	R110E	A2	B1	R642	F1	G4
C202	G2	C0	R126A	D2	C1	TP320	H3	D2
C214	F1	C1	R126B	D2	C1	TP546	H3	F4
C216	G2	C1	R126C	B1	B2	TP706	H3	H0
C220	F1	C2	R126D	B2	B2	U006A	D2	A0
C222	F2	C2	R126F	G5	B2	U026B	B4	A2
C234	F1	C3	R126G	F5	B2	U036A	C5	A3
C236	F2	C3	R130C	F5	B3	U036B	C5	A3
C302	F2	D0	R130D	C4	B3	U036C	B5	A3
C306	G2	D0	R130E	D5	B3	U036D	H4	A3
C314	G1	D1	R130F	E3	B3	U100A	E3	B0
C316	G2	D1	R130G	C6	B3	U100C	B1	B0
C330	G1	D3	R206A	D4	C0	U100D	B2	B0
C332	G2	D3	R206B	D4	C0	U106	C3	B0
C410	G1	E1	R206C	D4	C0	U110A	B6	B1
C412	G2	E1	R206D	D4	C0	U116	C1	B1
C432	H2	E3	R206E	D4	C0	U120A	C6	B2
C436	G1	E3	R206F	D4	C0	U120B	C4	B2
C440	H1	E4	R210A	D2	C1	U130A	A2	B3
C500	F2	F0	R210B	D2	C1	U130B	D4	B3
C502	F2	F0	R210C	B2	C1	U140A	E4	B4
C514	F1	F1	R210D	D2	C1	U140B	B4	B4
C516	F2	F1	R210E	D2	C1	U140C	A1	A4
C534	F2	F3	R210F	D2	C1	U200	D3	C0
C536	F1	F3	R210G	D2	C1	U206	E3	C0
C540	F1	F4	R226G	B4	C2	U210	D1	C1
C604	G2	G0	R230F	E6	C3	U216	E2	C1
C606	G2	G0	R300D	D4	D0	U220	G5	C2
C620	G1	G2	R300F	B6	D0	U300A	A2	D0
C622	G2	G2	R310D	C6	D1	U300B	E1	D0
C634	G1	G3	R326A	F5	D2	U306A	B2	D0
C636	G2	G3	R336E	E5	D3	U306B	B3	D0
C700	G1	H0	R340F	C5	D4	U316D	D6	D1
C710	G1	H1	R400A	A5	E0	U326D	F5	D2
C720	H2	H2	R400B	A5	E0	U340A	D5	D4
C740	H1	H4	R400C	A6	E0	U340B	D4	E3
CR642	F1	G4	R400D	A5	E0	U340E	C5	D4
F042	H2	A4	R400F	A5	E0	U410B	H4	E1
F046	H1	A4	R400G	A4	E0	U516B	E5	F1
R006C	C3	A0	R406A	C3	E0	U530D	F6	F3
R006D	G5	A0	R406D	C3	E0	U536B	B4	F3
R006E	E3	A0	R406E	C3	E0			
R026	B5	A2	R406F	C3	E0			

P/O A20 ASSY ALSO SHOWN ON ◇9 , ◇10


A
B
C
D
E
F
G
H
1
2
3
4
5
6
U140C 100131
U100C 10102
U026B 68
R100E 68
R126C 68
R100F 68
R106C 68
R100D 68
R100C 68
R126D 68
R210C 68
R110E 68
R006C 68
R106D 68
R006G 68
R006E 68
R130F 68
R106E,F 68
R206C,E 68
R206A,B,D,F 68
R210D,E,F,G 68
R126A,B 68
R406A,D,E,F 68
R520E 100
R520A 100
R400G 100
R400F 100
R400B 100
R400A 100
R400D 100
R400C 100
R226G 68
R026D 68
R026G 68
R026 68
R300F 68
R526D 68
R130G 68
R310D 68
R526C 68
R336E 68
R230F 68
R310C 68
R530C 68
R526A 68
R510E 68
R130D 68
R340F 100
R130E 68
R526B 68
R530F 68
R026F 68
R100A 68
R026E 68
R326A 68
R126G 68
R126F 68
R006D 68
R416C 68
R416F 68
R420E,F,G 68
U126 10016
U116 10145
U106 10145
U210 10016
U200 10016
U206 10113
U216 10113
U100D 10102
U130A 10131
U300A 10103
U306A 10104
U306B 10104
U006A 10104
U100A 10102
U300B 10103
U536B 10103
U026B 10104
U140B 100131
U120B 10131
U340B 100102
U340A 100102
U340E 100102
U036C 10103
U036A 10103
U036B 10103
U110A 10131
U120A 10131
U316D 10103
U5116B 10135
U326D 10102
U220 10016
U036D 10103
U410B 10103
U530D 10104
U130B 10131
U140A 100131
SEGADV
SEGRST
SEGLNG
HOFST
STRT
EOP
TB/8
TRIG LOC
SDM
ERE
WRITE
PGM
TL
TB3
EPOPM
5NS
PTNADV
PTNRST
PTNL
PGM(P)
FRS
DNE
B EOP
DN
SCO
SC1
SC2
SC3
EPPMRD
PCO
PC1
PC2
PC3
RSTA
HOFST
ED0
ED1
ED2
ED3
ED4
ED5
ED6
ED7
-5.2V
-V
-2V
F046 5A
F042 5A
C012 1000µF
C032 1000µF
CR642
R642 470
P/O MAIN INTERCON
BREAKPOINT LOCATOR
PARTITION COUNTER
TP320
TP546
TP706
TYPE | COM | -5.2V | VBB
1664 | 1,16 | 8 |
10010 | 1,16 | 8 |
10016 | 1,16 | 8 |
10102 | 1,16 | 8 |
10103 | 1,16 | 8 |
10104 | 1,16 | 8 |
10113 | 1,16 | 8 |
10131 | 1,16 | 8 |
10133 | 1,16 | 8 |
10135 | 1,16 | 8 |
10145 | 16 | 8 |
10161 | 1,16 | 8 |
10165 | 1,16 | 8 |
10176 | 1,16 | 8 |
10197 | 1,16 | 8 |
10210 | 1,16 | 8 |
100101 | 9,10 | 21 |
100102 | 9,10 | 21 |
100114 | 9,10 | 21 | 22
100131 | 9,10 | 21 |
100141 | 9,10 | 21 |
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2,R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
P/O TIME BASE BD. A20
Static Sensitive Devices
See Maintenance Section
SEQUENCE CONTROL (SN B030707 & BELOW) 8 NLL
7612D
2387-815
REV MAY 1983

TIMEBASE A20
(SN B030708 & UP)

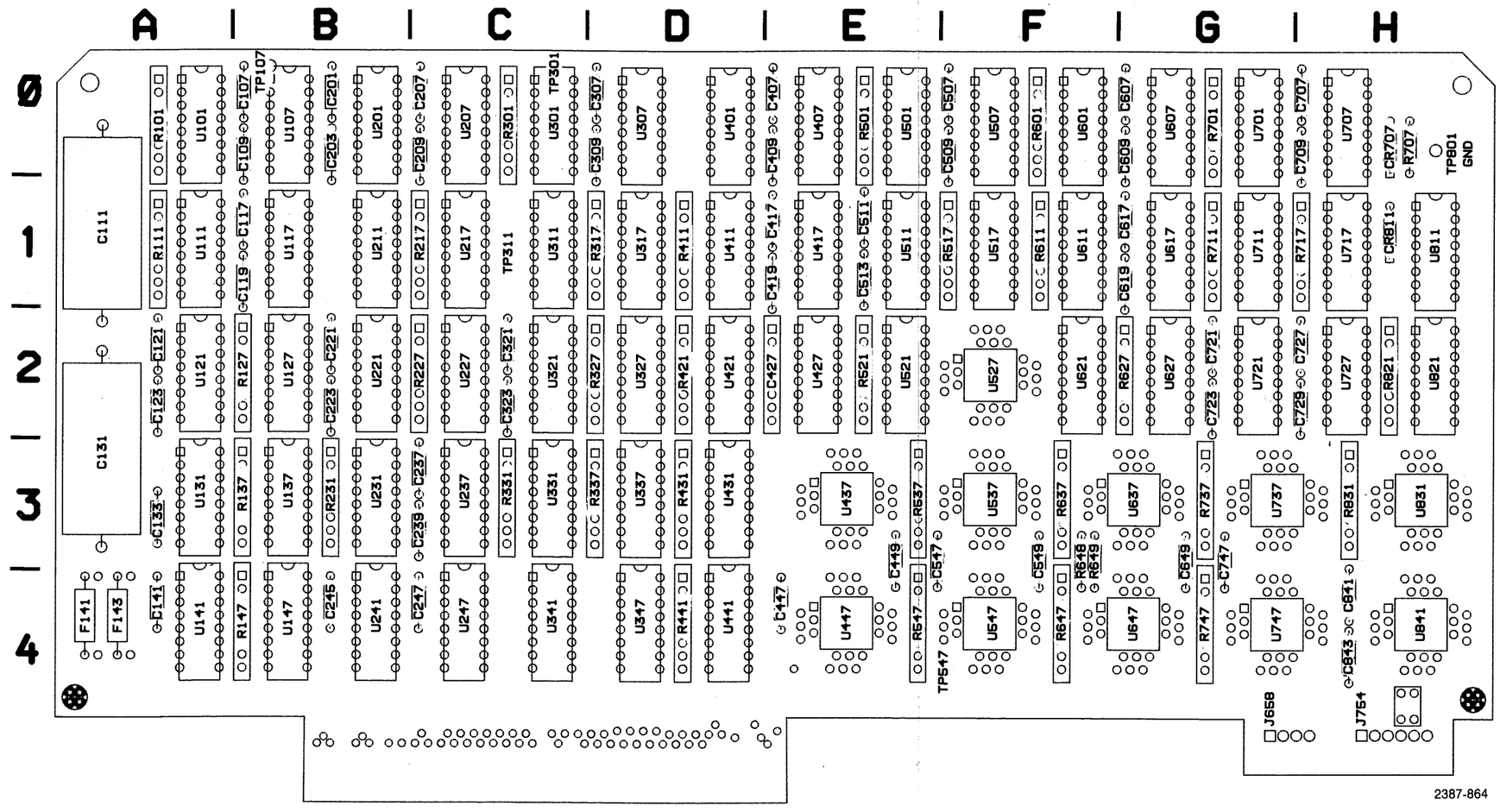
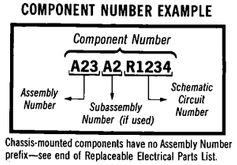


Fig. 8-10. Timebase circuit board, assembly A20 (SN B030708 & up).

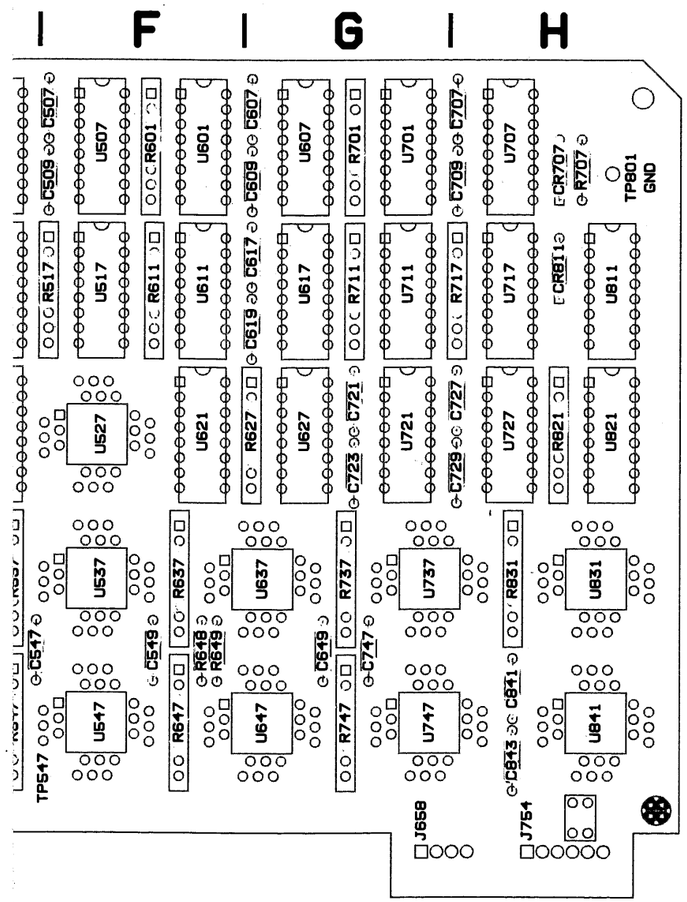
P/O A20 ASSY (SN	
Circuit Number	Sch Lo
C547	
CR702	
CR811	
L851	
R127E	
R127D	
R317D	
R337D	
R411B	
R517F	
R521B	
R521C	
R521D	
R537A	
R601A	
R601C	
R601D	
R601E	
R601F	
R601G	
R611E	
R611G	
R627A	
R627B	
R627C	
R627D	
R627E	
R627F	
R627G	
R637A	
R637F	
R647F	
R648	
R649	
R701B	
R701C	
R701D	
R701E	
R701F	
R701G	
R711A	
R711B	
R711D	

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

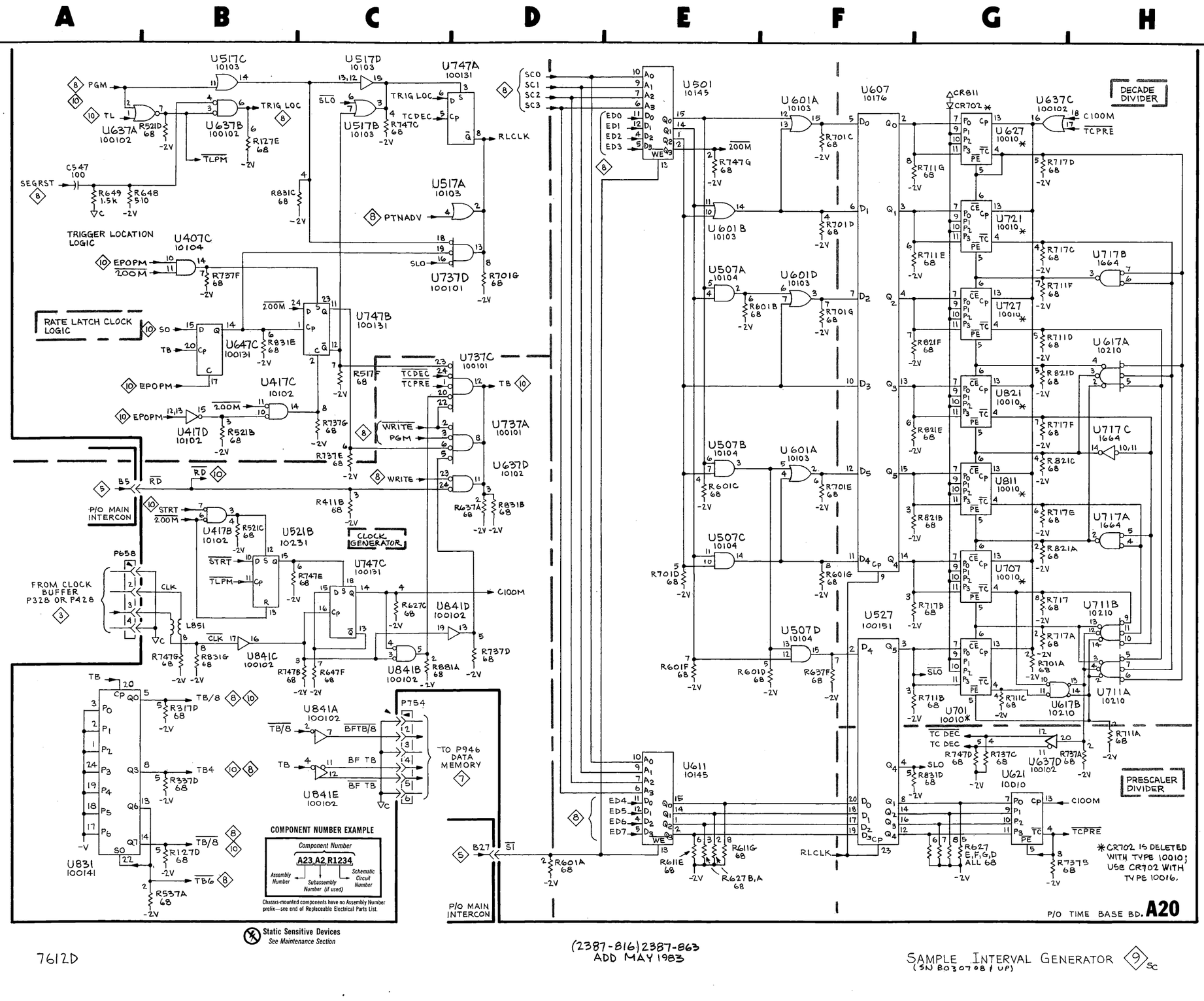


2387-864

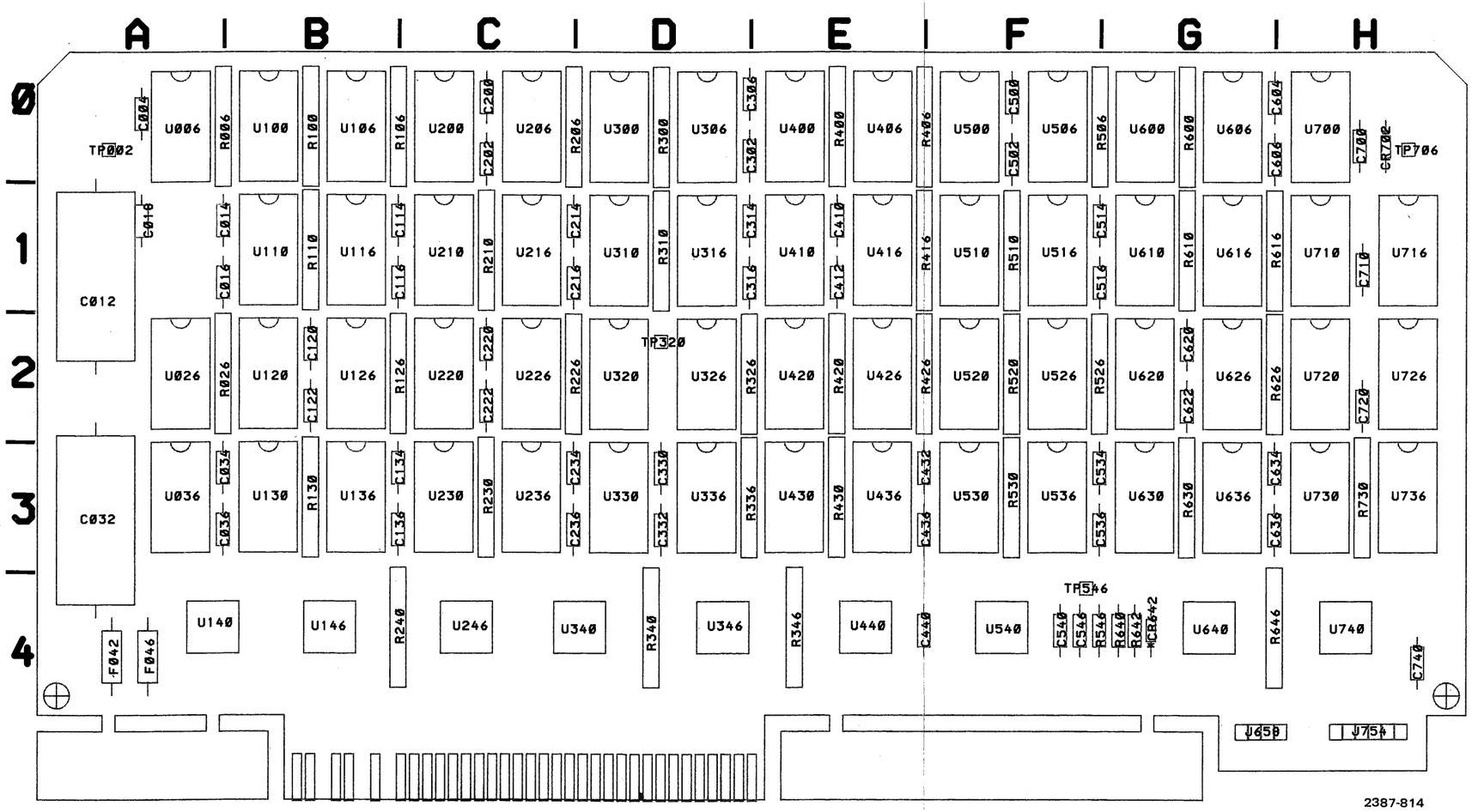
up).

P/O A20 ASSY (SN B030708 & UP)							SEQUENCE CONTROL ◇9◇	
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C547	A1	E3	R711E	G2	G1	U517C	B1	F1
			R711F	H2	G1	U517D	C1	F1
CR702	G1	H1	R711G	G1	G1			
CR811	G1	H1	R717A	G4	H1	U521B	C4	E3
			R717B	G4	H1	U527	F4	F2
L851	B4	H4	R717C	G2	H1	U601A	F3	F0
			R717D	G1	H1	U601B	F2	F0
R127E	B1	B2	R717E	G4	H1	U601C	E2	F0
R127D	B6	B2	R717F	G3	H1	U601D	F1	F0
R317D	B5	D1	R717G	G4	H1	U607	F1	G0
R337D	B5	D3	R737A	H5	G3	U611	E5	F1
R411B	C3	D1	R737B	H6	G3	U617A	H2	G1
R517F	C3	F1	R737C	G5	G3	U617B	H5	G1
R521B	B3	E2	R737D	D4	G3	U621	G5	F2
R521C	B4	E2	R737E	C3	G3	U627	G1	G2
R521D	B1	E2	R737G	C3	G3	U637A	A1	G3
R537A	B6	E3	R747A	E1	G4	U637B	B1	G3
R601A	D6	F0	R747B	C5	G4	U637C	G1	G3
R601C	E3	F0	R747C	C1	G4	U637D	G1	G3
R601D	F5	F0	R747D	G5	G4	U647C	B2	G3
R601E	F2	F0	R747E	C4	G4	U701	G5	G0
R601F	E5	F0	R747F	B2	G4	U707	G4	H0
R601G	F4	F0	R747G	B4	G4	U711A	H5	G0
R611E	E6	E6	R821A	G4	H2	U711B	H4	G0
R611G	E6	F1	R821B	G4	H2	U717A	H4	H1
R627A	E6	G2	R821C	G3	H2	U717B	H2	H1
R627B	E6	G2	R821D	G3	H2	U717C	H3	H1
R627C	C4	G2	R821E	G3	H2	U721	G2	G0
R627D	G6	G2	R821F	G2	H2	U727	G2	H2
R627E	G6	G2	R831A	D5	H3	U737A	D3	G3
R627F	G6	G2	R831B	D3	H3	U737C	D3	G3
R627G	G6	G2	R831C	B1	H3	U737D	D2	G3
R637A	D3	F3	R831D	G5	H3	U747A	D1	G4
R637F	F5	F3	R831E	B2	H3	U747B	C2	G4
R647F	C5	F4	R831G	B4	H3	U747C	C4	G4
R648	B1	F3				U811	G3	H1
R649	A1	F3	U407C	B2	E0	U821	G3	H2
R701B	F1	F0	U417B	B4	E1	U831	A6	H3
R701C	F1	F0	U417C	B3	E1	U841A	C5	H4
R701D	E4	F0	U417D	B3	E1	U841B	C5	H4
R701E	F3	F0	U501	A1	E0	U841C	B4	H4
R701F	F2	F0	U507A	E2	F0	U841D	C5	H4
R701G	D2	F0	U507B	E3	F0	U841D	C5	H4
R711A	H5	G1	U507C	E4	F0			
R711B	G5	G1	U507D	F4	F0			
R711D	G2	G1	U517A	D1	F1			
			U517B	C1	F1			

P/O A20 ASSY ALSO SHOWN ON ◇8◇ , ◇10◇


A
B
C
D
E
F
G
H
1
2
3
4
5
6
U517C 10103
U517D 10103
U747A 100131
PGM
TL
U637A 100102
R521D 68
-2V
U637B 100102
TRIG LOC
R127E 68
TLPM
SLO
U517B 10103
R747C 68
TCDEC
RLCLK
SEGRST
C547 100
R649 1.5k
R648 510
C
U517A 10103
PTNADV
R831C 68
TRIGGER LOCATION LOGIC
U407C 10104
EPOPM
200M
R737F 68
U737D 100101
R701G 68
RATE LATCH CLOCK LOGIC
SO
TB
U647C 100131
R831E 68
U747B 100131
R517F 68
U737C 100101
TCPRE
U417C 10102
R737G 68
U417D 10102
R521B 68
WRITE
PGM
U737A 100101
R737E 68
U637D 10102
RD
B5
R411B 68
R637A 68
R831B 68
P/O MAIN INTERCON
STRT
U417B 10102
R521C 68
U521B 10231
CLOCK GENERATOR
P658
FROM CLOCK BUFFER P328 OR P428
CLK
L851
U747C 100131
R747E 68
R627C 68
C100M
U841D 100102
R737D 68
R747G 68
R831G 68
U841C 100102
R747B 68
R647F 68
U841B 100102
R881A 68
TB/8
R317D 68
TB4
R337D 68
R127D 68
R537A 68
U831 100141
U841A 100102
BFTB/8
TB
BF TB
U841E 100102
P754
TO P946 DATA MEMORY
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2,R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
SC0
SC1
SC2
SC3
U501 10145
ED0
ED1
ED2
ED3
WE
R747G 68
U601A 10103
R701C 68
U601B 10103
R701D 68
U507A 10104
R601B 68
U601D 10103
R701G 68
U507B 10104
R601C 68
U601A 10103
R701E 68
U507C 10104
R701D 68
R601G 68
U507D 10104
R601F 68
R601D 68
R637F 68
U527 100151
SLO
U611 10145
ED4
ED5
ED6
ED7
R601A 68
R611E 68
R611G 68
R627B,A 68
RLCLK
B27
S1
P/O MAIN INTERCON
U607 10176
CR811
CR702
DECADE DIVIDER
U627 10010
R711G 68
U637C 100102
C100M
TCPRE
R717D 68
U721 10010
R711E 68
R717C 68
U717B 1664
R711F 68
U727 10010
R821F 68
R711D 68
U617A 10210
R821D 68
U821 10010
R821E 68
R717F 68
U717C 1664
R821C 68
U811 10010
R821B 68
R717E 68
U717A 1664
R821A 68
U707 10010
R717B 68
R717 68
U711B 10210
R717A 68
R701A 68
U711A 10210
U617B 10210
U701 10010
R711C 68
R711B 68
R711A 68
TC DEC
R747D 68
R737C 68
U637D 100102
R737A 68
U621 10010
R831D 68
PRESCALER DIVIDER
R627 E,F,G,D ALL 68
R737B 68
*CR702 IS DELETED WITH TYPE 10010; USE CR702 WITH TYPE 10016.
P/O TIME BASE BD. A20

TIMEBASE A20
(SN B030707 & BELOW)



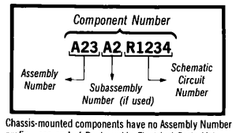
2387-814

Fig. 8-10A. Timebase circuit board, assembly A20 (SN B030707 & below).

P/O A20 ASSY (SN B030707 &	
Circuit Number	Schematic Location
C546	A1
CR702	G1
P658	A4
P754	C5
R006G	B6
R110F	B5
R130A	B1
R130B	B5
R240A	G5
R240A	G6
R240C	C4
R240E	C4
R240G	B2
R300D	C3
R300E	B1
R306*†	F6
R340B	D3
R340C	D3
R346F	C1
R346G	G5
R406C	D6
R428*†	C2
R506B	E2
R506B	E3
R506C	F1
R506D	F2
R506E	E5
R506F	F5
R506G	F2
R526F	C3
R526G	E1
R530E	B5
R546	A1
R600B	G2
R600C	F3
R600D	F4
R600E	E4
R600F	G2
R600G	G1
R610A	E6
R610B	E6
R610C	F5
R610D	F5
R610E	E6
R610F	D2
R610G	E6
R616D	G3
R616F	G2
R616G	G3
R626A	G4
R626C	G4
R626D	G3
R626E	G4
R626F	G5
R626G	G5
R630A	G6
R630B	G6
R630C	G6
R630D	G6
R630E	C3
R630F	C2
R630G	A6
R636*†	C1
R640	A1
R646A	G5

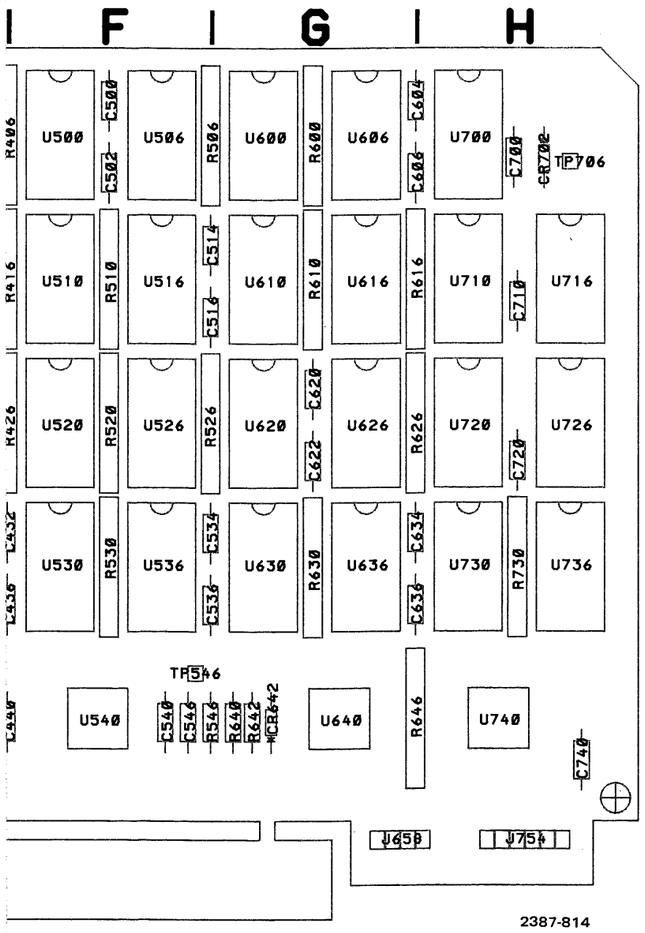
P/O ASS

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



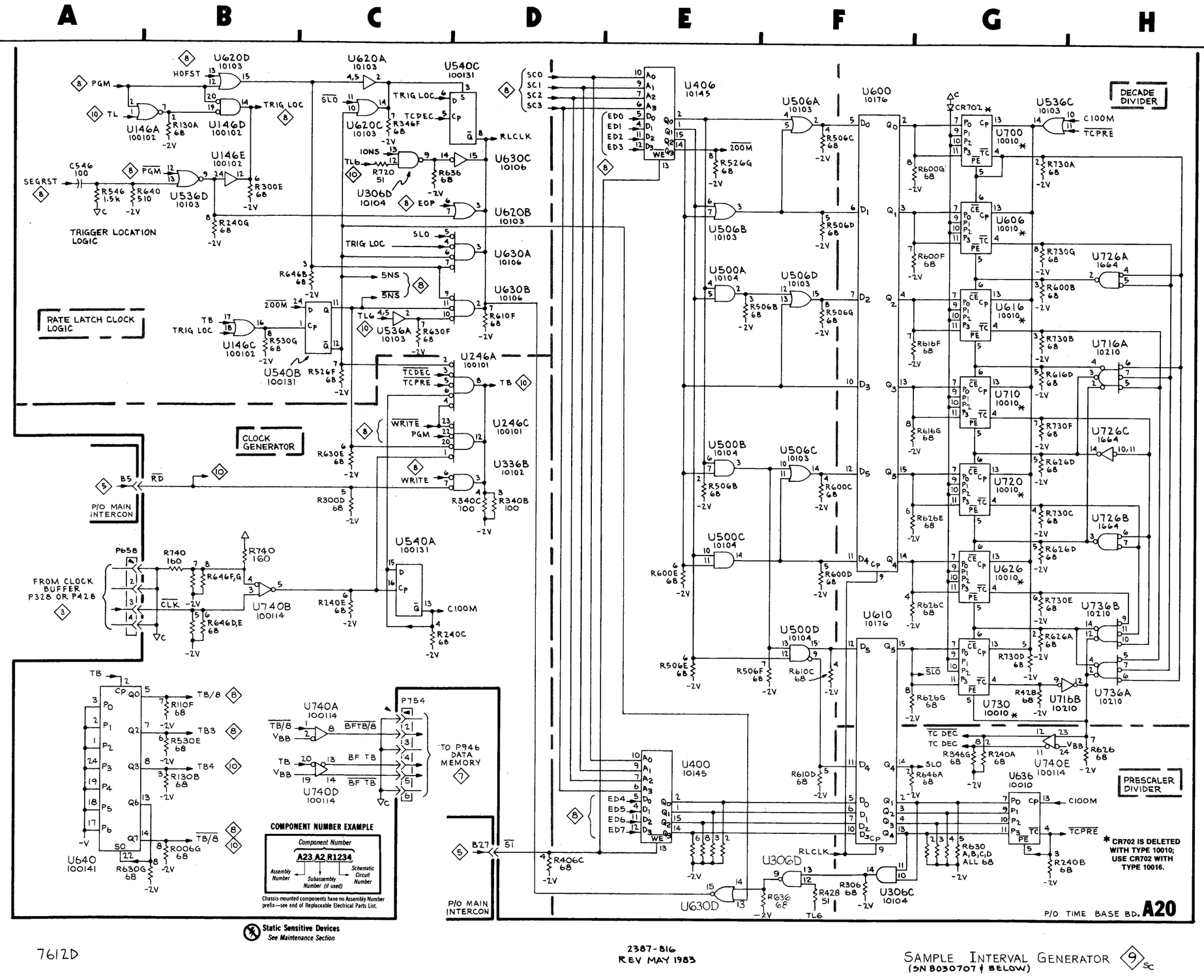
2387-814

)7 & below).

Y 1983

P/O A20 ASSY (SN B030707 & below)	SAMPLE INTERVAL GENERATOR ◇9				
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C546	A1	F4	R646B	C2	G4
CR702	G1	H0	R646D	B4	G4
P658	A4	G4	R646E	B4	G4
P754	C5	H4	R646F	B4	G4
R006G	B6	A0	R646G	B4	G4
R110F	B5	B1	R720*†	G5	H2
R130A	B1	B3	R730A	G1	H3
R130B	B5	B3	R730B	G2	H3
R240A	G5	C4	R730C	G4	H3
R240A	G6	C4	R730D	G5	H3
R240C	C4	C4	R730E	G4	H3
R240E	C4	C4	R730F	G3	H3
R240G	B2	C4	R730G	G2	H3
R300D	C3	D0	R740*†	B4	H4
R300E	B1	D0	U146A	B1	B4
R306*†	F6	D0	U146C	B2	B4
R340B	D3	D4	U146D	B1	B4
R340C	D3	D4	U146E	B1	B4
R346F	C1	D4	U246A	D3	C4
R346G	G5	E4	U246C	D3	C4
R406C	D6	E0	U306C*	G6	D0
R428*†	C2	F2	U306D*	C1	D0
R506B	E2	F0	U336B	D3	D3
R506B	E3	F0	U400	E5	E0
R506C	F1	F0	U406	E1	E0
R506D	F2	F0	U500A	E2	F0
R506E	E5	F0	U500B	E3	F0
R506F	F5	F0	U500C	E4	F0
R506G	F2	F0	U500D	F4	F0
R526F	C3	F2	U506A	F1	F0
R526G	E1	F2	U506B	E2	F0
R530E	B5	F3	U506C	F3	F0
R546	A1	F4	U506D	F2	F0
R600B	G2	G0	U530G	B2	F3
R600C	F3	G0	U536A	C2	F3
R600D	F4	G0	U536C	G1	F3
R600E	E4	G0	U536D	B1	F3
R600F	G2	G0	U540A	C4	F4
R600G	G1	G0	U540B	C2	F4
R610A	E6	G1	U540C	D1	F4
R610B	E6	G1	U600	F1	G0
R610C	F5	G1	U606	G2	G0
R610D	F5	G1	U610	F5	G1
R610E	E6	G1	U616	G2	G1
R610F	D2	G1	U620A	G1	G2
R610G	E6	G1	U620B	D2	G2
R616D	G3	G1	U620C	C1	G2
R616F	G2	G1	U620D	B1	G2
R616G	G3	G1	U626	G4	G2
R626A	G4	G3	U630A	D2	G3
R626C	G4	G2	U630B	D2	G3
R626D	G3	H2	U636	G6	G3
R626E	G4	G2	U640	A5	G4
R626F	G5	G2	U700	G1	H0
R626G	G5	G2	U710	G3	H1
R630A	G6	G3	U716A	H3	H1
R630B	G6	G3	U720	G3	H2
R630C	G6	G3	U726A	H2	H2
R630D	G6	G3	U726B	H4	H2
R630E	C3	G3	U726C	H3	H2
R630F	C2	G3	U730	G5	H3
R630G	A6	G3	U736A	G5	H3
R636*†	C1	G3	U736B	H4	H3
R640	A1	G4	U740A	C5	H4
R646A	G5	G4	U740B	B4	H4
			U740D	C5	H4
			U740E	G5	H4

P/O ASSY ALSO SHOWN ON ◇8 , ◇10


TRIGGER LOCATION LOGIC
RATE LATCH CLOCK LOGIC
CLOCK GENERATOR
DECADE DIVIDER
PRESCALER DIVIDER
P/O MAIN INTERCON
FROM CLOCK BUFFER P328 OR P428
TO P946 DATA MEMORY
COMPONENT NUMBER EXAMPLE
Component Number
A23, A2, R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
* CR702 IS DELETED WITH TYPE 10010; USE CR702 WITH TYPE 10016.
P/O TIME BASE BD. A20

TIMEBASE A20
(SN B030708 & UP)

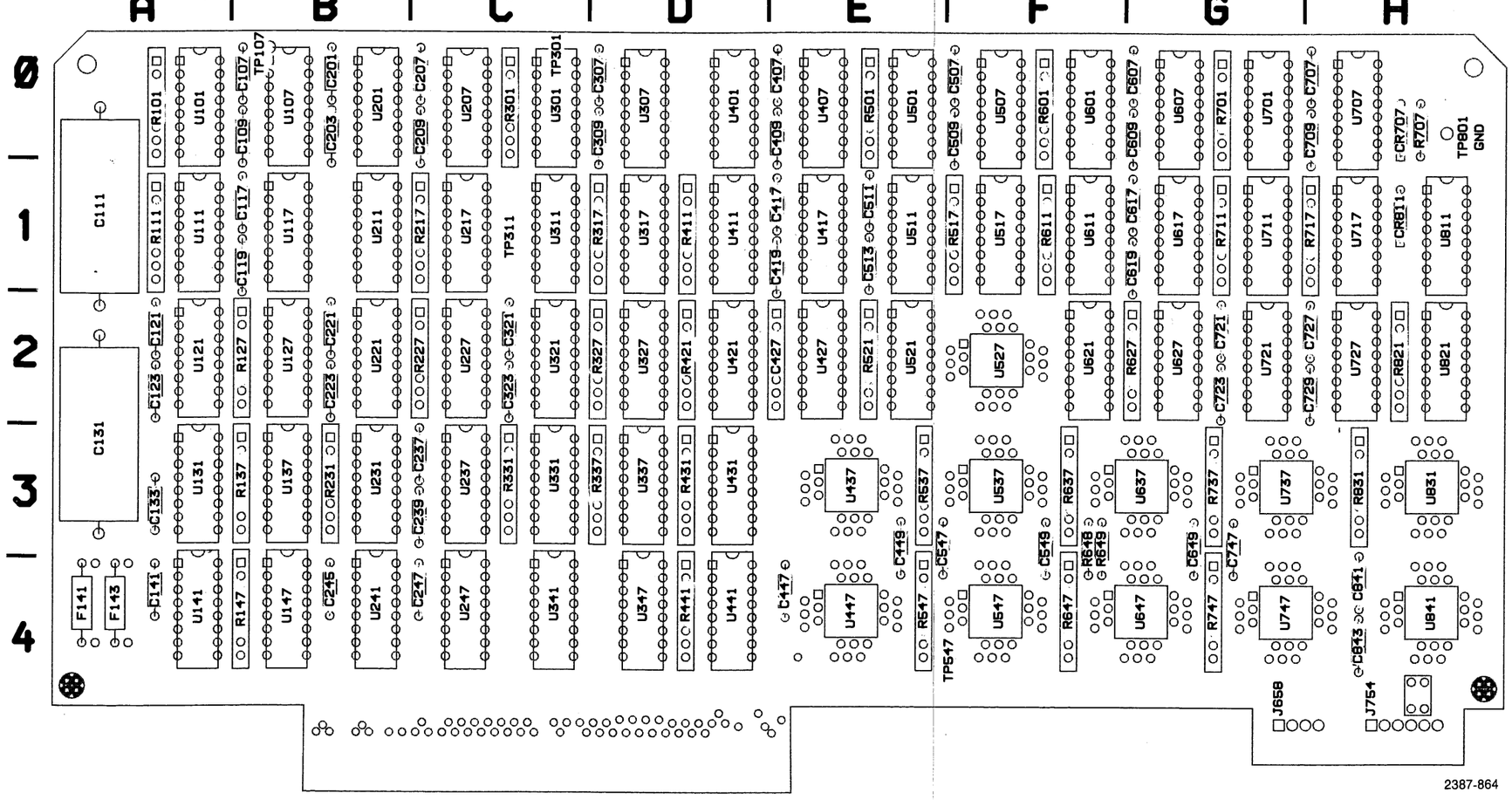
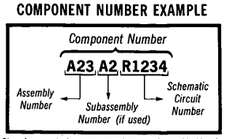


Fig. 8-11. Timebase circuit board, assembly A20 (SN B030708 & up).

P/O A20 ASSY (S	
Circuit Number	S
C449	
R137A	
R137D	
R137E	
R137F	
R137G	
R147C	
R147D	
R147E	
R147E	
R147G	
R231D	
R231E	
R231F	
R301G	
R317E	
R327B	
R327C	
R327D	
R331C	
R331F	
R331G	
R337A	
R337B	
R337C	
R337D	
R411A	
R411D	
R411F	
R421B	
R421C	
R421F	
R421G	
R427C	
R427D	
R427E	
R431A	
R431B	
R431C	
R431D	
R431E	
R431F	
R431G	

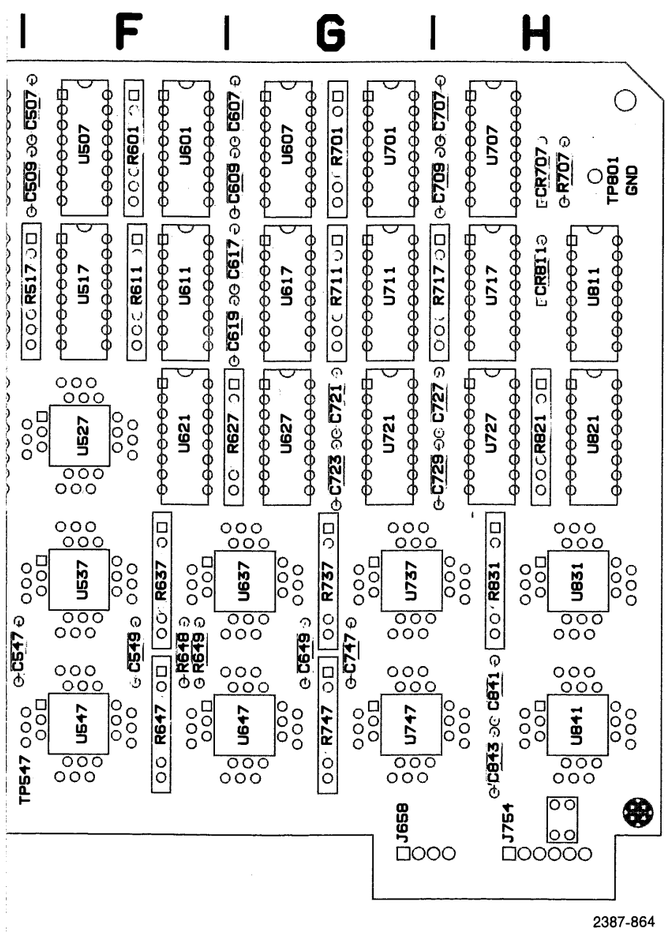
P/O A68 ASSY
R340A
R340B
R340C
R340D
R340E
R340F
R340G
R340H
R340J
R344A
R344B
R344C

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



2387-864

P/O A20 ASSY (SN B030708 & UP) — SEQUENCE CONTROL ◇10

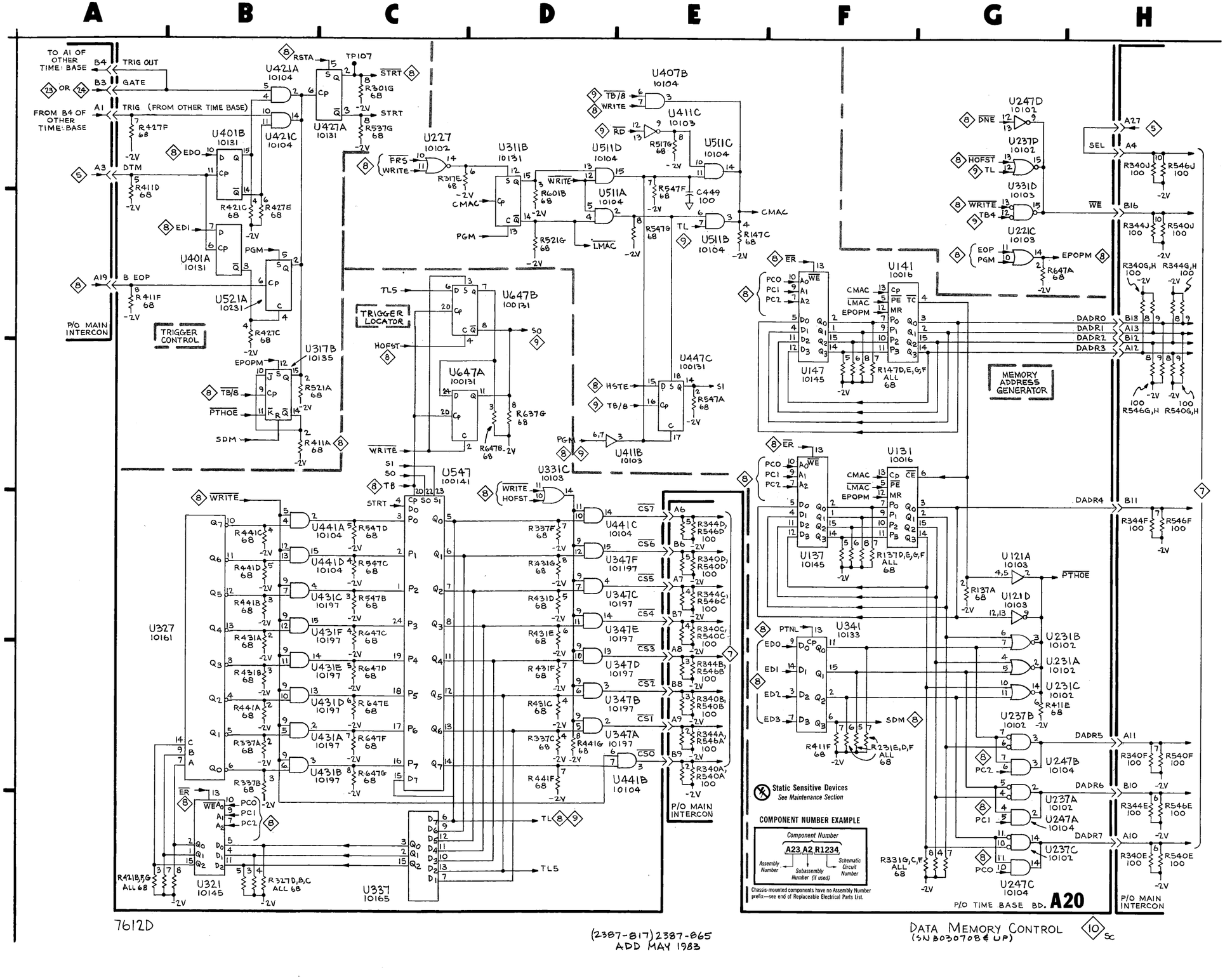
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C449	E2	E3	R441A	B5	D4	U247A	H5	C4
			R441B	B4	D4	U247B	H5	C4
R137A	G4	B3	R441C	B4	D4	U247C	G6	C4
R137D	F4	B3	R441D	B5	D4	U247D	G1	C4
R137E	F4	B3	R441E	G5	D4	U311B	D1	C1
R137F	F4	B3	R441F	D5	D4	U317B	C3	D1
R137G	F4	B3	R441G	D5	D4	U321	B6	C2
R147C	E2	B4	R517G	E1	F1	U327	A4	D2
R147D	F3	B4	R521A	C3	E2	U331C	D3	C3
R147E	F3	B4	R521G	D2	E2	U331D	G1	C3
R147E	F3	B4	R537G	C1	E3	U337	C6	D3
R147G	F3	B4	R547A	E3	E4	U341	F4	C4
R231D	F5	B3	R547B	C4	E4	U347A	E5	D4
R231E	F5	B3	R547C	C4	E4	U347B	E5	D4
R231F	F5	B3	R547D	C4	E4	U347C	E4	D4
R301G	C1	C0	R547F	E2	E4	U347D	E5	D4
R317E	C1	D1	R547G	E2	E4	U347E	E4	D4
R327B	B6	D2	R601B	D2	F0	U347F	E4	D4
R327C	B6	D2	R637G	D3	F3	U401A	B2	D0
R327D	B6	D2	R647A	G2	F4	U401B	B1	D0
R331C	F6	C3	R647B	D3	F4	U407B	E1	E0
R331F	F6	C3	R647C	C4	F4	U411B	E3	E0
R331G	F6	C3	R647D	C5	F4	U411C	E1	E0
R337A	B5	D3	R647E	C5	F4	U421A	B1	D2
R337B	B5	D3	R647F	C5	F4	U421C	B1	D2
R337C	D5	D3	R647G	C5	F4	U427B	C1	E2
R337D	D4	D3				U431A	C5	D3
R411A	C3	D1	TP107	C1	H0	U431B	C5	D3
R411D	A1	D1				U431C	C4	D3
R411F	F5	D1	U121A	G4	A2	U431D	C5	D3
R421B	A6	D2	U121D	G4	A2	U431E	C5	D3
R421C	B2	D2	U131	F3	A3	U431F	C4	D3
R421F	A6	D2	U137	F4	B3	U441A	C4	D4
R421G	A6	D2	U141	F2	A4	U441B	E5	D4
R427C	B2	E2	U147	F3	B4	U441C	E4	D4
R427D	B2	E2	U221C	G2	B2	U441D	C4	D4
R427E	B1	E2	U227C	C1	C2	U447C	E3	E4
R431A	B4	D2	U231A	G5	B3	U511A	D2	E1
R431B	B5	D2	U231B	G4	B3	U511B	E2	E1
R431C	D5	D2	U231C	G5	B3	U511C	E1	E1
R431D	D4	D2	U237A	H5	C3	U511D	D2	E1
R431E	D4	D2	U237B	G5	C3	U521A	B2	E2
R431F	D5	D2	U237C	H5	C3	U547	C3	F4
R431G	D4	D2	U237D	G1	C3	U647A	D3	G3
						U647B	D2	G3

P/O ASSY ALSO SHOWN ON ◇8 , ◇9

P/O A68 ASSY — DATA MEMORY CONTROL ◇10

R340A	E5	D4	R344D	E4	D4	R540G	H3	G4
R340B	E5	D4	R344E	H6	D4	R540H	H3	G4
R340C	E4	D4	R344F	H4	D4	R540J	H2	G4
R340D	E4	D4	R344G	H2	D4	R546A	E5	G4
R340E	H6	D4	R344H	H2	D4	R546B	E5	G4
R340F	H5	D4	R344J	H2	D4	R546C	E4	G4
R340G	H2	D4	R540A	E5	G4	R546D	E4	G4
R340H	H2	D4	R540B	E5	G4	R546E	H6	G4
R340J	H1	D4	R540C	E4	G4	R546F	H4	G4
R344A	E5	D4	R540D	E4	G4	R546G	H3	G4
R344B	E5	D4	R540E	H6	G4	R546H	H3	G4
R344C	E4	D4	R540F	H5	G4	R546J	H1	G4

A68 ASSY SHOWN IN FIG. 8-31

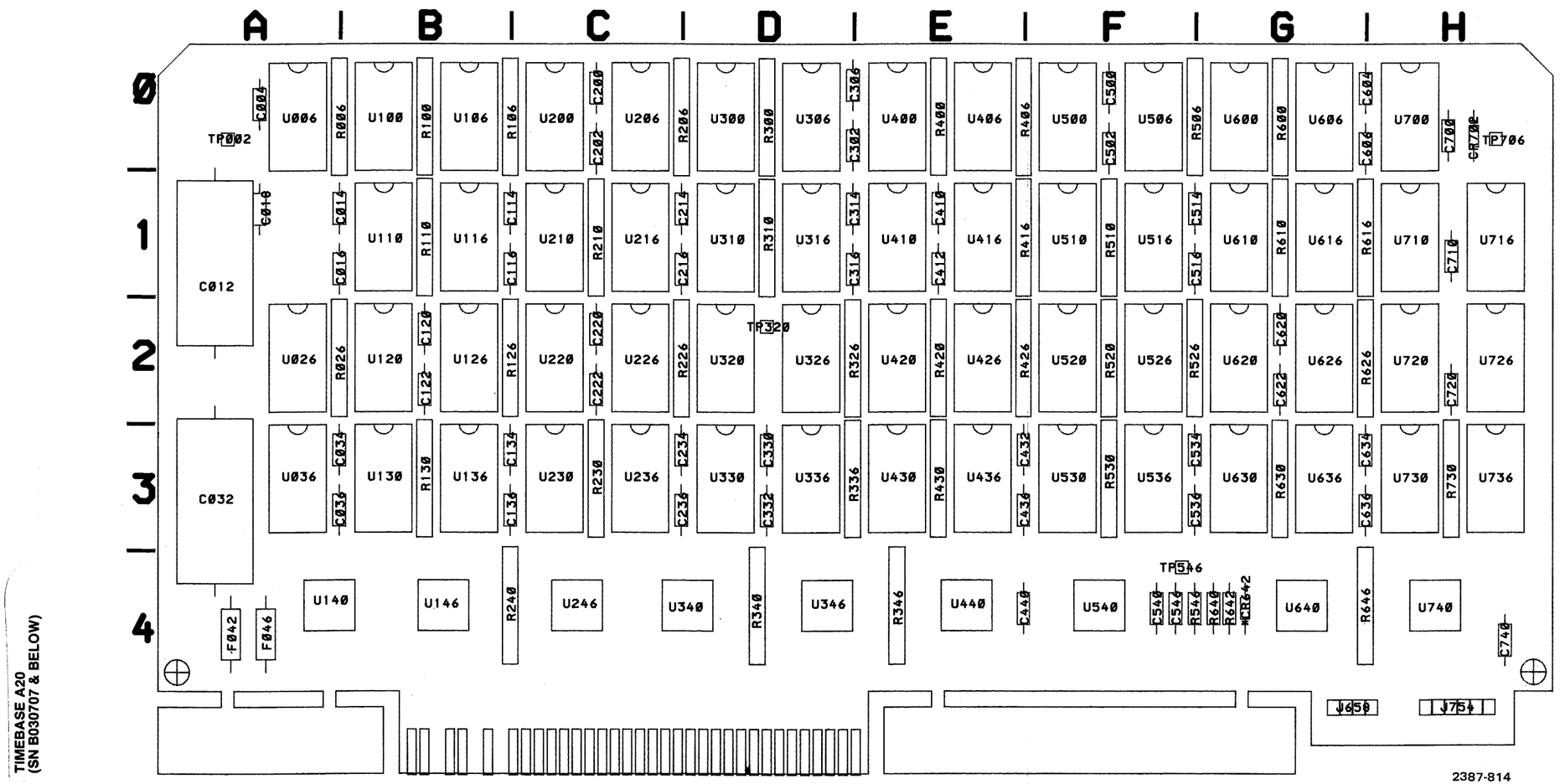


7612D

(2387-817) 2387-865
ADD MAY 1983

DATA MEMORY CONTROL
(SN B030708 & UP)
10 5C

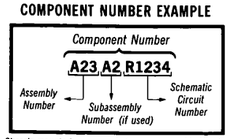
DATA MEMORY CONTROL
(SN B030708 & UP)
10



TIMEBASE A20
(SN B030707 & BELOW)

Fig. 8-11A. Timebase circuit board, assembly A20 (SN B030707 & below).

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

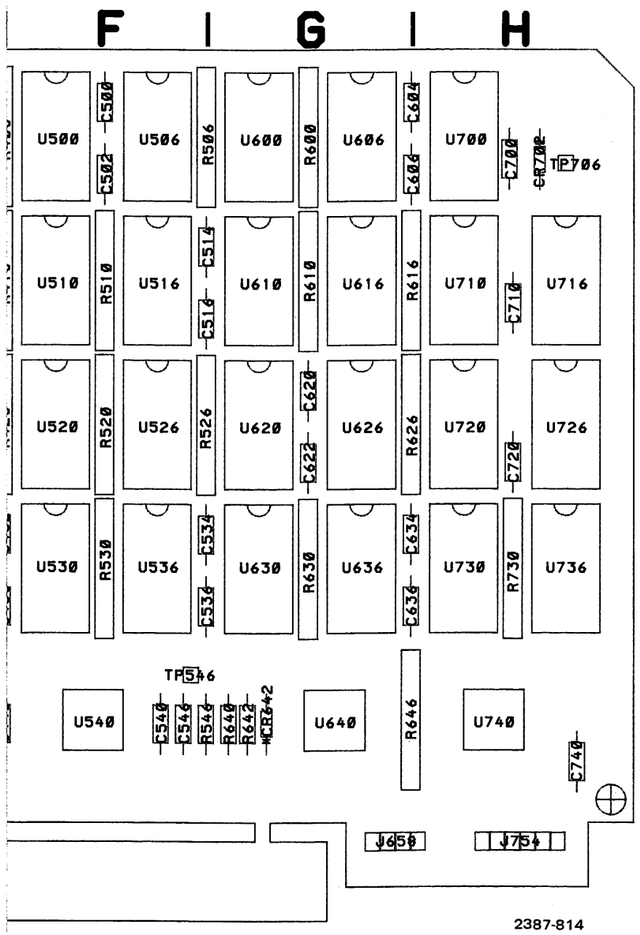
P/O A20 ASSY (SN B030707 & below)

Circuit Number	Schematic Location	Board Location
C018	C2	A1
R006B	C1	A0
R006G	D2	A0
R026A	D4	A2
R110A	F5	B1
R110B	C2	B1
R110D	D3	B1
R110G	E3	B1
R126E	E3	B2
R130C	G2	B3
R206G	C1	C0
R226A	F4	C2
R226C	D2	C2
R226D	F4	C2
R226E	F4	C2
R226F	F4	C2
R230A	F5	C3
R230B	F3	C3
R230C	F3	C3
R230D	F3	C3
R230E	F3	C3
R240D	E1	C4
R310A	G4	D1
R310G	C1	D1
R326B	B4	D2
R326C	B5	D2
R326D	B5	D2
R326E	B4	D2
R326F	B4	D2
R326G	F5	D2
R336A	G6	D3
R336B	B5	D3
R336C	G6	D3
R336D	F5	D3
R336F	G6	D3
R336G	D5	D3
R340A	D4	E3
R340D	C3	D4
R340E	C3	D4
R346A	C3	E4
R346B	F1	E4
R346C	E1	E4
R346D	E1	E4
R346E	F2	E4
R416A	A6	E1
R416B	A6	E1
R416E	A1	E1
R416G	A6	E1

P/O A

P/O A68 ASSY

R340A	E5	D4
R340B	E5	D4
R340C	E4	D4
R340D	E4	D4
R340E	H6	D4
R340F	H5	D4
R340G	H2	D4
R340H	H2	D4
R340J	H1	D4
R344A	E5	D4
R344B	E5	D4
R344C	E4	D4



2387-814

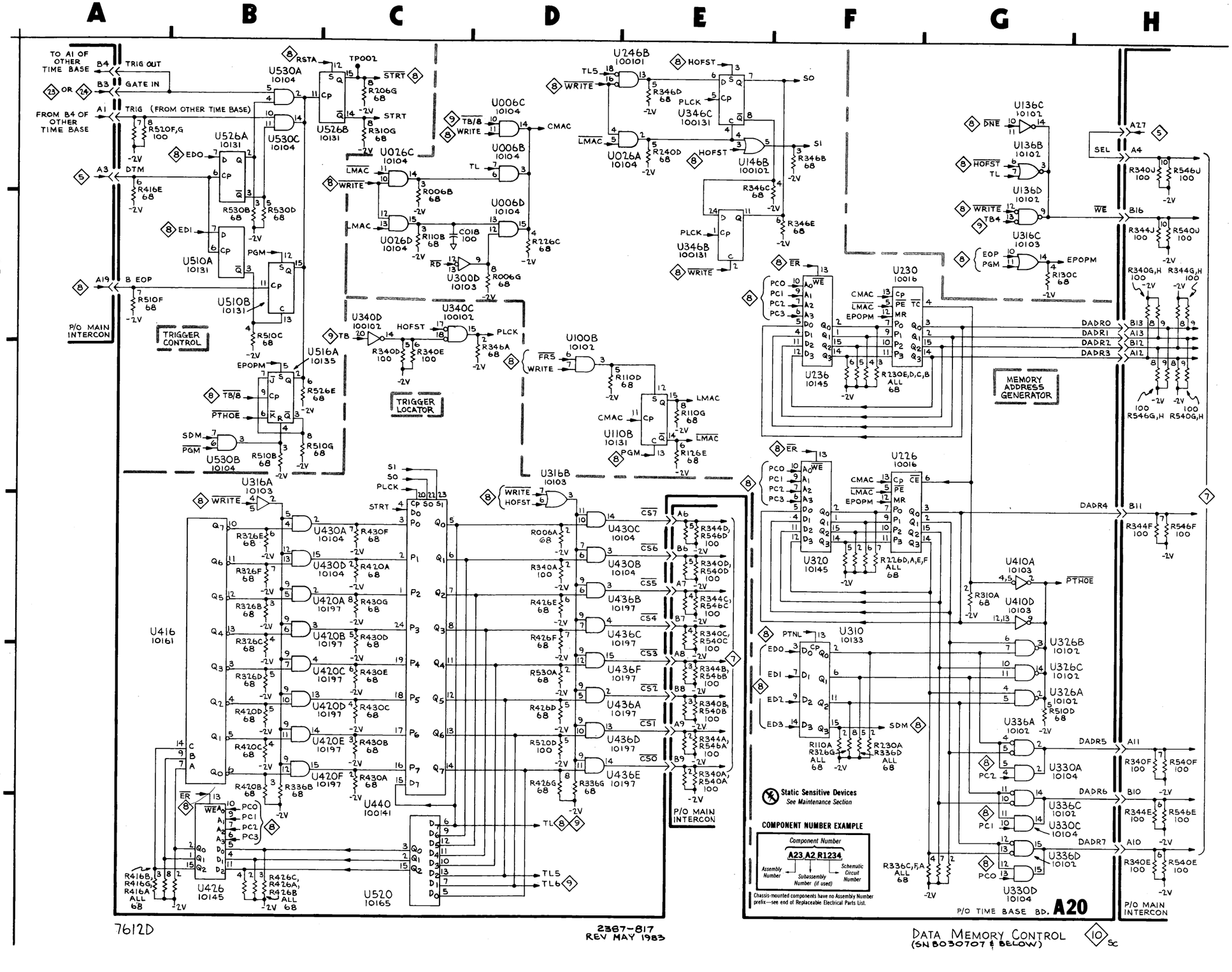
07 & below).

P/O A20 ASSY (SN B030707 & below)					DATA MEMORY CONTROL ◇10			
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C018	C2	A1	R420A	C4	E2	U310	F5	D1
R006B	C1	A0	R420B	B5	E2	U316A	B4	D1
R006G	D2	A0	R420C	B5	E2	U316B	D4	D1
R026A	D4	A2	R420D	B5	E2	U316C	G2	D1
R110A	F5	B1	R426A	B6	E2	U320	F4	D2
R110B	C2	B1	R426B	B6	E2	U326A	G5	D2
R110D	D3	B1	R426C	B6	E2	U326B	G5	D2
R110G	E3	B1	R426D	D4	E2	U326C	G5	D2
R126E	E3	B2	R426E	D4	E2	U330A	G5	D3
R130C	G2	B3	R426F	D4	E2	U330C	G6	D3
R206G	C1	C0	R426G	D5	E2	U330D	G6	D3
R226A	F4	C2	R430A	C5	E3	U336A	G5	D3
R226C	D2	C2	R430B	C5	E3	U336C	G6	D3
R226D	F4	C2	R430C	C5	E3	U336D	G6	D3
R226E	F4	C2	R430D	C4	E3	U340A	B4	E3
R226F	F4	C2	R430E	C5	E3	U340C	C2	D4
R230A	F5	C3	R430F	C4	E3	U340D	C2	D4
R230B	F3	C3	R430G	C4	E3	U346B	E2	D4
R230C	F3	C3	R510B	B3	F1	U346C	E1	D4
R230D	F3	C3	R510C	B2	F1	U410A	G4	E1
R230E	F3	C3	R510D	G5	F1	U410D	G4	E1
R240D	E1	C4	R510F	A2	F1	U416	B4	E1
R310A	G4	D1	R510G	B3	F1	U420A	B4	E2
R310G	C1	D1	R520	D5	F2	U420B	B4	E2
R326B	B4	D2	R520F	A1	F2	U420C	B5	E2
R326C	B5	D2	R520G	A1	F2	U420D	B5	E2
R326D	B5	D2	R526E	B3	F3	U420E	B5	E2
R326E	B4	D2	R530A	D4	F3	U420F	B5	E2
R326F	B4	D2	R530B	B2	F3	U426	B6	E2
R326G	F5	D2	R530D	B2	F3	U430B	D4	E3
R336A	G6	D3	TP002	C1	A0	U430C	D4	E3
R336B	B5	D3	U006B	D1	A0	U430D	B4	E3
R336C	G6	D3	U006C	D1	A0	U436A	D5	E3
R336D	F5	D3	U006D	D2	A0	U436B	D4	E3
R336F	G6	D3	U026A	D1	A2	U436C	D4	E3
R336G	D5	D3	U026C	C1	A2	U436D	D5	E3
R340A	D4	E3	U026D	C2	A2	U436E	D5	E3
R340D	C3	D4	U026D	C2	A2	U436F	D5	E3
R340E	C3	D4	U100B	D3	B0	U440	C5	E4
R346A	C3	E4	U110B	E3	B1	U510A	B2	F1
R346B	F1	E4	U136B	G1	B3	U510B	B2	F1
R346C	E1	E4	U136C	G1	B3	U516A	B3	F1
R346D	E1	E4	U136D	G1	B3	U520	C6	F2
R346E	F2	E4	U146B	E1	B4	U526A	B1	F2
R416A	A6	E1	U226	F3	C2	U526B	C1	F2
R416B	A6	E1	U230	F2	C3	U530A	B1	F3
R416E	A1	E1	U236	F3	C3	U530B	B3	F3
R416G	A6	E1	U246B	D1	C4	U530C	B1	F3

P/O A20 ASSY ALSO SHOWN ON ◇8 , ◇9

P/O A68 ASSY						DATA MEMORY CONTROL ◇10		
R340A	E5	D4	R344D	E4	D4	R540G	H3	G4
R340B	E5	D4	R344E	H6	D4	R540H	H3	G4
R340C	E4	D4	R344F	H4	D4	R540J	H2	G4
R340D	E4	D4	R344G	H2	D4	R546A	E5	G4
R340E	H6	D4	R344H	H2	D4	R546B	E5	G4
R340F	H5	D4	R344J	H2	D4	R546C	E4	G4
R340G	H2	D4	R540A	E5	G4	R546D	E4	G4
R340H	H2	D4	R540B	E5	G4	R546E	H6	G4
R340J	H1	D4	R540C	E4	G4	R546F	H4	G4
R344A	E5	D4	R540D	E4	G4	R546G	H3	G4
R344B	E5	D4	R540E	H6	G4	R546H	H3	G4
R344C	E4	D4	R540F	H5	G4	R546J	H1	G4

A68 ASSY SHOWN IN FIG. 8-31



7612D

2387-817
REV MAY 1983

DATA MEMORY CONTROL
(SN B030707 & BELOW)
10 SC

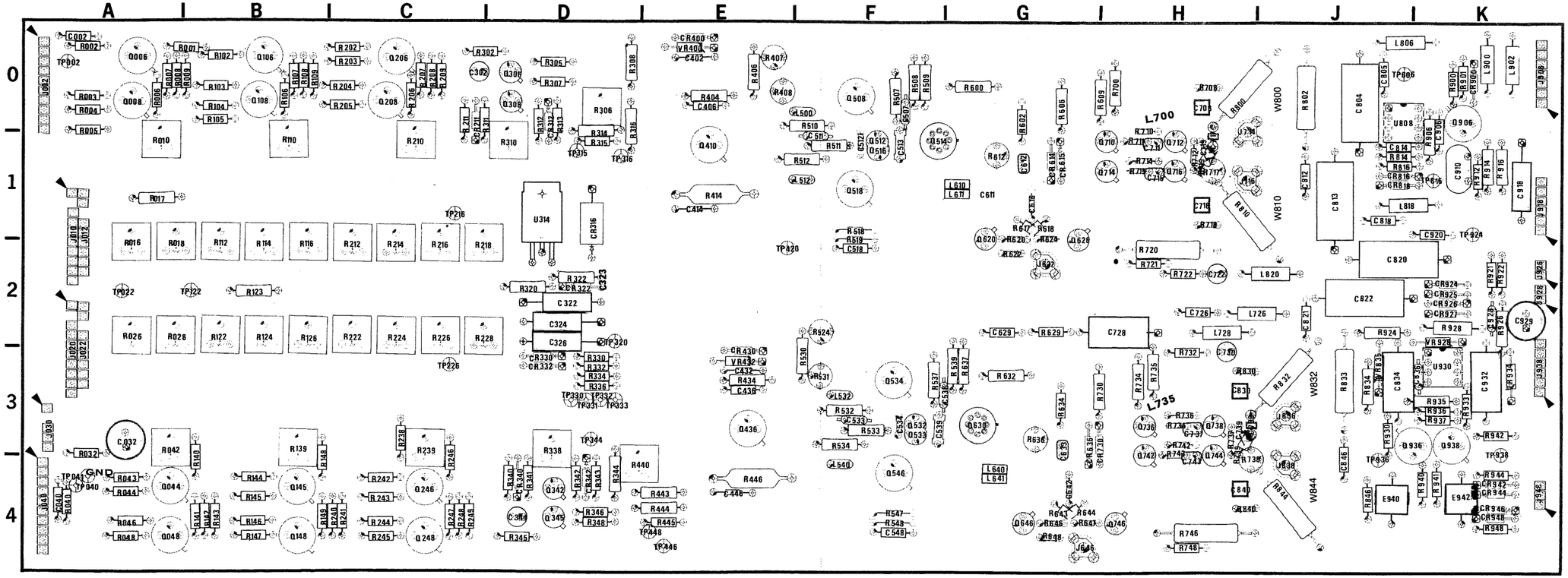


Fig. 8-12a. Deflection Amplifier circuit board, assembly A26.

2387-818

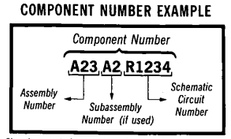
Fig. 8-1

†Located on back board.

P/O A68 ASSY			VERTICAL AMPLIFIER ◇11		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
P520	E6	G2	—	—	—
A68 ASSY SHOWN IN FIG. 8-31					

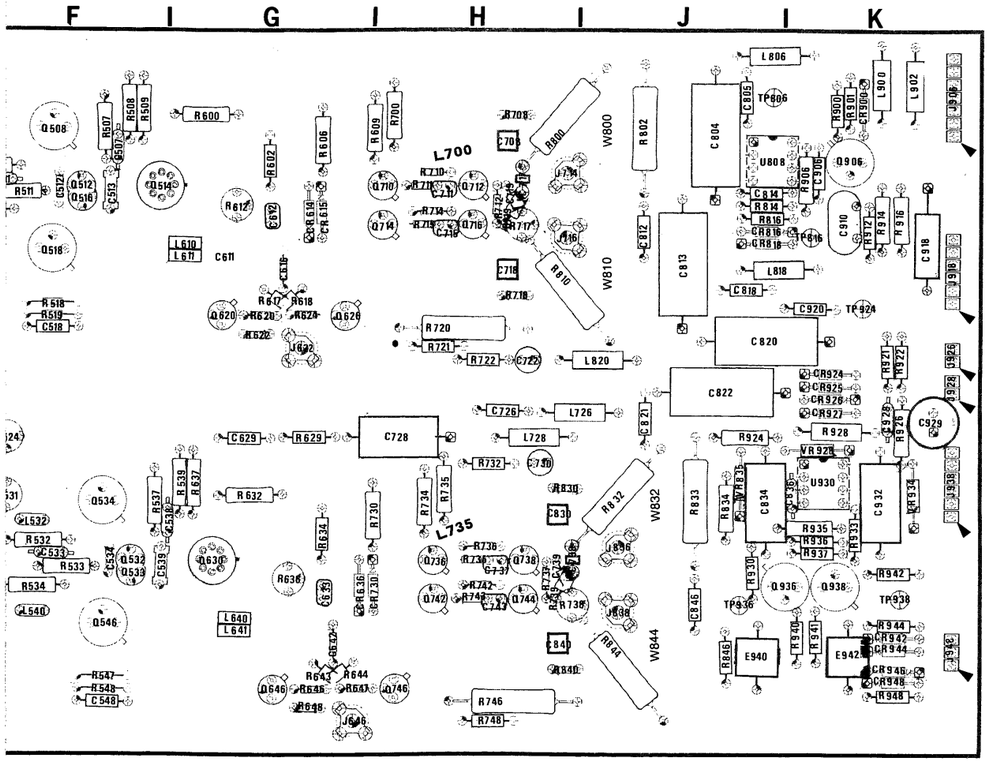
P/O A26 ASSY (cont.)			VERT
Circuit Number	Schematic Location	Board Location	Circuit Number
R643	C4	G4	R737
R644	C5	G4	R738
R646	C4	G4	R739
R647	C5	G4	R742
R648	C4	G4	R743
R700	B2	H0*	R746
R708	A2	H0	R748
R710	B3	H1	R800
R711	B3	H1	R802
R712	A2	H1	R810
R714	B1	H1	R830
R715	B1	H1	R832
R717	B2	H1	R833
R718	A1	H1	R840
R719	A2	H1	R844
R720	B2	H2	TP420
R721	C2	H2	U5015
R722	D6	H2	U5040
R730	D4	H3	VR400
R732	D6	H3	VR432
R734	B5	H3*	W800
R735	B4	H3*	W810
R735	B6	H3	W832
R736	B5	H3	W844
P/O A26 ASSY ALSO SHOWN ON ◇4			

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

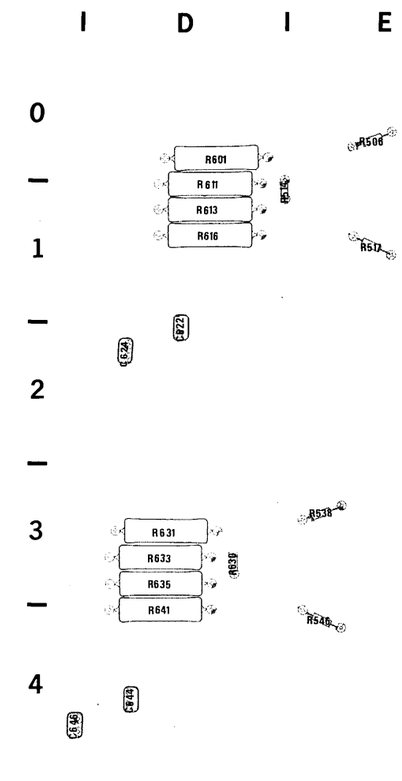


2387-818

it board, assembly A26.

		VERTICAL AMPLIFIER ◇11		
Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
E6	G2	—	—	—

A68 ASSY SHOWN IN FIG. 8-31



2387-818

Fig. 8-12b. Rear-mounted components.

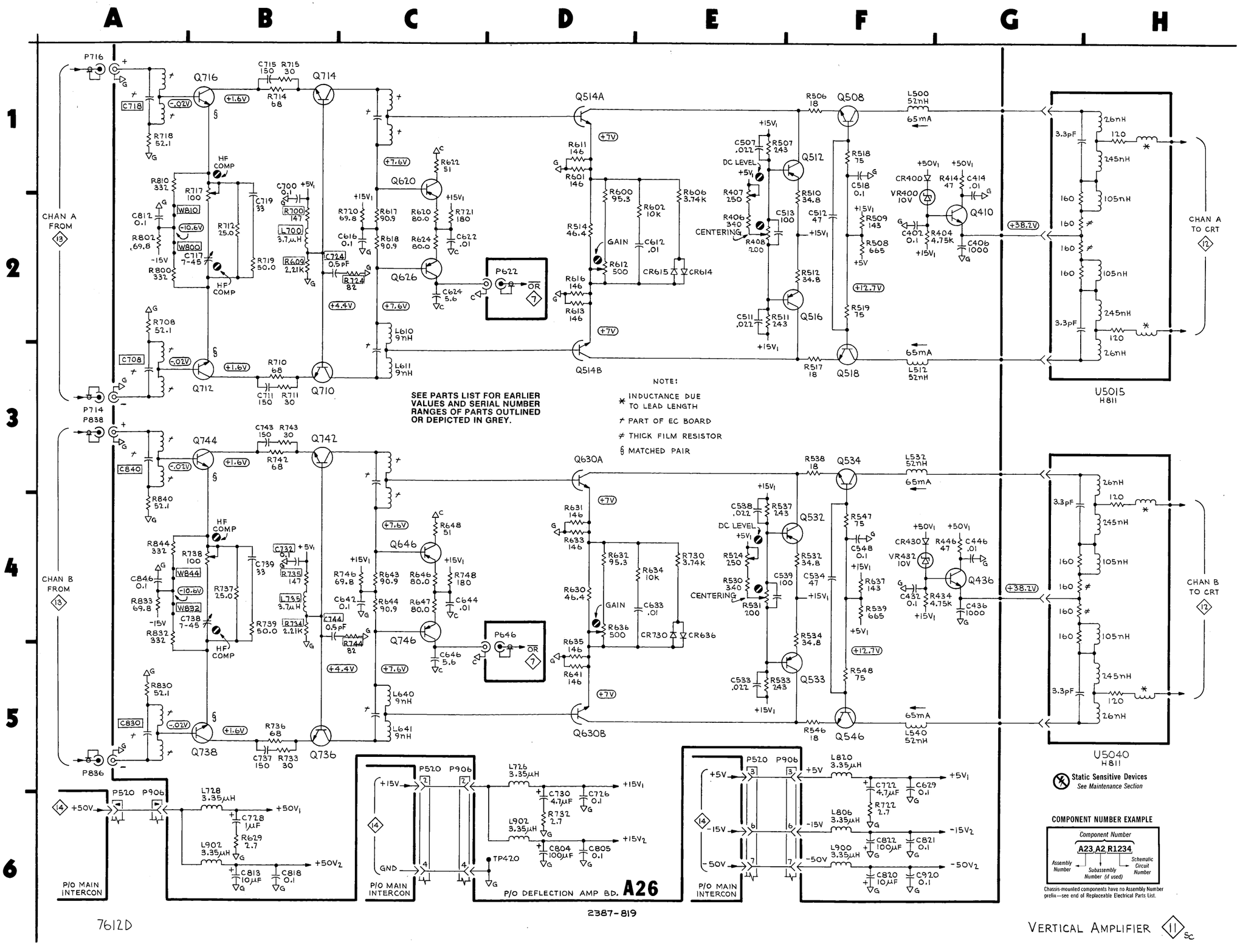
†Located on back of board.

*See Parts List for serial number ranges.

P/O A26 ASSY (cont.)		VERTICAL AMPLIFIER ◇11			
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
R643	C4	G4	R737	A4	H3
R644	C5	G4	R738	B4	H3
R646	C4	G4	R739	A5	H3
R647	C5	G4	R742	B4	H3
R648	C4	G4	R743	B3	H1
R700	B2	H0*	R746	B4	A4
R708	A2	H0	R748	C4	H4
R710	B3	H1	R800	B2	J0
R711	B3	H1	R802	B2	J0
R712	A2	H1	R810	B2	J1
R714	B1	H1	R830	A5	H3
R715	B1	H1	R832	B5	J3
R717	B2	H1	R833	B5	J3
R718	A1	H1	R840	A4	H4
R719	A2	H1	R844	B4	J4
R720	B2	H2	TP420	D6	E2
R721	C2	H2	U5015	G3	CHASSIS
R722	D6	H2	U5040	G5	CHASSIS
R730	D4	H3	VR400	F2	E0
R732	D6	H3	VR432	F4	E3
R734	B5	H3*	W800	A2	J0*†
R735	B4	H3*	W810	A2	J1*†
R735	B6	H3	W832	A4	J3*†
R736	B5	H3	W844	A4	J4*†

P/O A26 ASSY ALSO SHOWN ON ◇4 , ◇12

P/O A26 ASSY		VERTICAL AMPLIFIER ◇11			
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C402	F2	E0	P906	E6	K0
C406	F2	E0	Q410	F2	E1
C414	F2	E1	Q436	F4	E3
C432	F5	E3	Q508	F1	F0
C436	F5	E3	Q512	E1	F1
C446	F4	E4	Q514	D1	F1
C507	E1	F0	Q514	D3	F1
C511	E2	F1	Q516	E2	F1
C512	E2	F1	Q518	F3	F1
C513	E2	F1	Q532	E4	F3
C518	F1	F2	Q533	E5	F3
C533	E5	F3	Q534	F4	F3
C534	E4	F3	Q546	F5	F4
C538	E4	F3	Q620	C2	G2
C539	E5	F3	Q626	C2	G2
C548	F4	F4	Q630	D4	G3
C612	D2	G1	Q630	D5	G3
C616	B2	G1	Q646	C4	G4
C622	C2	D2†	Q710	B3	H1
C624	C2	D2†	Q712	A3	H1
C629	D6	G2	Q714	B1	H1
C633	D5	G3	Q716	A1	H1
C642	B5	G4	Q736	B6	H3
C644	C5	D4†	Q738	A5	H3
C646	C5	H4†	Q742	B4	H3
C708	A3	H0	Q744	A4	H3
C711	B3	H1	Q746	C5	H4
C715	B1	H1	R404	F2	E0
C717	B2	H1	R406	E2	E0
C718	A1	H1	R407	E2	E0
C719	A2	H1	R408	E2	E0
C722	D6	H1	R414	F2	E1
C726	D6	H2	R434	F5	E3
C728	C6	H2	R446	F4	E4
C730	D6	H3	R506	E1	E0†
C737	B6	H3	R507	E1	F0
C738	B5	H3	R508	F2	F0
C739	A4	H3	R509	F2	F0
C743	B3	H4	R510	E2	F1
C804	D6	J0	R511	E2	F1
C805	D6	J0	R512	E2	F1
C812	B2	H1	R514	D2	D1†
C813	C6	J1	R517	E3	E1†
C818	C6	J1	R518	F1	F1
C820	E6	J1	R519	F2	F2
C821	D6	J2	R524	E4	F2
C822	D6	J2	R530	E4	F3
C830	A5	H3	R531	E5	F3
C840	A4	H4	R532	E4	F3
C846	B4	J4	R533	E5	F3
C920	E6	K1	R534	E5	F3
CR400	F2	E0	R537	E4	F3
CR430	F4	E3	R538	E4	E3†
CR614	D2	G1	R539	F5	G3
CR615	D2	G1	R546	E5	E4†
CR636	D5	G3	R547	F4	F4
CR730	D5	G3	R548	F5	F4
L500	F1	F0	R600	D2	G0
L512	F3	F1	R601	D1	D1†
L532	F4	F3	R602	D2	G0
L540	F5	F4	R606	D2	G0
L610	C3	G1	R609	B2	H0*
L611	C3	G1	R611	D1	D1†
L640	C5	G4	R612	D2	G1*
L641	C5	G4	R613	D2	D1†
L700	B2	H0*	R616	D2	D1†
L726	C6	J2	R617	C2	G1
L728	C6	H2	R618	C2	G1
L735	B4	H3*	R620	C2	G2
L806	D6	J1	R622	C1	G2
L818	C6	J1	R624	C2	G2
L820	D6	J2	R629	C6	G2
L900	E6	K0	R630	D4	D3†
L902	D6	K0	R631	D4	C3†
P622	C2	G2	R632	D4	G3
P646	C5	G4	R633	D4	C3†
P714	A3	H1	R634	D4	G3
P716	A1	H1	R635	D5	D3†
P836	A6	J3	R636	D5	G3*
P838	A3	J3	R637	F4	G3
			R641	D5	D4†


A
B
C
D
E
F
G
H
1
2
3
4
5
6
P716
Q716
Q714
C715 150
R715 30
R714 68
C718
-.02V
+1.6V
R718 52.1
HF COMP
R810 332
R717 100
C719 33
C812 0.1
W810
-10.6V
R712 25.0
R719 50.0
R802 69.8
W800
C717 7-45
-15V
R800 332
HF COMP
C700 0.1
+5V1
R700 47
L700 3.7µH
R609 2.21K
C724 0.5pF
R724 82
+15V1
R720 69.8
R617 90.9
R618 90.9
C616 0.1
+7.6V
Q620
R622 51
R620 80.0
R624 80.0
Q626
C622 .01
C624 5.6
+4.4V
P622
OR
7
CHAN A FROM
13
Q514A
Q514B
+7V
R611 146
R601 146
R600 95.3
R602 10K
R606 3.74K
R514 46.4
GAIN
R612 500
C612 .01
CR615
CR614
R616 146
R613 146
R506 18
Q508
L500 52nH
65mA
+15V1
C507 .022
R507 243
DC LEVEL
+5V
Q512
R407 250
R406 340
CENTERING
R408 200
C513 100
R510 34.8
C512 47
R518 75
C518 0.1
+15V1
R509 143
R508 665
+5V
+12.7V
R519 75
Q516
R512 34.8
C511 .022
R511 243
+15V1
R517 18
Q518
65mA
L512 52nH
+50V1
CR400
VR400 10V
R414 47
C414 .01
Q410
C407 0.1
R404 4.75K
C406 1000
+38.2V
3.3pF
26nH
120
245nH
105nH
160
CHAN A TO CRT
12
U5015
H811
L708 9nH
L610 9nH
L611 9nH
C708
R708 52.1
Q712
Q710
R710 68
C711 150
R711 30
P714
P838
C840
R840 52.1
Q744
Q742
C743 150
R743 30
R742 68
HF COMP
R844 332
R738 100
C739 33
C846 0.1
W844
-10.6V
R737 25.0
R833 69.8
W832
C738 7-45
-15V
R832 332
HF COMP
C732 0.1
+5V1
R735 147
L735 3.7µH
R734 2.21K
C744 0.5pF
R744 82
+15V1
R746 69.8
R643 90.9
R644 90.9
C642 0.1
+7.6V
Q646
R648 51
R646 80.0
R647 80.0
Q746
C644 .01
C646 5.6
+4.4V
P646
OR
7
CHAN B FROM
13
Q630A
Q630B
+7V
R631 146
R633 146
R632 95.3
R634 10K
R730 3.74K
R630 46.4
GAIN
R636 500
C633 .01
CR730
CR636
R635 146
R641 146
R538 18
Q534
L532 52nH
65mA
+15V1
C538 .022
R537 243
DC LEVEL
+5V1
Q532
R524 250
R530 340
CENTERING
R531 200
C539 100
R531 34.8
C534 47
R547 75
C548 0.1
+15V1
R537 143
R539 665
+5V1
+12.7V
R548 75
Q533
R534 34.8
C533 .022
R533 243
+15V1
R546 18
Q546
65mA
L540 52nH
+50V1
CR430
VR432 10V
R446 47
C446 .01
Q436
C432 0.1
R434 4.75K
C436 1000
+38.2V
3.3pF
26nH
120
245nH
105nH
160
CHAN B TO CRT
12
U5040
H811
L640 9nH
L641 9nH
C830
R830 52.1
Q738
Q736
R736 68
C737 150
R733 30
P836
P520
P906
+50V
14
L728 3.35µH
C728 1µF
R629 2.7
L902 3.35µH
C813 10µF
C818 0.1
+50V1
+50V2
P/O MAIN INTERCON
+15V
GND
L726 3.35µH
C730 4.7µF
R732 2.7
C726 0.1
L902 3.35µH
C804 100µF
C805 0.1
+15V1
+15V2
TP420
P/O MAIN INTERCON
P/O DEFLECTION AMP BD. A26
+5V
-15V
-50V
L810 3.35µH
C722 4.7µF
R722 2.7
C629 0.1
+5V1
L806 3.35µH
C822 100µF
C821 0.1
-15V1
L900 3.35µH
C820 10µF
C920 0.1
-50V1
P/O MAIN INTERCON
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE:
* INDUCTANCE DUE TO LEAD LENGTH
≠ PART OF EC BOARD
≠ THICK FILM RESISTOR
§ MATCHED PAIR
Static Sensitive Devices
See Maintenance Section
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
2387-819
7612D
VERTICAL AMPLIFIER 11 Sc
VERTICAL AMPLIFIER
11

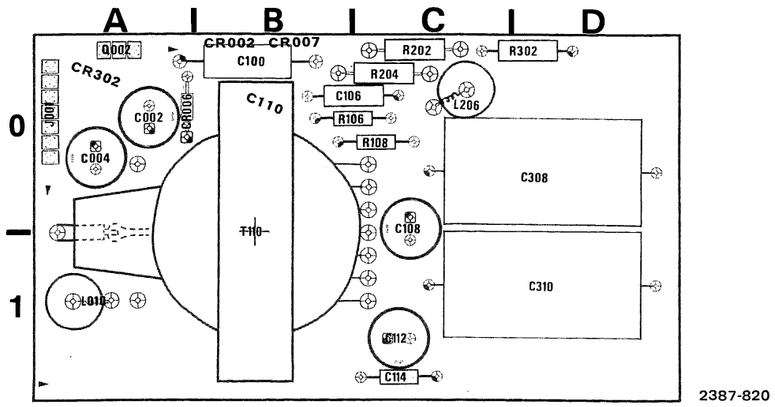


Fig. 8-13. High Voltage Oscillator circuit board, assembly A76.

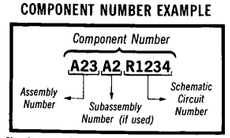
A76 ASSY			HIGH VOLTAGE/CRT ◇12◇		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C002	G6	A0	CR302*	G6	A0
C004	G6	A0	L010	G6	A1
C100	G6	B0	L206	G6	C0
C106	G6	C0	P001	F6	A0
C108	G6	C0	P001	H6	A0
C110*	G6	B0	Q002	G6	A0
C112	F6	C1	R106	G6	C0
C114	G6	C1	R108	G6	C0
C308	G6	D0	R202	F6	C0
C310	G6	D1	R204	F6	C0
CR002*	G6	B0	R302	G6	D0
CR006	G6	A0	R302**	G6	B0
CR007*	G6	B0	T110	G6	B0
			VR110*	G6	
P/O A68 ASSY			HIGH VOLTAGE/CRT ◇12◇		
P558	G5	A6	——	——	——
A68 ASSY SHOWN IN FIG. 8-31					

*See Parts List for serial number ranges.

**. Located on front of board SN B010000—SN B029999

†Located back of board.

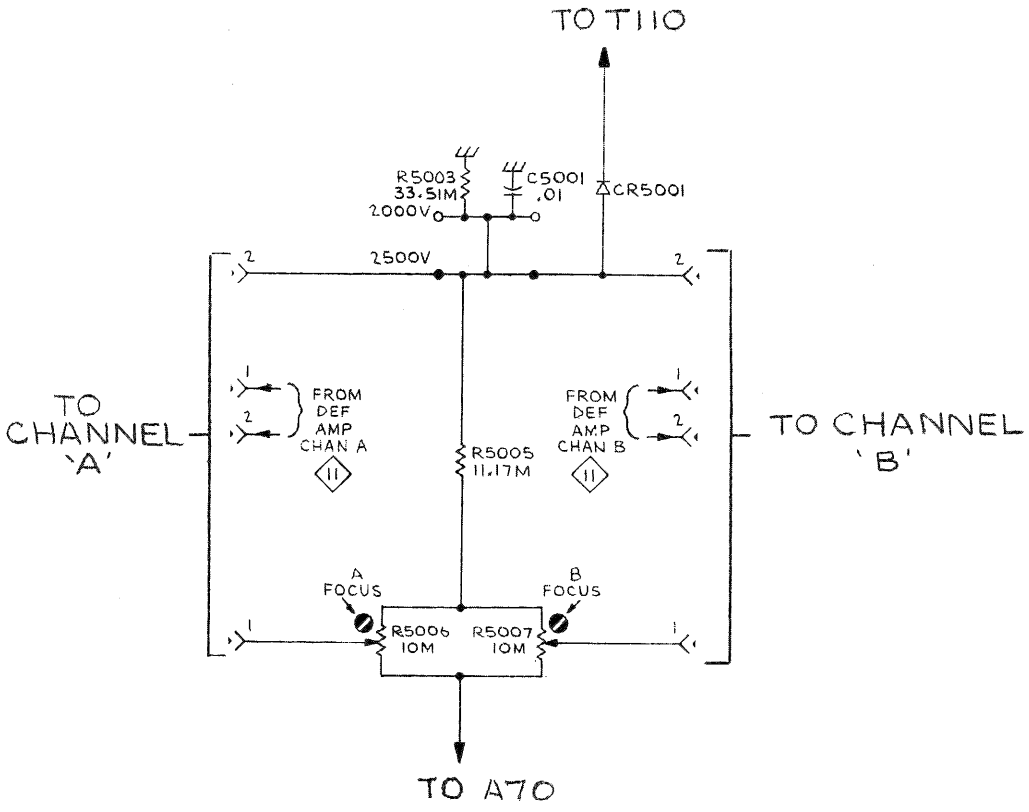
COMPONENT NUMBER EXAMPLE



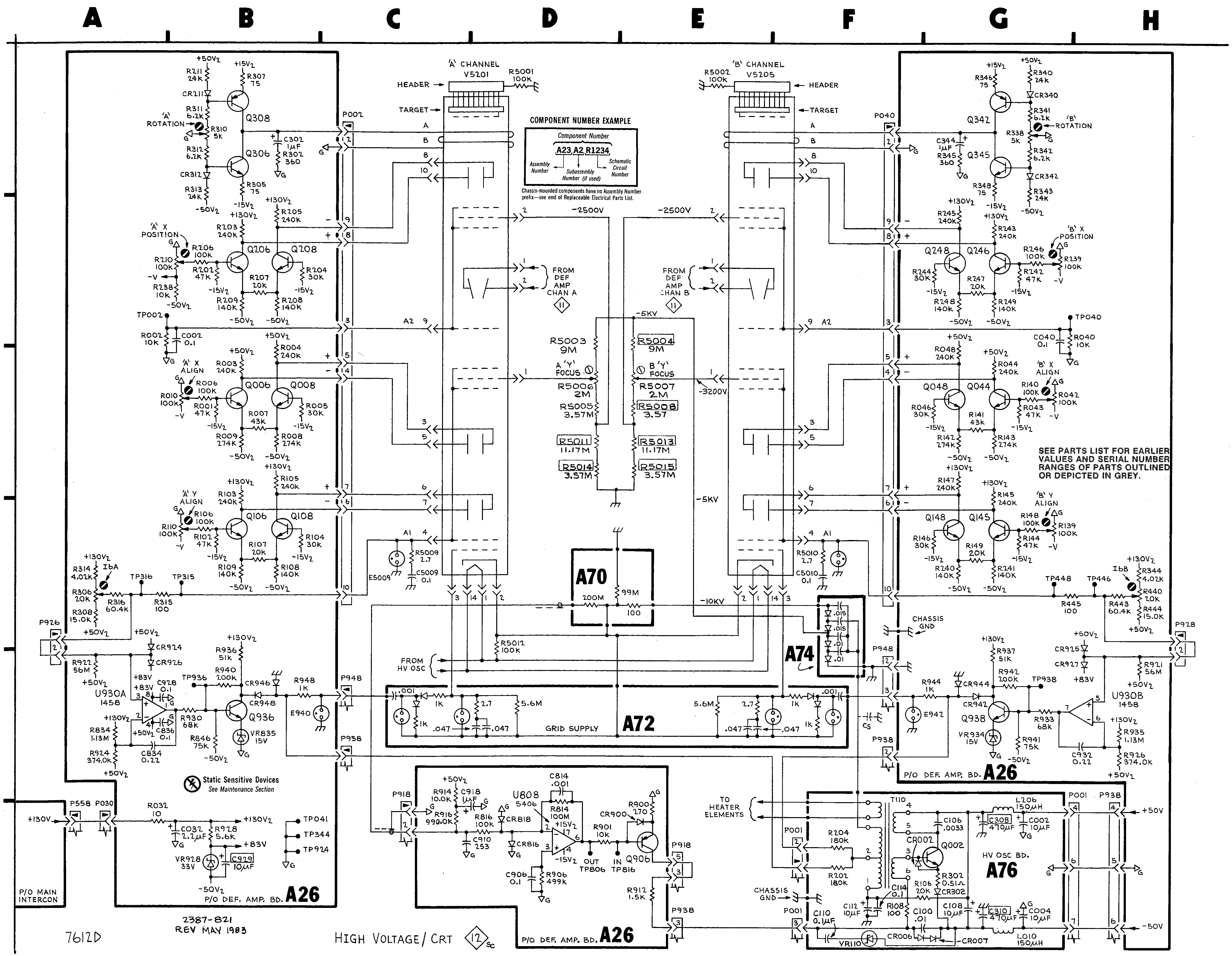
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

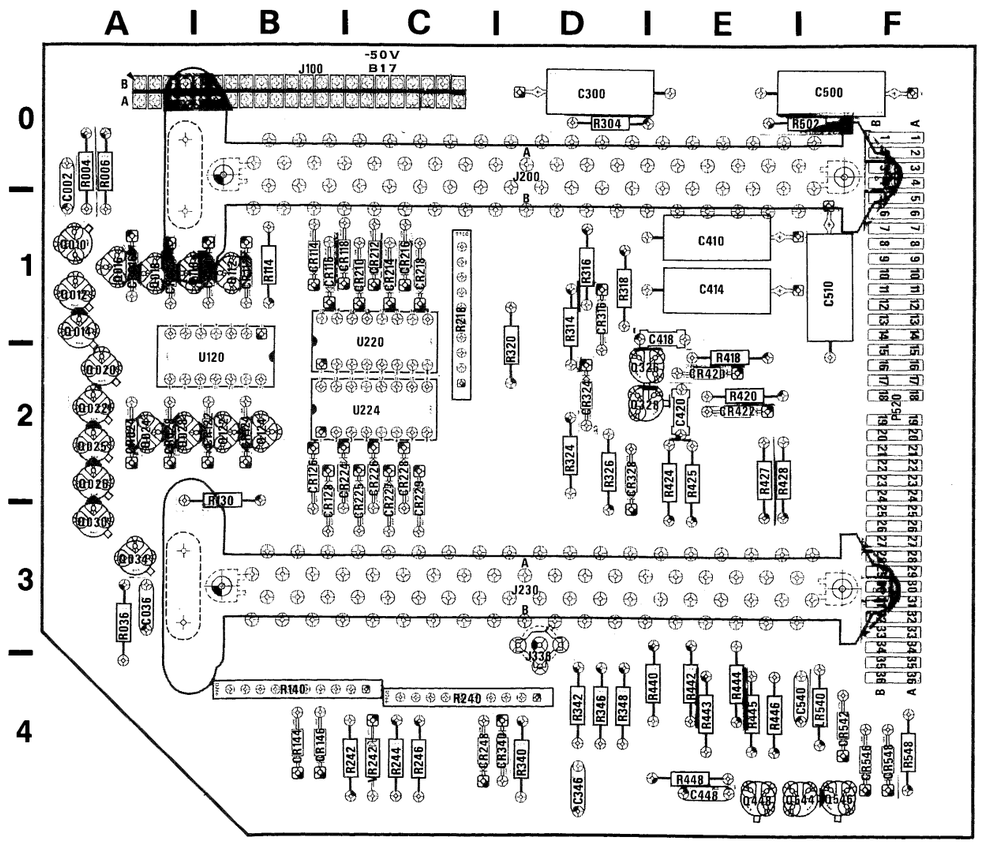
Static Sensitive Devices
See Maintenance Section

P/O A26 ASSY			HIGH VOLTAGE/CRT ◇12◇					
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C002	B2	A0	R006	B3	A0	R343	G1	D4
C032	B6	A3	R007	B3	A0	R344	H4	D4
C040	G2	A4	R008	B3	A0	R345	G1	D4
C302	B1	C0	R009	B3	A0	R346	G1	D4
C344	G1	D4	R010	B3	A1	R348	G1	D4
C814	E6	J1	R032	A6	A3	R440	H4	D4
C814	E6	J1	R040	G2	A4	R443	H4	E4
C834	B5	J3	R042	G3	A3	R444	H4	E4
C836	A5	K3	R043	G3	A4	R445	G4	E4
C906	E6	K1	R044	G3	A4	R814	P5	J1
C910	D6	K1	R046	G3	A4	R816	D6	J1
C918	D6	K1	R048	G3	A4	R834	A5	J3
C928	A5	K2	R102	B4	B0	R846	B5	J4
C929	B6	K2	R103	B3	B0	R900	F6	K0
C932	G5	K3	R104	B4	B0	R901	E6	K0
C5001*	CHASSIS	CHASSIS	R105	B3	B0	R906	E6	K1
C5009	C4	CHASSIS	R106	B4	B0	R912	F6	K1
C5010	F4	CHASSIS	R107	B4	B0	R914	D6	K1
CR211	B1	C1	R108	B4	B0	R916	D6	K1
CR312	B1	D1	R109	B4	B0	R921	H5	K2
CR340	G1	D4	R110	B4	B1	R922	A5	K2
CR342	G1	D4	R139	G4	B3	R924	A5	J2
CR816	E6	J1	R140	G3	B4	R926	H5	K2
CR818	E6	J1	R141	G3	B4	R928	B6	K2
CR900	F6	K0	R142	G3	B4	R930	B5	J3
CR924	A5	K2	R143	G3	B4	R933	G5	K3
CR925	H5	K2	R144	G4	B4	R935	H5	K3
CR926	A5	K2	R145	G4	B4	R936	B5	K3
CR927	H5	K2	R146	G4	B4	R937	G5	K3
CR942	G5	K4	R147	G3	B4	R940	B5	K4
CR944	G5	K4	R148	G4	B4	R941	G5	K4
CR946	B5	K4	R149	G4	B4	R942	G5	K3
CR948	B5	K4	R202	B2	C0	R944	G5	K3
CR5001*	CHASSIS	CHASSIS	R203	B2	C0	R948	B5	K4
E940	B5	J4	R204	B2	C0	R5001	D1	CHASSIS
E942	F5	K4	R205	B2	C0	R5002	E1	CHASSIS
E5009	C4	CHASSIS	R206	B2	C0	R5003	D1	CHASSIS
E5010	F4	CHASSIS	R207	B2	C0	R5004*	E2	CHASSIS
P002	C1	D0	R208	B2	C0	R5005	E2	CHASSIS
P002	C1	A0	R209	B2	C0	R5006	D3	CHASSIS
P030	A6	A3	R210	B2	C1	R5007	D3	CHASSIS
P040	F1	A4	R211	B1	C1	R5008*	CHASSIS	CHASSIS
P918	D6	K1	R238	B2	C3	R5009	C4	CHASSIS
P918	F6	K1	R239	G2	C3	R5010	F4	CHASSIS
P926	A4	K2	R240	G4	C4	R5011*	CHASSIS	CHASSIS
P928	H4	K2	R241	G4	C4	R5013*	D5	CHASSIS
P938	C5	K3	R242	G2	C4	R5013*	CHASSIS	CHASSIS
P938	F5	K3	R243	G2	C4	R5014*	CHASSIS	CHASSIS
P938	H6	K3	R244	G2	C4	R5015*	CHASSIS	CHASSIS
P948	C5	K4	R245	G2	C4	R5009	C4	CHASSIS
P948	F5	K4	R246	G2	C4	R5010	F4	CHASSIS
Q006	B3	A0	R247	G2	C4	R5012	D5	CHASSIS
Q008	B3	A0	R248	G2	C4	R5202	E1	CHASSIS
Q044	G3	A4	R249	G2	C4	TP002	A2	A0
Q048	G3	A4	R302	B1	D0	TP040	G2	A4
Q106	B4	B0	R305	B1	D0	TP041	B6	A4
Q108	B4	B0	R306	A4	D0	TP315	B4	D1
Q145	G4	B4	R307	B1	D0	TP316	A4	D1
Q148	G4	B4	R308	A4	D0	TP344	B6	D3
Q206	B2	C0	R310	B1	D1	TP446	H4	E4
Q208	B2	C0	R311	B1	D1	TP448	G4	E4
Q246	G2	C4	R312	B1	D1	TP806	E6	J0
Q248	G2	C4	R313	B1	D1	TP816	E6	K1
Q306	B1	D0	R314	A4	D1	TP924	B6	K1
Q308	B1	D0	R315	A4	D1	TP936	B5	J3
Q342	G1	D4	R316	A4	D1	TP938	G5	K3
Q345	G1	D4	R338	G1	D3	U808	E6	J0
Q906	F6	K0	R340	G1	D4	U930A	A5	K3
Q936	B5	K3	R341	G1	D4	U930B	H5	K3
Q938	G5	K3	R342	G1	D4	V5201	C1	CHASSIS
R001	B3	A0				VR835	B5	J3
R002	A2	A0				VR928	B6	K2
R003	B3	A0				VR934	G5	K3
R004	B3	A0						
R005	B3	A0						
P/O A26 ASSY ALSO SHOWN ON ◇4◇ , ◇11◇								



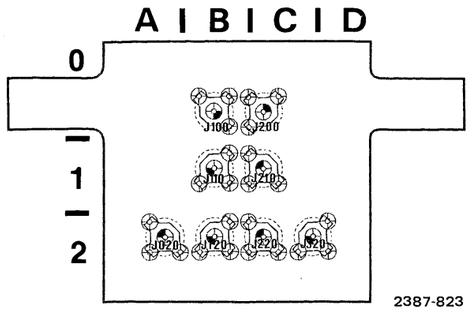
SN B029999 & BELOW


A
B
C
D
E
F
G
H
1
2
3
4
5
6
'A' CHANNEL V5201
'B' CHANNEL V5205
HEADER
TARGET
R5001 100k
R5002 100k
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
'A' ROTATION
'B' ROTATION
'A' X POSITION
'B' X POSITION
'A' X ALIGN
'B' X ALIGN
'A' Y ALIGN
'B' Y ALIGN
Q308
Q306
Q342
Q345
Q206
Q208
Q248
Q246
Q006
Q008
Q048
Q044
Q106
Q108
Q148
Q145
P002
P040
-2500V
-5KV
-3200V
-10KV
FROM DEF AMP CHAN A
FROM DEF AMP CHAN B
R5003 9M
R5004 9M
A 'Y' FOCUS
B 'Y' FOCUS
R5006 2M
R5007 2M
R5005 3.57M
R5008 3.57
R5011 11.17M
R5013 11.17M
R5014 3.57M
R5015 3.57M
A70
200M
99M
100
A74
A72
GRID SUPPLY
TP002
TP040
TP316
TP315
TP448
TP446
IbA
Ib8
E5009
R5009 2.7
C5009 0.1
R5010 2.7
C5010 0.1
R5012 100K
FROM HV OSC
CHASSIS GND
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
P926
P928
P948
P938
U930A 1458
U930B 1458
Q936
Q938
E940
E942
TP936
TP938
Static Sensitive Devices
See Maintenance Section
P/O DEF. AMP. BD. A26
P558
P030
+130V
R032 10
C032 2.2μF
R928 5.6K
VR928 33V
C929 10μF
TP041
TP344
TP924
P/O MAIN INTERCON
P918
U808 5406
Q906
OUT TP806
IN TP816
TO HEATER ELEMENTS
T110
Q002
HV OSC BD. A76
P001
+50V
-50V
L206 150μH
L010 150μH
C308 470μF
C310 470μF
VR110
7612D
2387-821
REV MAY 1983
HIGH VOLTAGE / CRT 12 SC



2387-822

Fig. 8-14a. Plug-in Interface circuit board, assembly A46.



2387-823

Fig. 8-14b. Vertical Interconnect circuit board, assembly A44.

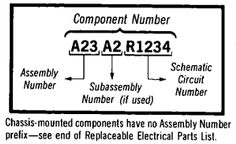
A44 ASSY			PLUG-IN INTERFACE ◇13		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
J020	D3	A2	J200	G4	C0
J100	D3	B0	J210	G4	C1
J110	D3	B1	J220	G4	C2
J120	D3	B2	J320	G4	D2

P/O A46 ASSY			PLUG-IN INTERFACE ◇13		
J200	C2	C2	R346	F3	D4
J230	D3	F2	R440	F3	E4
J336	E2	D3	R442	C4	E4
R304	C2	D0	R443	C4	E4
R316	C3	D1	R444	E4	E4
R324	F2	D2	R445	E4	E4
R342	F2	D4	R502	C4	F0
P/O A46 ASSY ALSO SHOWN ON ◇14					

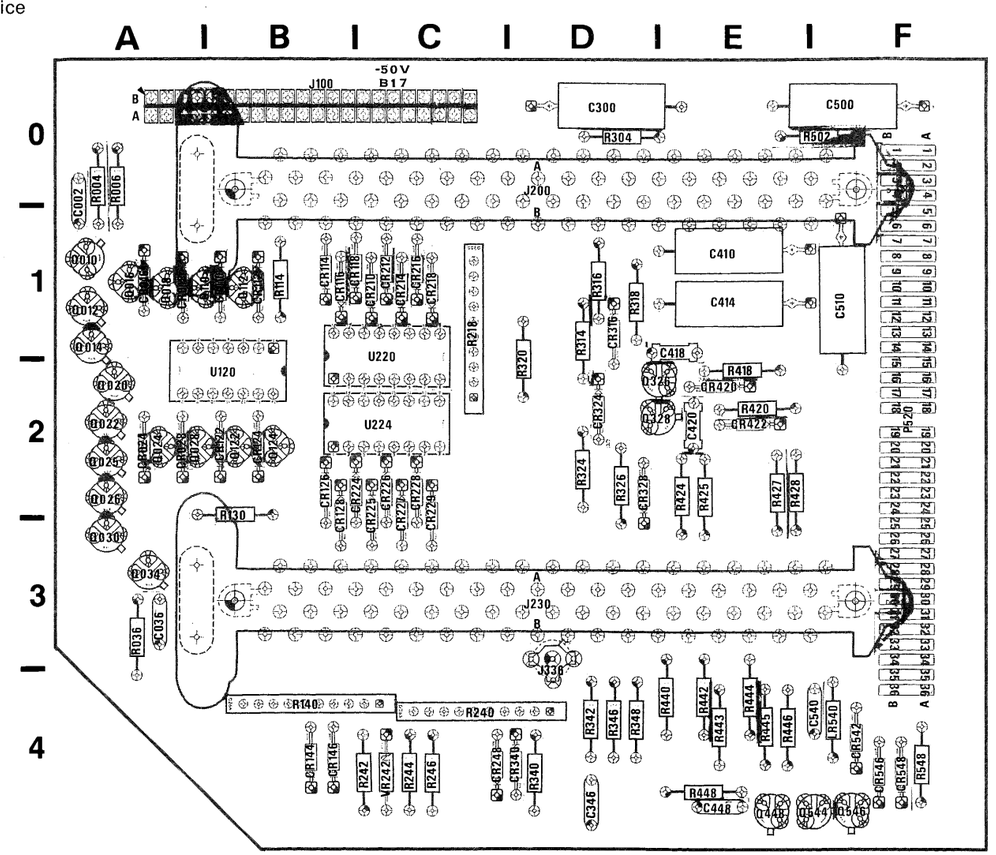
P/O A68 ASSY			PLUG-IN INTERFACE ◇13		
P118	B4	B1	P118	E4	B1
A68 ASSY SHOWN IN FIG. 8-31					

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



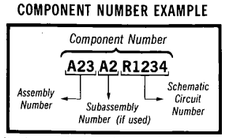
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



2387-822

Fig. 8-15. Plug-in Interface circuit board, assembly A46.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

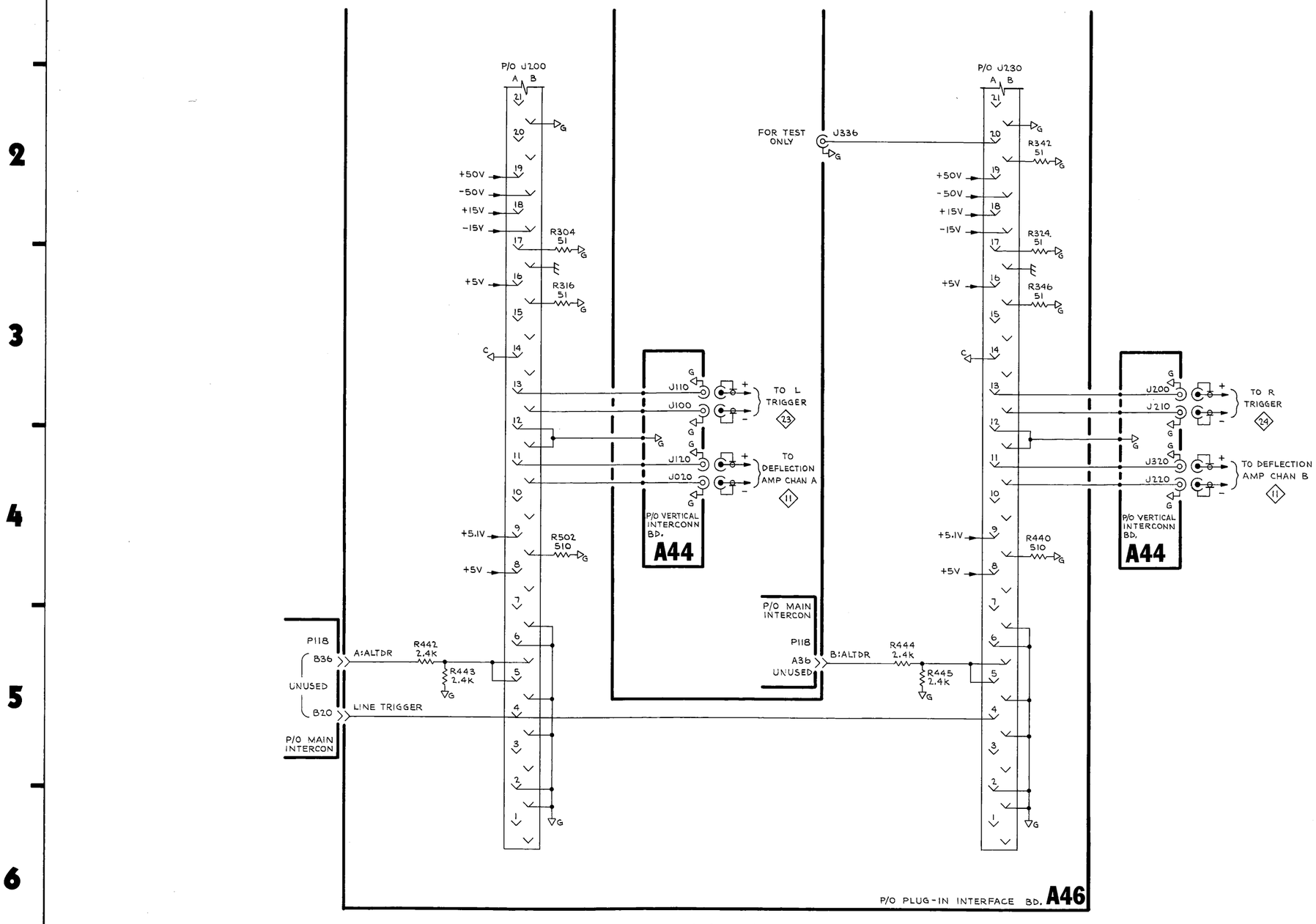
Static Sensitive Devices
See Maintenance Section

P/O A46 ASSY			READOUT/7K ACQUISITION ◇14		
Circuit Number	**Schematic Location**	**Board Location**	**Circuit Number**	**Schematic Location**	**Board Location**
C002	B1	A0	Q110	B2	A1
C036	A2	A3	Q112	B2	B1
C300	D5	D0	Q122	F2	B2
C346	F4	D4	Q124	G2	B2
C410	D5	E1	Q326	D4	D2
C414	D5	E1	Q328	E4	D2
C418	D4	E2	Q448	B4	E4
C420	E4	E2	Q544	B4	E4
C448	B4	E4	Q546	A4	F4
C500	D5	F0	R004	B1	A0
C510	D5	F1	R006	B1	A0
C540	B3	E4	R036	A2	A3
CR016	C2	A1	R114	A1	B1
CR018	B2	A1	R130	G3	B3
CR024	F2	A2	R140A	G4	B4
CR028	F2	B2	R140B	G4	B4
CR110	B2	B1	R140C	G3	B3
CR112	B2	B1	R140D	G4	B4
CR114	D3	A1	R140E	G4	B4
CR116	D3	B1	R140F	G4	B4
CR118	D3	C1	R140G	G3	B3
CR122	F2	B2	R140H	G3	B3
CR124	G2	B2	R140J	G3	B4
CR126	F3	C2	R218	C4	C1
CR128	F3	B3	R218A	C3	C1
CR144	B3	B4	R218B	C3	C1
CR146	H3	B4	R218C	C3	C1
CR210	D3	C1	R218D	C3	C1
CR212	D3	C1	R218E	C4	D2
CR214	D3	C1	R218F	C3	C1
CR216	D3	C1	R218G	C4	C1
CR218	D3	C1	R218H	C3	C1
CR224	F3	C2	R218J	C3	C1
CR225	F3	C2	R240A	F4	C4
CR226	E3	C2	R240B	F4	C4
CR227	E3	C2	R240C	F4	C4
CR228	E3	C2	R240D	F4	C4
CR229	F3	C2	R240E	F4	C4
CR248	F4	C4	R240F	F4	C4
CR316	D4	D1	R240G	F4	C4
CR324	E4	D2	R240H	F4	C4
CR328	D3	D2	R240J	F4	C4
CR340	F4	D4	R242	D2	C4
CR420	E4	E2	R244	D2	C4
CR422	E4	E2	R246	D2	C4
CR542	A4	F4	R314	E4	D1
CR546	A4	F4	R318	D4	D1
CR548	B4	F4	R320	C4	D2
J200	C2	D0	R326	D3	D2
J230	G2	D3	R340	D2	D4
LR540	A3	F4	R348	B4	D4
P100	A6	B0	R418	D4	E2
Q010	C1	A1	R420	E4	E2
Q012	C1	A1	R424	D2	E2
Q014	B1	A1	R425	D2	E2
Q016	C2	A1	R427	D2	E2
Q018	C2	A1	R428	D2	E2
Q020	B1	A2	R446	B4	E4
Q022	F1	A2	R448	B4	E4
Q024	F2	A2	R548	A5	F4
Q025	F1	A2	U120	A2	B2
Q026	G1	A2	U220	D3	C1
Q028	F2	A2	U224	E3	C2
Q030	G1	A3	VR242	F5	C4
Q034	B2	A3			

P/O A46 ASSY ALSO SHOWN ON ◇13

P/O A68 ASSY			READOUT/7K INTERFACE ◇14		
P118	A1	B1	P118	E6	B1
P118	D1	B1	P118	H1	B1

A68 ASSY SHOWN IN FIG. 8-31


P/O J200
A B
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
G
+50V
-50V
+15V
-15V
+5V
+5.1V
R304
51
R316
51
R502
510
J110
J100
J120
J020
TO L TRIGGER
23
TO DEFLECTION AMP CHAN A
11
P/O VERTICAL INTERCONN BD.
A44
FOR TEST ONLY
J336
P/O J230
R342
51
R324
51
R346
51
R440
510
J200
J210
J320
J220
TO R TRIGGER
24
TO DEFLECTION AMP CHAN B
P/O MAIN INTERCON
P118
A36
UNUSED
B:ALTDR
R444
2.4K
R445
2.4K
P118
B36
A:ALTDR
R442
2.4K
R443
2.4K
UNUSED
B20
LINE TRIGGER
P/O MAIN INTERCON
P/O PLUG-IN INTERFACE BD. A46

2387-824

P/O PLUG-IN INTERFACE

P/O MAIN INTERCON

P118

7KDIO1 7KDIO2 7KDIO3 7KDIO4 7KDIO5 7KDIO6 7KDIO7 7KDIO8 RORST ROT

ANALOG DATA B33

Q020 Q014 Q012 Q010 Q022 Q026 Q030

CR016 CR018 CR110 CR112 CR122 CR124 CR024 CR028

U120 74LS164

R114 1K +5.1V

BDO A20

SHIFT A22

TIMESLOT A21

R006 220 +5V

C002 .01

R004 300

R036 3.9K +5V

C036 .01 -15V

Q034

R246 R244 R242 R340 R414 R427 R415 R418 ALL 39K -15V

Q112 Q110 Q018 Q016 Q028 Q024 Q122 Q124

P/O U200 A B

P/O U230 A B

CR114 CR116 CR118 CR210 CR218 CR216 CR214 CR212

CR126 CR128 CR224 CR225 CR229 CR228 CR227 CR226

U220 ETS

U224 ETS

R328 470 +5V

CR326 CR328

R326 2.2K -15V

C418 220

R318 10K

R314 10K

C420 220

R420 10K

R418 10K

Q326 Q318

CR316 CR374

CR420 CR422

R218 ALL 150K

R320 150K

TS 1 TS 4 TS 3 TS 6 TS 5 TS 8 TS 7 TS 10 TS 9

B32 7KLVADR

CR144

L540 0.5μH

C540 .01 +15V

R100 100

R548 18K

Q546 Q544 Q448

C448 .0022

R448 4.7K +5V

R564 20K -15V

CR548

R348 10K -15V

CR542 CR546

ETS

CR146 7KRVADR B31

R130 150K

R140 ALL 150K

R240 ALL 510Ω

CR148 CR340

C346 0.1

VR242 8.2V -5.2V

+5.1V -5.2V

7KSND B27

7KNDAC A29

7KNRFD A30

7KIFC B26

7KATN B25

7KDAV A31

7KREN B24

7KEOI A25

7KSRQ A26

+50V +15V +5V -15V -50V GND GND SENS +50V SENS +15V SENS +5V SENS -15V SENS -50V SENS +130V

C500 10μF

C300 10μF

C510 10μF

C410 10μF

C414 10μF

P100

TO/FROM REGULATOR BD. P420 (29)

P118 +130V

CHASSIS GND

P/O MAIN INTERCON

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

2387-825

7612D

READOUT/ 7K ACQUISITION (14) 5c

READOUT/7K ACQUISITION (14)

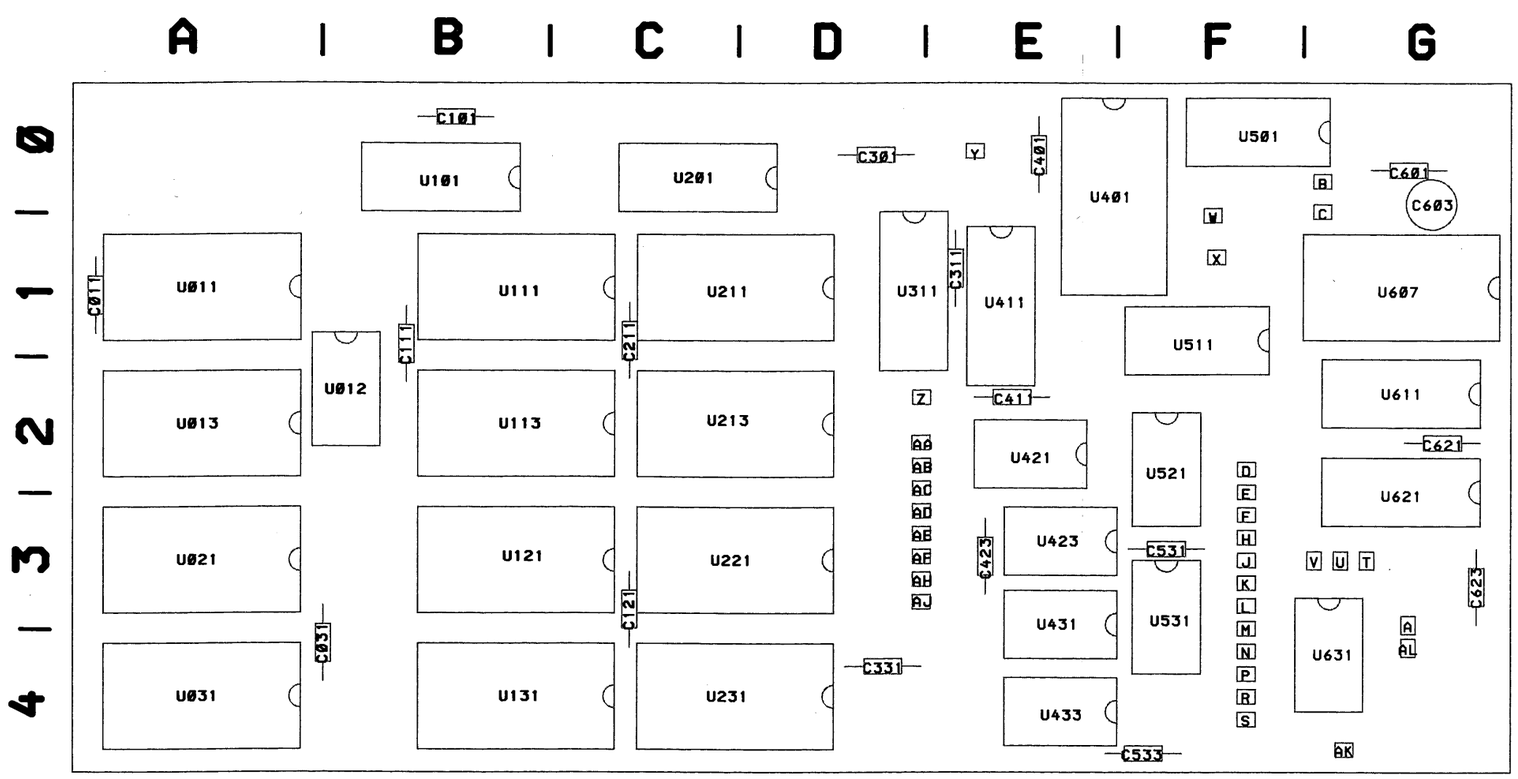


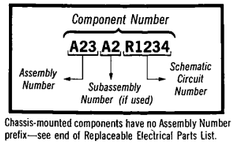
Fig. 8-16. MPU Memory circuit board, assembly A52.

P/O A52 ASSY — MPU MEMORY SELEC

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location
C011	F3	B0	U421B	C5
C031	F3	B4	U421C	C5
C101	F3	B0	U421D	C5
C111	F3	B1	U423A	D5
C121	F3	C3	U423B	D5
C211	E3	C1	U423C	D2
C301	F3	D0	U423D	D2
C311	F3	E1	U431A	D4
C331	F3	D4	U431B	D4
C401	F3	E0	U431C	D4
C411	F3	E2	U431D	D5
C423	E4	E3	U433	D2
C531	F4	F3	U433B	D1
C533	F3	F4	U433C	D1
C601	F3	G0	U433D	D1
C603	E3	G1	U521A	C1
C621	F3	G2	U521F	D6
C623	F3	G3	U531A	C5
U012A	D3	B2	U531B	C5
U012B	D3	B2	U611	F2
U012C	D3	B2	U621	F1
U012D	D3	B2	U631	C6
U421A	C1	E2		

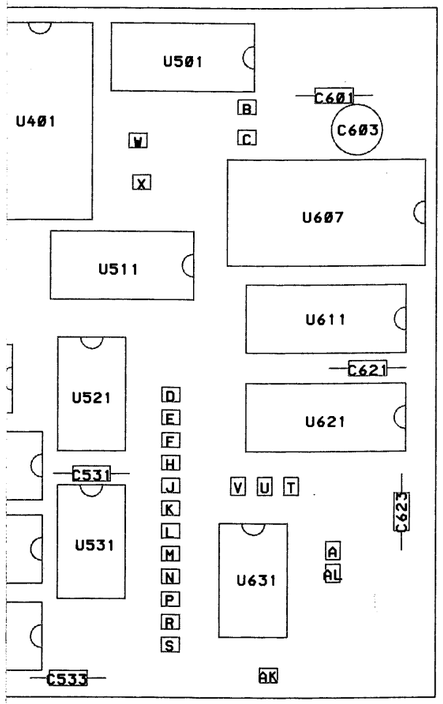
P/O A52 ASSY ALSO SHOWN ON 16

COMPONENT NUMBER EXAMPLE



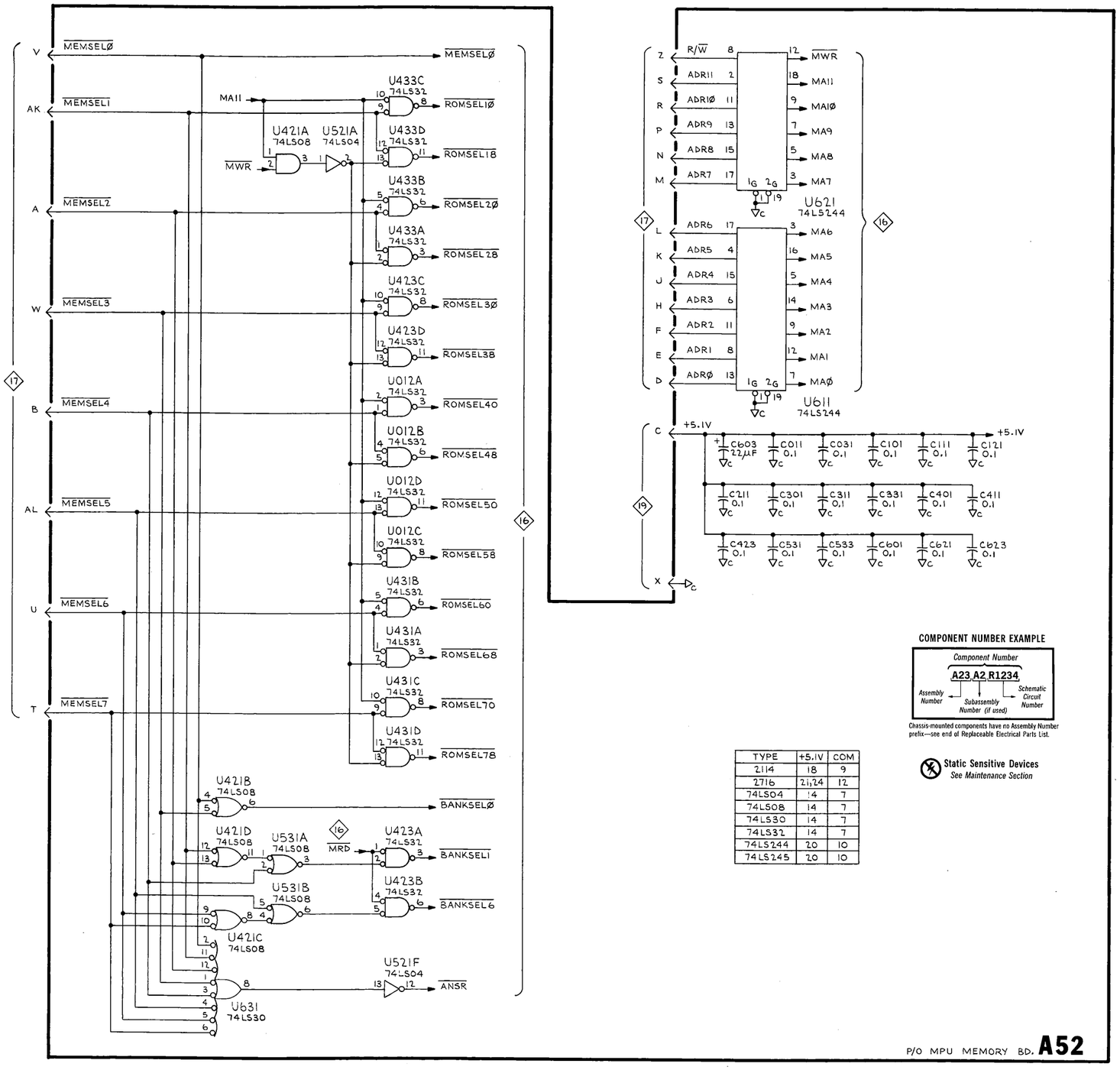
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



P/O A52 ASSY			MPU MEMORY SELECT 15		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C011	F3	B0	U421B	C5	E2
C031	F3	B4	U421C	C5	E2
C101	F3	B0	U421D	C5	E2
C111	F3	B1	U423A	D5	E3
C121	F3	C3	U423B	D5	E3
C211	E3	C1	U423C	D2	E3
C301	F3	D0	U423D	D2	E3
C311	F3	E1	U431A	D4	E3
C331	F3	D4	U431B	D4	E3
C401	F3	E0	U431C	D4	E3
C411	F3	E2	U431D	D5	E3
C423	E4	E3	U433	D2	E4
C531	F4	F3	U433B	D1	E4
C533	F3	F4	U433C	D1	E4
C601	F3	G0	U433D	D1	E4
C603	E3	G1	U521A	C1	F2
C621	F3	G2	U521F	D6	F2
C623	F3	G3	U531A	C5	F3
U012A	D3	B2	U531B	C5	F3
U012B	D3	B2	U611	F2	G2
U012C	D3	B2	U621	F1	G3
U012D	D3	B2	U631	C6	G4
U421A	C1	E2			

P/O A52 ASSY ALSO SHOWN ON 16



COMPONENT NUMBER EXAMPLE

Component Number: A23,A2,R1234
(Assembly Number · Subassembly Number (if used) · Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TYPE	+5.1V	COM
2114	18	9
2716	21,24	12
74LS04	14	7
74LS08	14	7
74LS30	14	7
74LS32	14	7
74LS244	20	10
74LS245	20	10

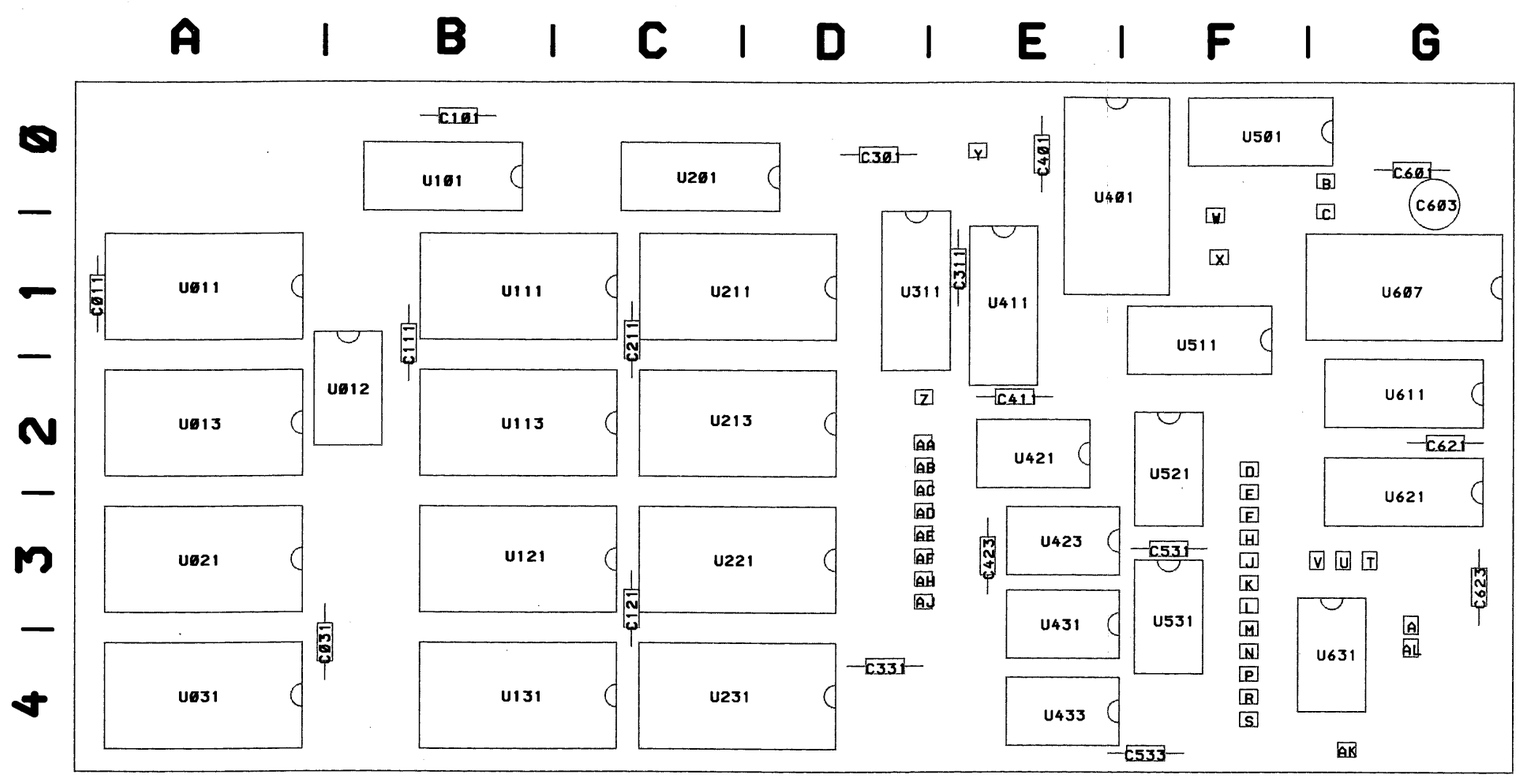
Static Sensitive Devices
See Maintenance Section

P/O MPU MEMORY BD. **A52**

2387-827

7612D

MPU MEMORY SELECT 15 sc

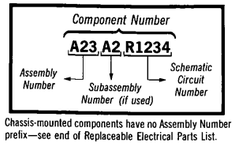


2387-826

Fig. 8-17. MPU Memory circuit board, assembly A52.

P/O A52 ASSY			MPU MEMORY 16		
Circuit Number	**Schematic Location**	**Board Location**	**Circuit Number**	**Schematic Number**	**Board Location**
U011	A5	A1	U213	C5	C2
U013	B5	A2	U221	E5	C3
U021	E3	A3	U231	F5	C4
U031	F3	A4	U311	H2	D1
U101	G4	B0	U401	C1	E0
U111	D3	B1	U411	G2	E1
U113	C3	B2	U501	F1	F0
U121	B3	B3	U511	E1	F1
U131	A3	B4	U521B	G2	F2
U201	G5	C0	U607	D1	G1
U211	D5	C1			
P/O A52 ASSY ALSO SHOWN ON 15					

COMPONENT NUMBER EXAMPLE



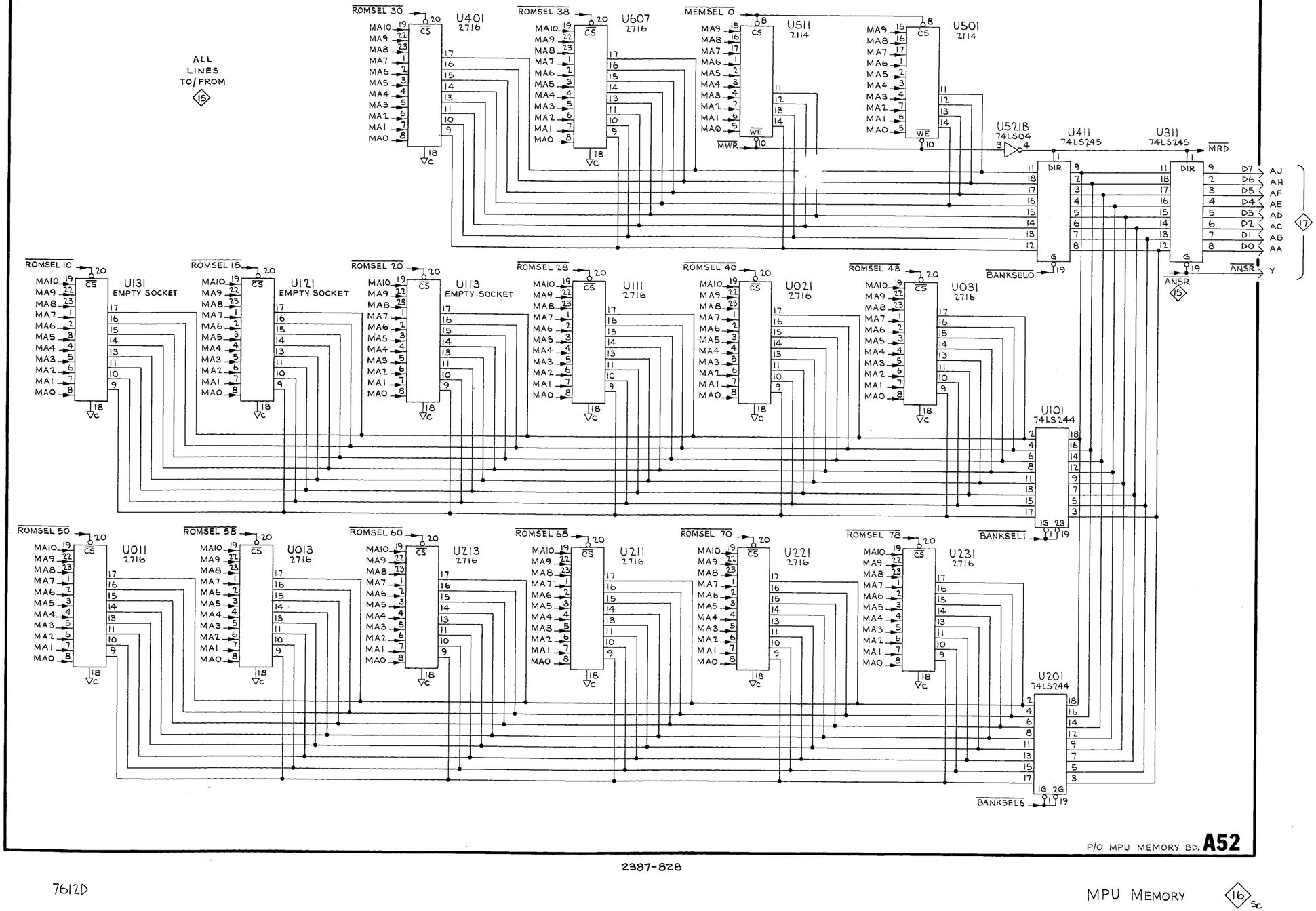
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A B C D E F G H

1 2 3 4 5 6

ALL LINES TO/FROM 15

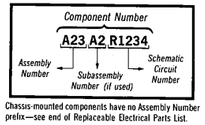


P/O MPU MEMORY BD. **A52**

2387-828

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

MPU A54

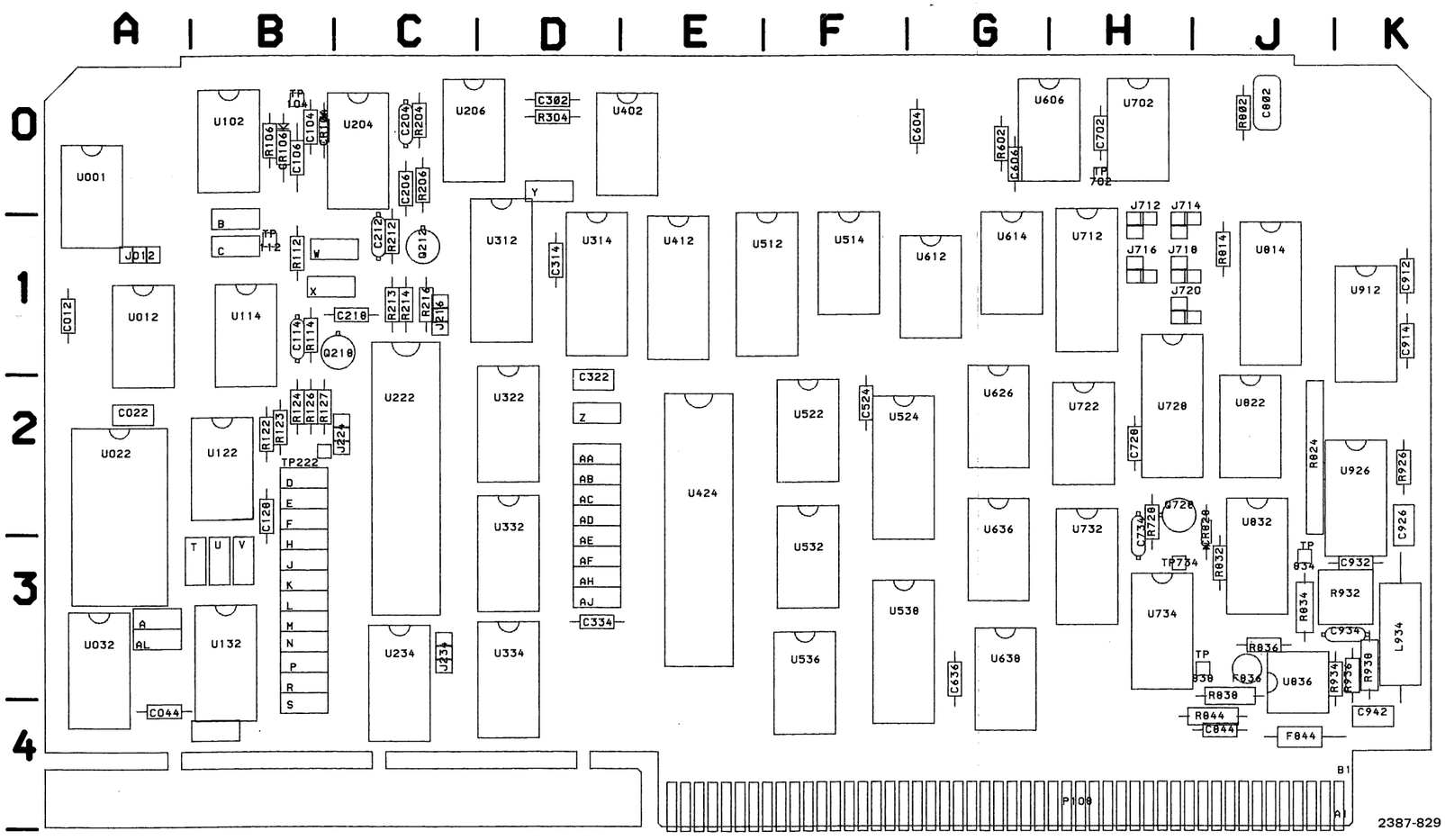


Fig. 8-18. MPU circuit board, assembly A54.

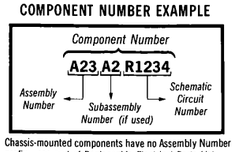
P/O A54 ASSY				
Circuit Number	Schematic Location	Board Location	Circuit Number	Sche Loc
C106	C4	B0	U012D	E
C114	B5	B1	U012E	E
C204	B3	C0	U012F	E
C212	B5	C1	U022	A
CR104	B4	B0	U032	A
CR106	C4	B0	U102A	E
J108	A1	H4	U102B	E
J108	H1	H4	U114A	C
P012	D6	A1	U114D	E
P216	D5	C1	U114E	E
P224	D5	B2	U114F	C
P234	G3	C3	U122A	F
Q212	C5	C1	U122B	D
Q218	C5	B1	U122D	H
R106	C4	B0	U132	E
R112	C3	B1	U204A	E
R122	D4	B2	U206A	E
R123	C3	B2	U206B	C
R124	C4	B2	U206C	E
R124	C5	B1	U206D	D
R126	C5	B2	U222	D
R127	C5	B2	U234A	E
R204	B3	C0	U312	E
R212	C5	C1	U314	E
R213	C5	C1	U322	C
R214	C5	C1	U332	C
R216	C5	C1	U334	C
R304	A3	D0	U402A	C
TP222	D4	B2	U402B	A
U001A	B5	A0	U402C	C
U001B	B6	A0	U702A	A
U012A	B5	A1	U734A	E
U012B	B5	A1	U734B	F

P/O A54 ASSY ALSO SHOWN ON ◇18

P/O A68 ASSY				
J108	A1	C1	J108	H

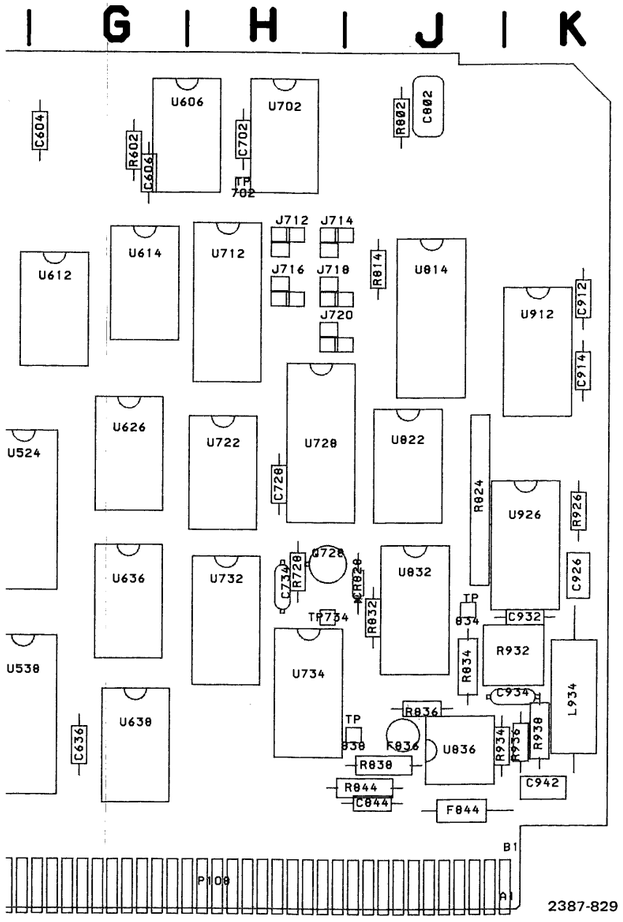
A68 ASSY SHOWN IN FIG. 8-31

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

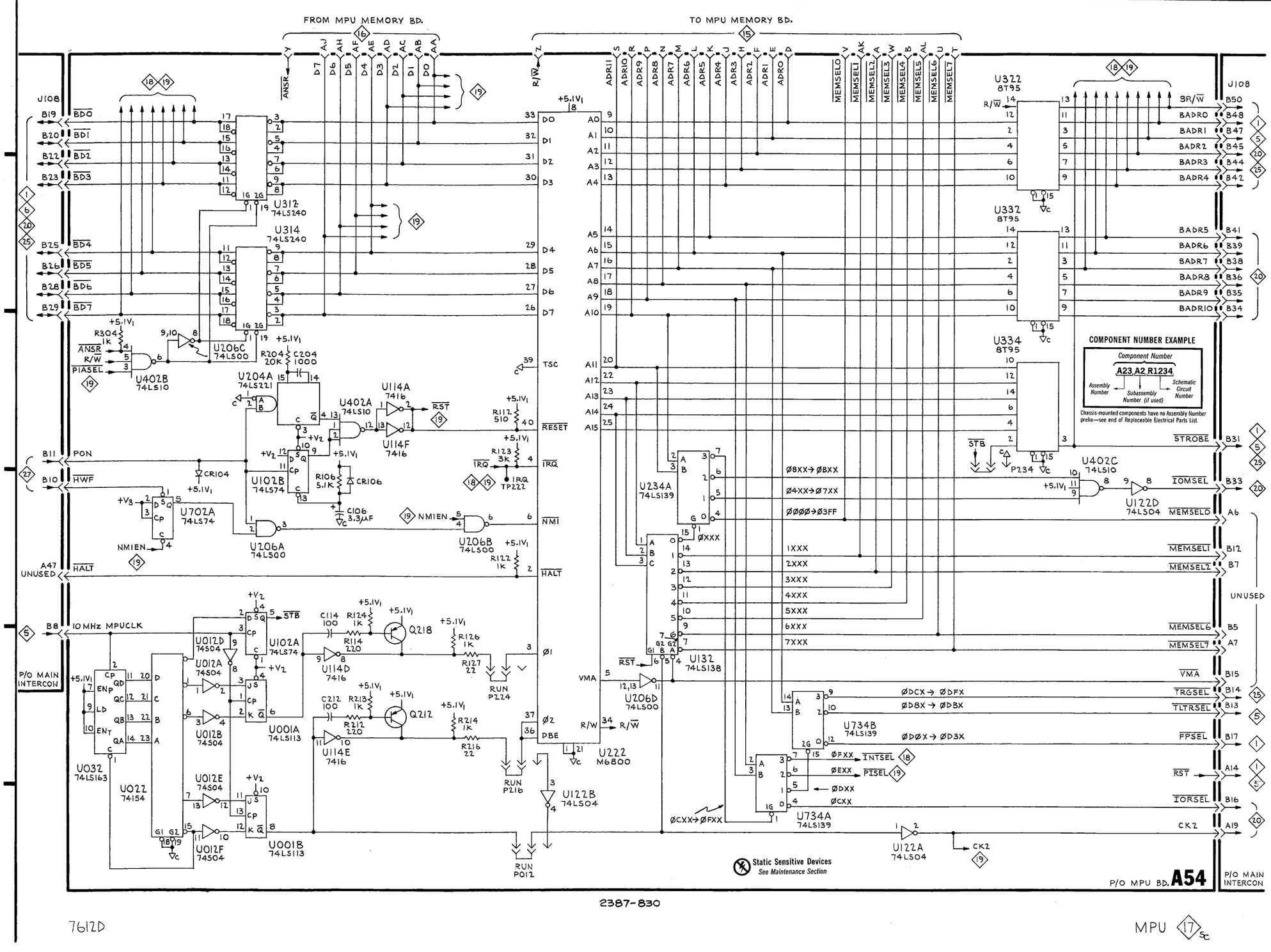


P/O A54 ASSY				MPU 17	
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C106	C4	B0	U012D	B5	A1
C114	B5	B1	U012E	B6	A1
C204	B3	C0	U012F	B6	A1
C212	B5	C1	U022	A6	A2
CR104	B4	B0	U032	A5	A3
CR106	C4	B0	U102A	B5	B0
J108	A1	H4	U102B	B4	B0
J108	H1	H4	U114A	C3	B1
P012	D6	A1	U114D	B5	B1
P216	D5	C1	U114E	B5	B1
P224	D5	B2	U114F	C3	B1
P234	G3	C3	U122A	F6	B2
Q212	C5	C1	U122B	D5	B2
Q218	C5	B1	U122D	H4	B2
R106	C4	B0	U132	E4	B3
R112	C3	B1	U204A	B3	C0
R122	D4	B2	U206A	B4	C0
R123	C3	B2	U206B	C4	C0
R124	C4	B2	U206C	B3	C0
R124	C5	B1	U206D	D5	C0
R126	C5	B2	U222	D5	C2
R127	C5	B2	U234A	E4	C3
R204	B3	C0	U312	B2	D1
R212	C5	C1	U314	B2	D1
R213	C5	C1	U322	G1	D2
R214	C5	C1	U332	G2	D2
R216	C5	C1	U334	G3	D3
R304	A3	D0	U402A	C3	E0
TP222	D4	B2	U402B	A3	E0
U001A	B5	A0	U402C	G4	E0
U001B	B6	A0	U702A	A4	H0
U012A	B5	A1	U734A	E5	H3
U012B	B5	A1	U734B	F5	H3

P/O A54 ASSY ALSO SHOWN ON 18 , 19

P/O A68 ASSY				MPU 17	
J108	A1	C1	J108	H1	C1

A68 ASSY SHOWN IN FIG. 8-31


FROM MPU MEMORY BD.
TO MPU MEMORY BD.
J108
P/O MAIN INTERCON
U312 74LS240
U314 74LS240
U206C 74LS00
U402B 74LS10
U204A 74LS221
U402A 74LS10
U114A 7416
U114F 7416
U102B 74LS74
U702A 74LS74
U206A 74LS00
U206B 74LS00
U102A 74LS74
U114D 7416
U114E 7416
U012D 74S04
U012A 74S04
U012B 74S04
U012E 74S04
U012F 74S04
U001A 74LS113
U001B 74LS113
U032 74LS163
U022 74154
U234A 74LS139
U734B 74LS139
U734A 74LS139
U132 74LS138
U206D 74LS00
U222 M6800
U122B 74LS04
U122D 74LS04
U122A 74LS04
U402C 74LS10
U372 8T95
U332 8T95
U334 8T95
Q218
Q217
P234
ØXXX
1XXX
2XXX
3XXX
4XXX
5XXX
6XXX
7XXX
ØBXX→ØBXX
Ø4XX→Ø7XX
ØØØØ→Ø3FF
ØDCX→ØDFX
ØD8X→ØDBX
ØDØX→ØD3X
ØFXX
ØEXX
ØDXX
ØCXX
ØCXX→ØFXX
INTSEL
PISEL
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2,R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
P/O MPU BD. A54
P/O MAIN INTERCON
2387-830
7612D
MPU 17 SC
MPU 17

MPU A54

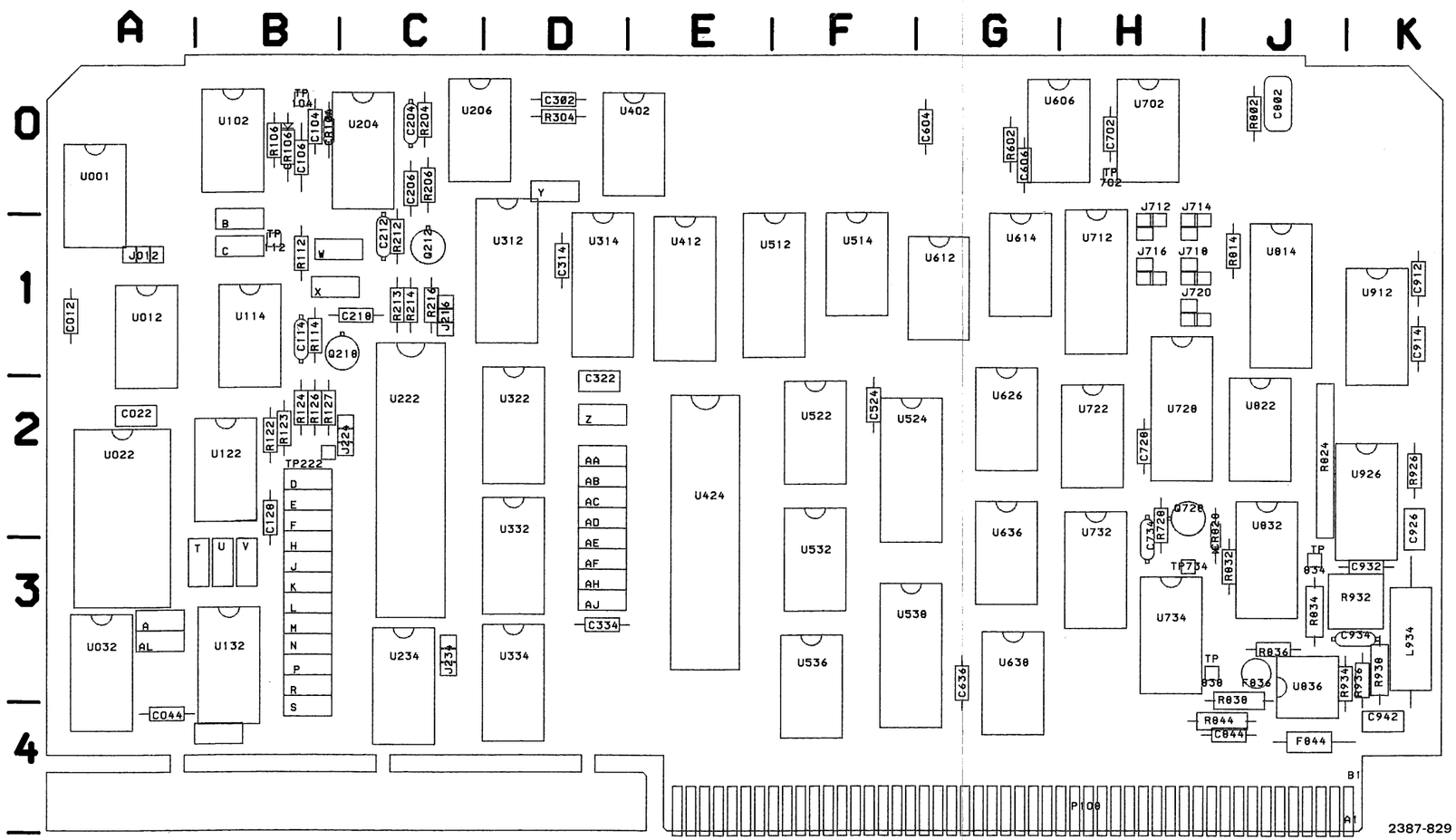


Fig. 8-19. MPU circuit board, assembly A54.

P/O A54 ASSY			6800 INTERR
Circuit Number	Schematic Location	Board Location	Circuit Number
C802	F3	J0	U612C
J108	E3	H4	U614A
P712	C2	H1	U614B
P714	C1	H1	U614C
P716	C3	H1	U614D
P718	C2	H1	U626B
P720	C2	H1	U636B
R802	E3	J0	U702B
U234B	F5	C3	U712
U514A	B4	F1	U722A
U514C	C4	F1	U722B
U514D	D3	F1	U722C
U524	G3	F2	U722D
U532D	F6	F3	U728
U606D	B3	H0	U732
U612A	G4	G1	
P/O A54 ASSY ALSO SHOWN ON 17			

P/O A68 ASSY			6800 INTERR
J108	A1	C1	—
A68 ASSY SHOWN IN FIG. 8-3			

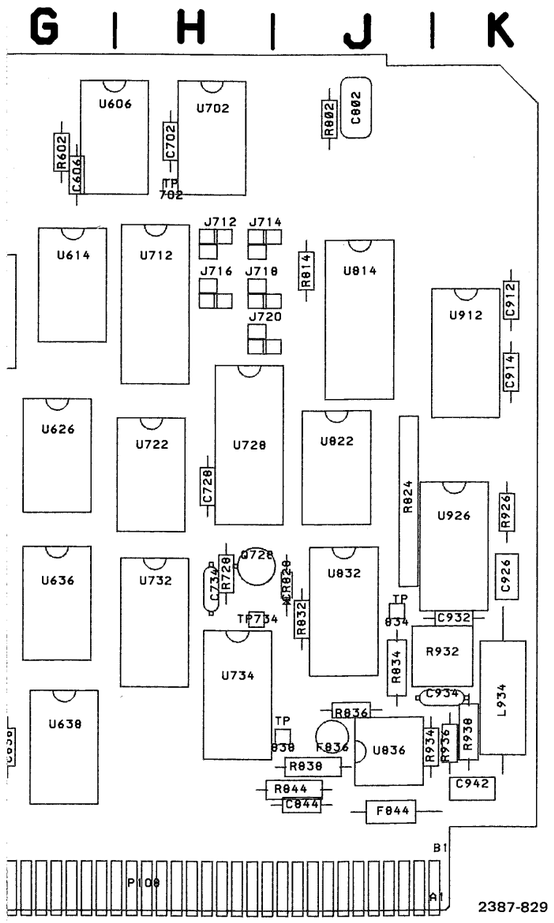
COMPONENT NUMBER EXAMPLE

Component Number: A23,A2,R1234

- A23 — Assembly Number
- A2 — Subassembly Number (if used)
- R1234 — Schematic Circuit Number

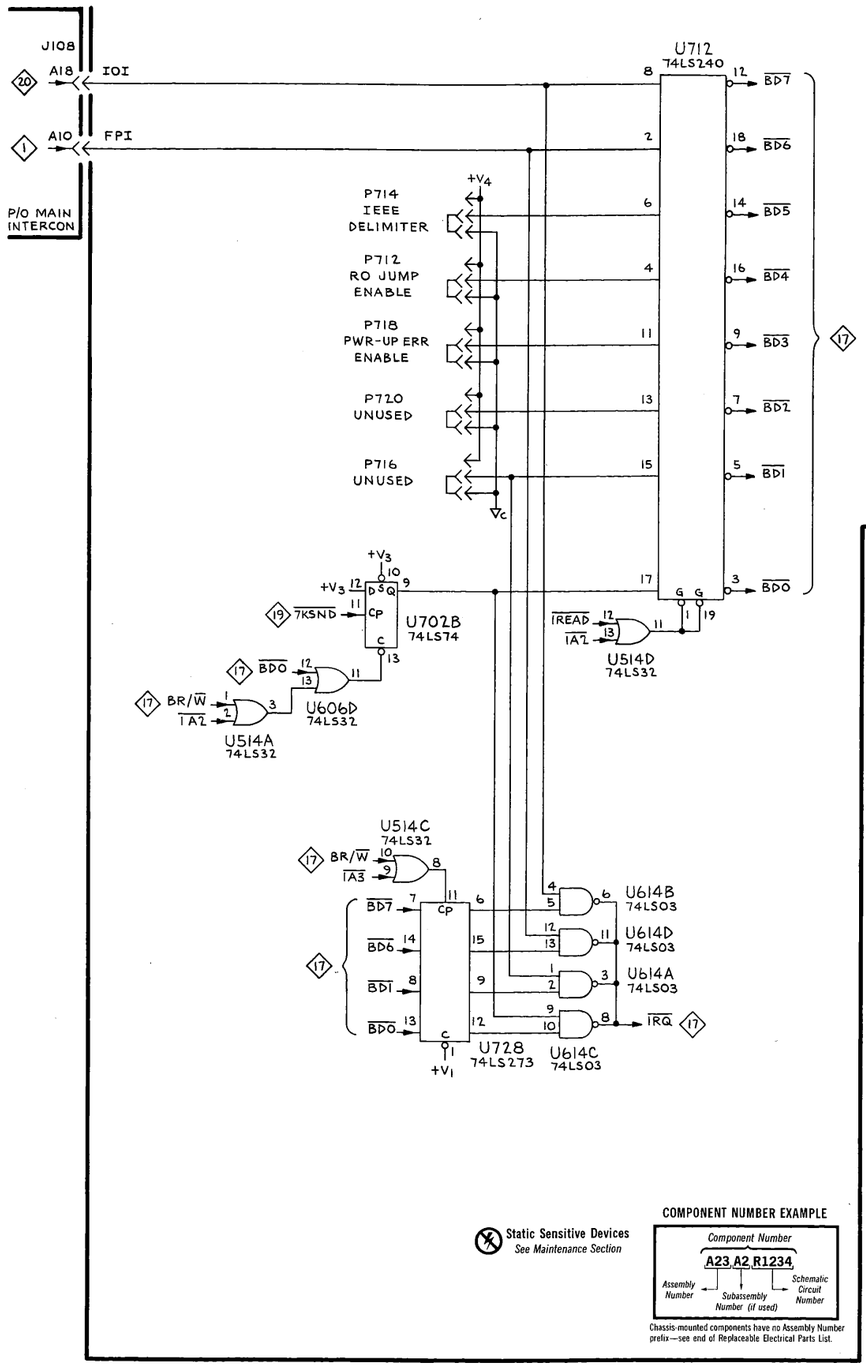
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



P/O A54 ASSY			6800 INTERRUPT CONTROL ◇18		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C802	F3	J0	U612C	F4	G1
J108	E3	H4	U614A	D5	G2
P712	C2	H1	U614B	C4	G1
P714	C1	H1	U614C	D5	G2
P716	C3	H1	U614D	D4	G1
P718	C2	H1	U626B	F6	G2
P720	C2	H1	U636B	F6	G3
R802	E3	J0	U702B	C3	H0
U234B	F5	C3	U712	D1	H1
U514A	B4	F1	U722A	F4	H2
U514C	C4	F1	U722B	F4	H2
U514D	D3	F1	U722C	F5	H2
U524	G3	F2	U722D	F5	H2
U532D	F6	F3	U728	C5	H2
U606D	B3	H0	U732	F5	H3
U612A	G4	G1			
P/O A54 ASSY ALSO SHOWN ON ◇17 , ◇19					

P/O A68 ASSY			6800 INTERRUPT CONTROL ◇18		
J108	A1	C1	—	—	—
A68 ASSY SHOWN IN FIG. 8-31					



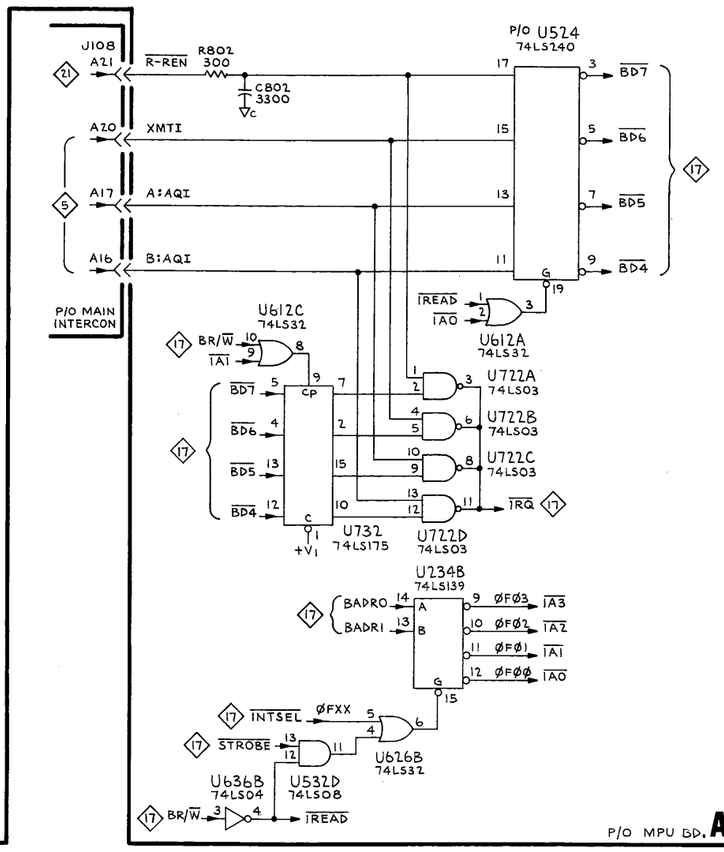
TYPE	+5.1V$_I$	COM
74LS00	14	7
74LS03	14	7
74LS04	14	7
74LS08	14	7
74LS10	14	7
7416	14	7
74LS32	14	7
74LS33	14	7
74LS74	14	7
74LS113	14	7
74LS138	16	8
74LS139	16	8
74147	16	8
74154	24	12
74LS163	16	8
74LS175	16	8
74LS221	16	8
74LS240	20	10
74LS273	20	10
8T95	16	8

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23,A2,R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



2387-831

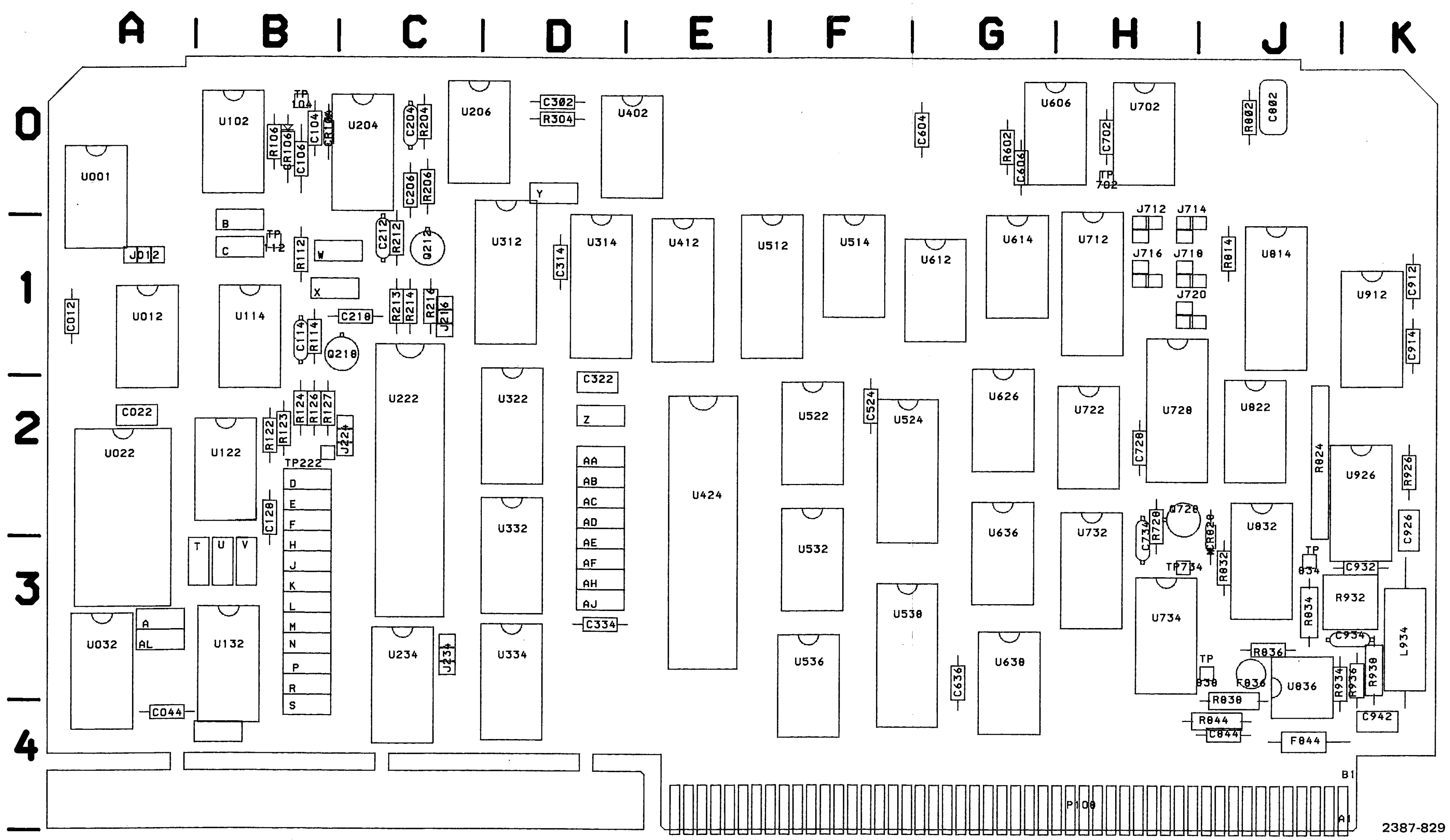


Fig. 8-20. MPU circuit board, assembly A54.

MPU A54

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

P/O A54 ASSY **READOUT/**

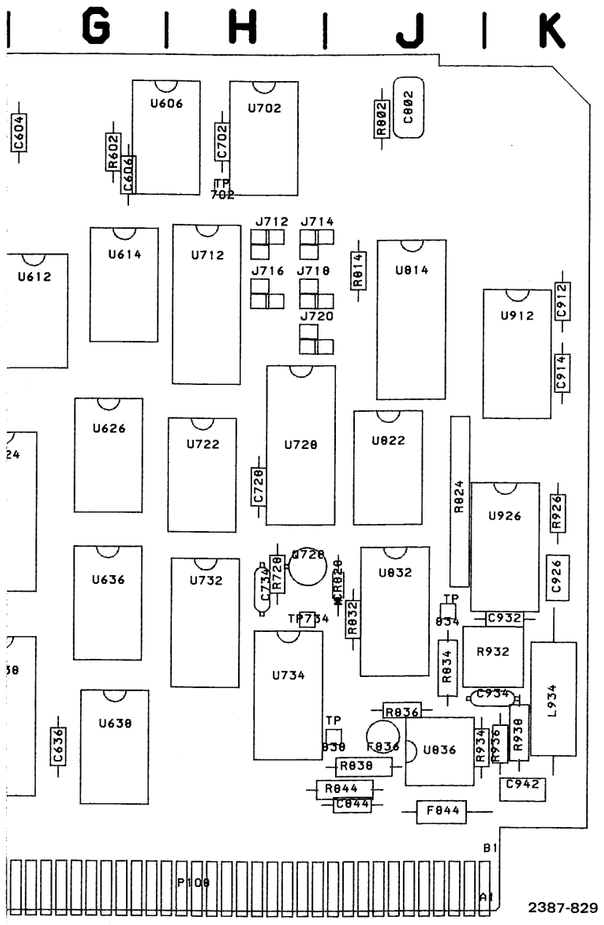
Circuit Number	Schematic Location	Board Location	Circuit Number
C012	A1	A1	R834
C022	A1	A2	R836
C044	A1	A4	R838
C104	A1	B0	R844
C128	A1	B2	R926
C206	C2	C0	R932
C218	A1	C1	R934
C302	B2	D0	R936
C314	B2	D1	R938
C322	A1	D2	TP104
C334	B2	D3	TP112
C524	C2	F2	TP702
C604	C2	G0	TP734
C606	C2	G0	TP834
C636	C2	G3	TP838
C702	D2	H0	U412
C728	B2	H2	U424
C734	C5	H2	U512
C844	B3	J4	U522A
C912	B2	K2	U524
C914	B2	K1	U532A
C926	A1	K2	U532C
C932	B3	K3	U536A
C934	A3	K3	U536B
C942	A1	K4	U536C
CR828	B6	J3	U536D
F836	A1	J3	U538
F844	A1	J4	U626A
L934	A1	K3	U626C
Q728	B6	H2	U626D
R206	C2	C0	U636A
R602	C2	G0	U636D
R728	C5	H2	U638A
R814	C2	J1	U638B
R824B	D3	J2	U638D
R824C	C3	J2	U814
R824D	C3	J2	U822A
R824E	C3	J2	U822B
R824F	D3	J2	U822C
R824G	C3	J2	U822D
R824H	C3	J2	U832
R824I	C3	J2	U836
R824J	C3	J2	U912
R832	B6	J3	U926

P/O A54 ASSY ALSO SHOWN ON 17

P/O A68 ASSY **READOUT/7**

Circuit Number	Schematic Location	Board Location	Circuit Number
J108	A1	C1	J108
J108	D5	C1	J108

A68 ASSY SHOWN IN FIG. 8-3



P/O A54 ASSY			READOUT/7K INTERFACE 19		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C012	A1	A1	R834	B3	J3
C022	A1	A2	R836	D3	J3
C044	A1	A4	R838	B3	J3
C104	A1	B0	R844	B3	J4
C128	A1	B2	R926	B2	K2
C206	C2	C0	R932	B3	K3
C218	A1	C1	R934	B3	K3
C302	B2	D0	R936	A3	K3
C314	B2	D1	R938	A3	K3
C322	A1	D2	TP104	A2	B0
C334	B2	D3	TP112	D2	B1
C524	C2	F2	TP702	A2	H0
C604	C2	G0	TP734	A2	H3
C606	C2	G0	TP834	B3	J3
C636	C2	G3	TP838	A2	J3
C702	D2	H0	U412	G1	E1
C728	B2	H2	U424	F3	E2
C734	C5	H2	U512	G2	F1
C844	B3	J4	U522A	G3	F2
C912	B2	K2	U524	G5	F2
C914	B2	K1	U532A	G3	F3
C926	A1	K2	U532C	G4	F3
C932	B3	K3	U536A	G4	F3
C934	A3	K3	U536B	G4	F3
C942	A1	K4	U536C	G4	F3
CR828	B6	J3	U536D	G4	F3
F836	A1	J3	U538	F5	F3
F844	A1	J4	U626A	E3	G2
L934	A1	K3	U626C	E4	G2
Q728	B6	H2	U626D	G6	G2
R206	C2	C0	U636A	H1	G3
R602	C2	G0	U636D	C5	G3
R728	C5	H2	U638A	G5	G3
R814	C2	J1	U638B	G3	G3
R824B	D3	J2	U638D	G5	G3
R824C	C3	J2	U814	D3	J1
R824D	C3	J2	U822A	D4	J2
R824E	C3	J2	U822B	B5	J2
R824F	D3	J2	U822C	B5	J2
R824G	C3	J2	U822D	A5	J2
R824H	C3	J2	U832	B6	J3
R824I	C3	J2	U836	B3	J3
R824J	C3	J2	U912	D4	K1
R832	B6	J3	U926	B4	K2

P/O A54 ASSY ALSO SHOWN ON 17 , 18

P/O A68 ASSY			READOUT/7K INTERFACE 19		
J108	A1	C1	J108	E5	C1
J108	D5	C1	J108	H1	C1

A68 ASSY SHOWN IN FIG. 8-31

J108 B1 +15V F836 1A +15V
B3 B4 +5.1V F844 5A L934 3.2µH C942 1µF C926 1µF
+5.1V TP112 +5.1V
C322 1µF C022 1µF C012 .01 C044 .01 C104 .01 C128 .01 C218 .01
C302 .01 C314 .01 C334 .01 C524 .01 C604 .01 C636 .01 C702 .01
C728 .01 C912 .01 R926 1K R206 1K R602 510 R814 1K
C914 .01 C206 .01 C606 .01 +V1 +V2 +V3 +V4
A48 TP838 GND
TP104 TP702 TP734 COM
+5.1V1 TO MPU MEMORY 16

COMPONENT NUMBER EXAMPLE
Component Number: A23 A2 R1234
Assembly Number · Subassembly Number (if used) · Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

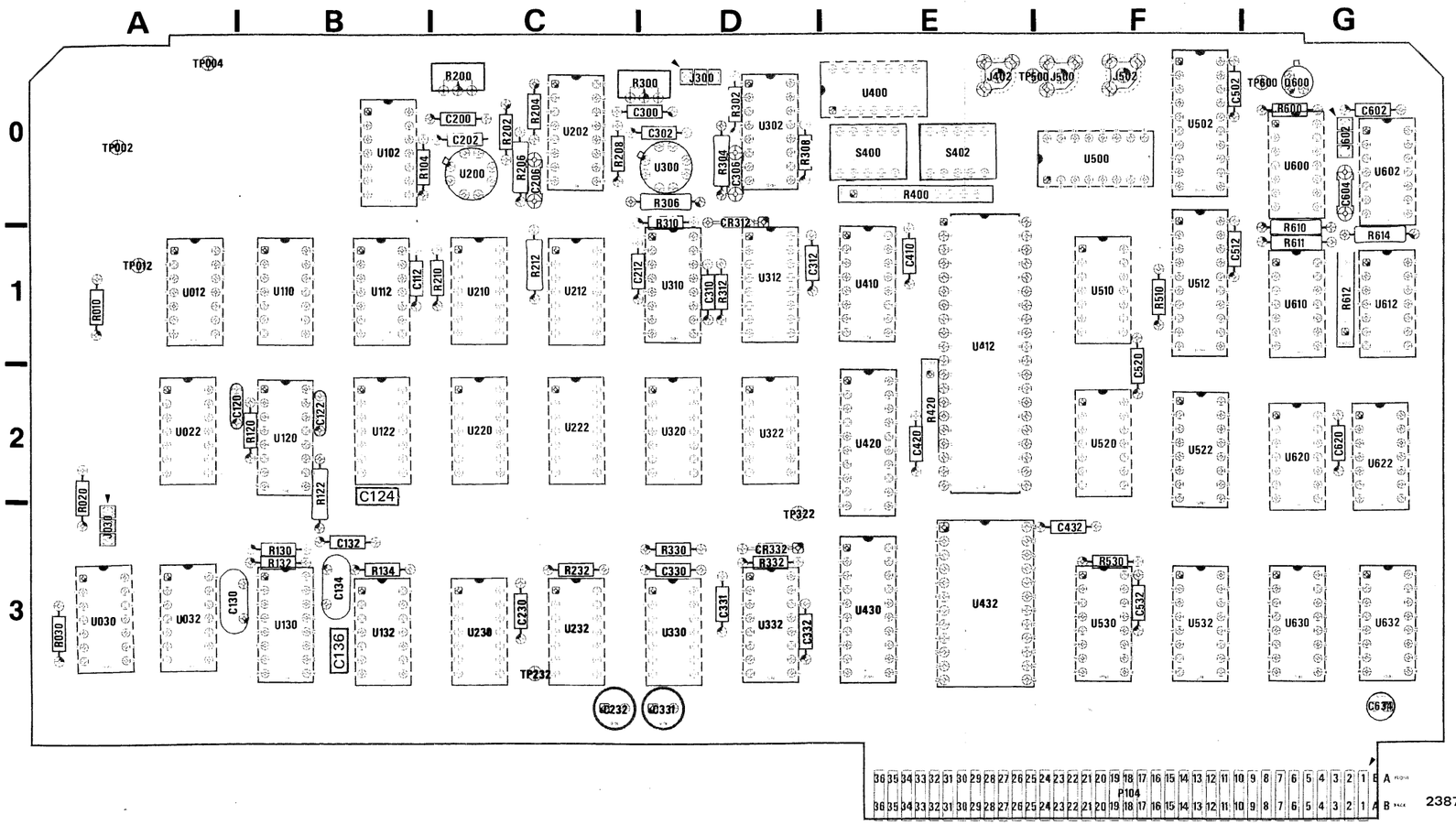
+15V R838 5.49K R844 8.25K C844 .01 U836 LM311
A50 ANALOG DATA R936 1K +15V C934 1000 R938 75.0K
R934 3.3K READOUT CENTERING R932 500 R834 5.11K TP834 RO +15V
C932 .01 +15V
U926 -0014-
R824U 4.7K R824I 4.7K R824H 4.7K R824G 4.7K R824F 4.7K
R824E 4.7K R824D 4.7K R824C 4.7K R824B 4.7K
+5.1V1 R836 4.7K
U814 74LS240
BD7 BD3 BD2 BD1 BD0
U912 74147
BADR4 PISEL ØEXX U822A 74LS32 ØEEF
BADR2 PISTROBE U626C 74LS32 ØEF8

A5 A12 A15 A35 A41 A49 B9 B18 B21 B24 B27 B30 B32 B37 B40 B43 B46 B49

U822D 74LS32 PISEL ØEXX STROBE PISTROBE
U822B 74LS32 BADR6 BADR5 ØEBF ØEDF
U822C 74LS32
U832 74LS175 BD3 BD2 BD1 BD0 RST NMIEN CR828 BLOKRST
C734 1000 R728 200 U636D 74LS04 TIMESLOT
Q728 R832 5.1K
SHIFT ROT RORST
J108 A23 A22 A25 A24
P/O MAIN INTERCON

+5.1V1 U626A 74LS32 PISEL BADR7 ØE7C PIASEL
BADR1 BADR0 U424 MB8820
IRQ BR/W CK2 RST D7 D6 D5 D4 D3 D2 D1 D0 BADR6
IRQA IRQB R/W EN RST CA1 CA2 PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0 PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0 CS0 CS1 CS2 RS1 RS0 CB2 CB1
U538 74LS273
7KSND U412 74LS273 U636A 74LS04
7KDIO8 7KDIO7 7KDIO6 7KDIO5 7KDIO4 7KDIO3 7KDIO2 7KDIO1
U512 74LS240
U522A 74LS74 U531A 74LS08
U638B 74LS33 7KDAV
U532C 74LS08
U536D 74LS33 7KEOI
U536B 74LS33 7KIFC
U536A 74LS33 7KATN
U536C 74LS33 7KREN
U638D 74LS33 7KLVADR
U638A 74LS33 7KRVADR
P/O U524 74LS240
U626D 74LS32 PISEL BADR3 ØEF4
J108 A40 A34 A27 7KNRFD 7KNDAC 7KSRQ
P/O MAIN INTERCON
P/O MPU BD. A54

2387-832



P/O A56 ASSY			IEEE
Circuit Number	Schematic Location	Board Location	Circuit Number
R400A	F3	E0	U222C
R400B	F3	E0	U302
R400C	F3	E0	U320B
R400D	F2	E0	U410
R400E	F4	E0	U410
R400E	F4	E0	U412
R400G	F4	E0	U412
R400H	F4	E0	U432
R400J	F4	E4	U500
R612D	F3	G1	U500
R612E	C1	G1	U502
S400	E2	E0	U512
S402	E4	E0	U522
U122B	C3	B2	U522
U132B	C5	B3	U610C
U220A	F6	C2	U610D
U220B	F6	C2	U612A

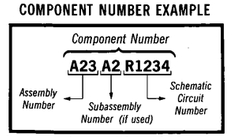
P/O A56 ASSY ALSO SHOWN ON 21

P/O A68 ASSY			IEEE
J104	B1	B0	J104

A68 ASSY SHOWN IN FIG. 8-3

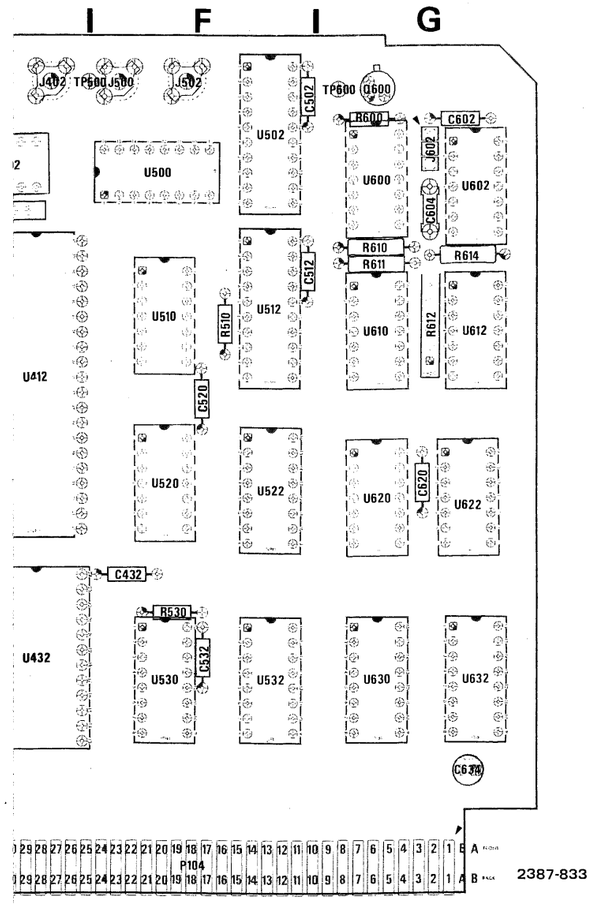
Fig. 8-21. IEEE 488 Interface circuit board, assembly A56.

COMPONENT NUMBER EXAMPLE

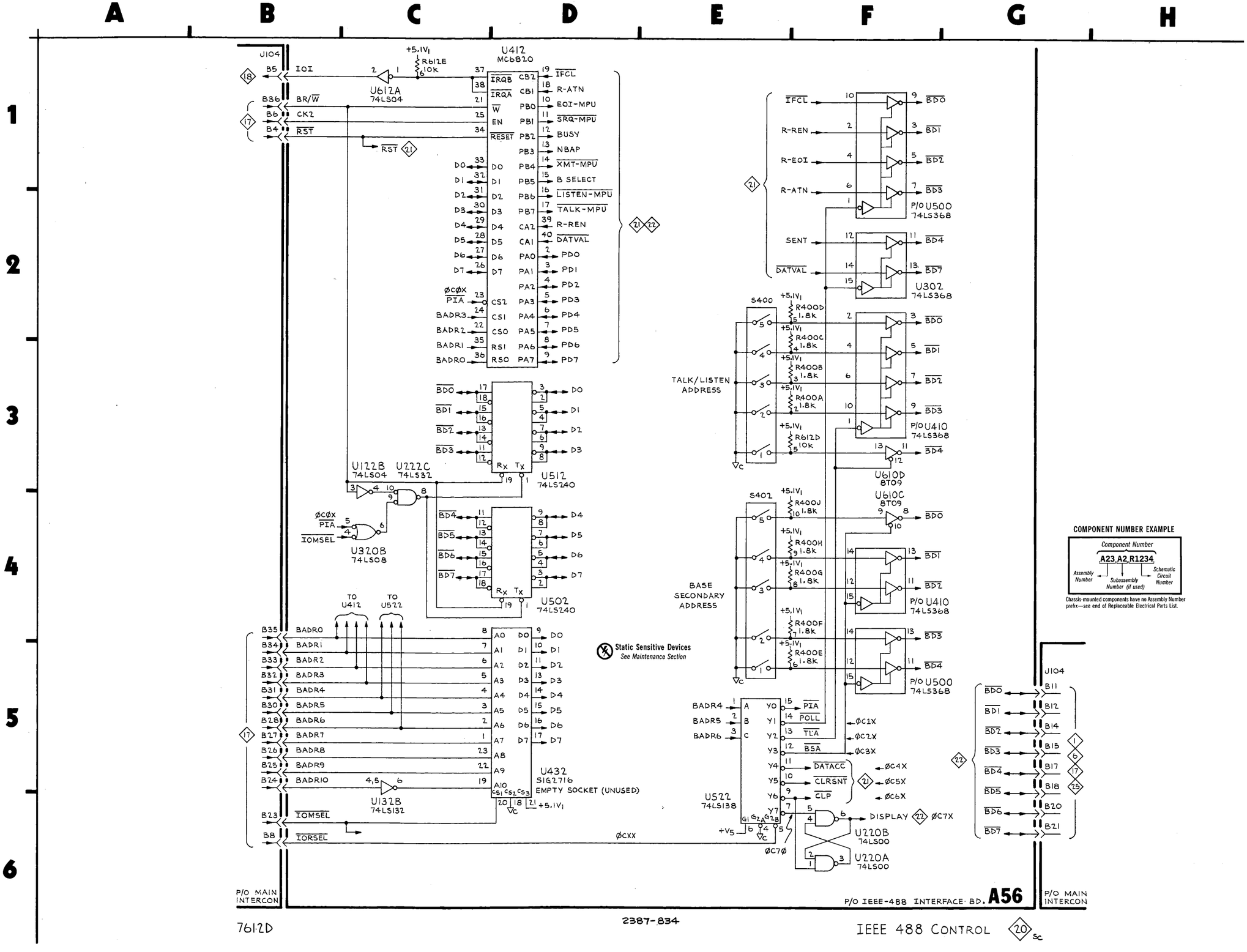


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



P/O A56 ASSY			IEEE 488 CONTROL ◇20		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
R400A	F3	E0	U222C	C3	C2
R400B	F3	E0	U302	F2	D0
R400C	F3	E0	U320B	C4	D2
R400D	F2	E0	U410	F3	E1
R400E	F4	E0	U410	F4	E1
R400E	F4	E0	U412	C4	E1
R400G	F4	E0	U412	D1	E1
R400H	F4	E0	U432	D5	E3
R400J	F4	E4	U500	F1	F0
R612D	F3	G1	U500	F5	F0
R612E	C1	G1	U502	D4	F1
S400	E2	E0	U512	D3	F1
S402	E4	E0	U522	C4	F2
U122B	C3	B2	U522	E5	F2
U132B	C5	B3	U610C	F4	G1
U220A	F6	C2	U610D	F3	G2
U220B	F6	C2	U612A	C1	G1
P/O A56 ASSY ALSO SHOWN ON ◇21 , ◇22					
P/O A68 ASSY			IEEE 488 CONTROL ◇20		
J104	B1	B0	J104	G5	B0
A68 ASSY SHOWN IN FIG. 8-31					



761-2D

2387-834

IEEE 488 CONTROL 20 SC

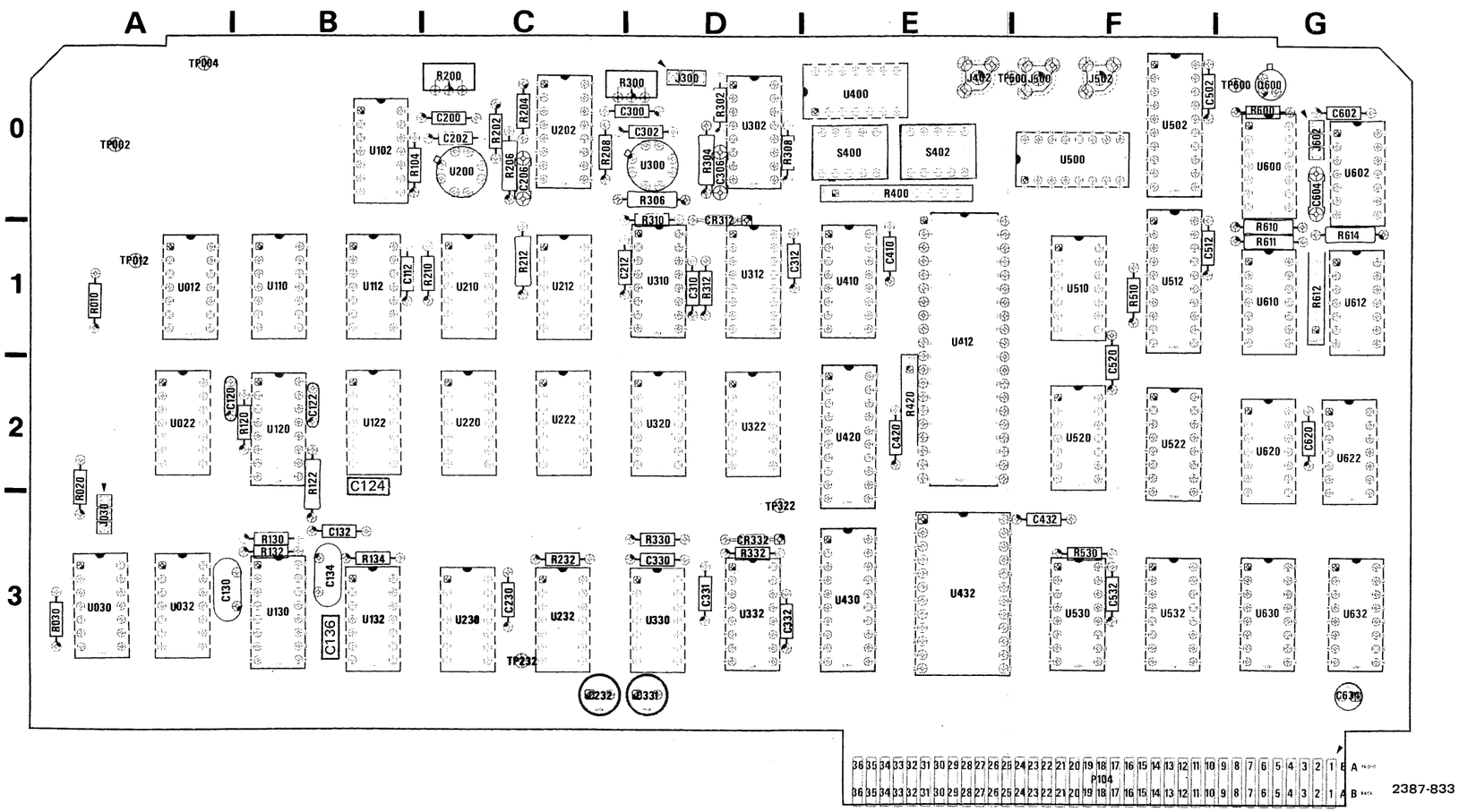
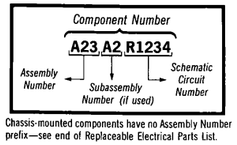


Fig. 8-22. IEEE 488 Interface circuit board, assembly A56.

COMPONENT NUMBER EXAMPLE

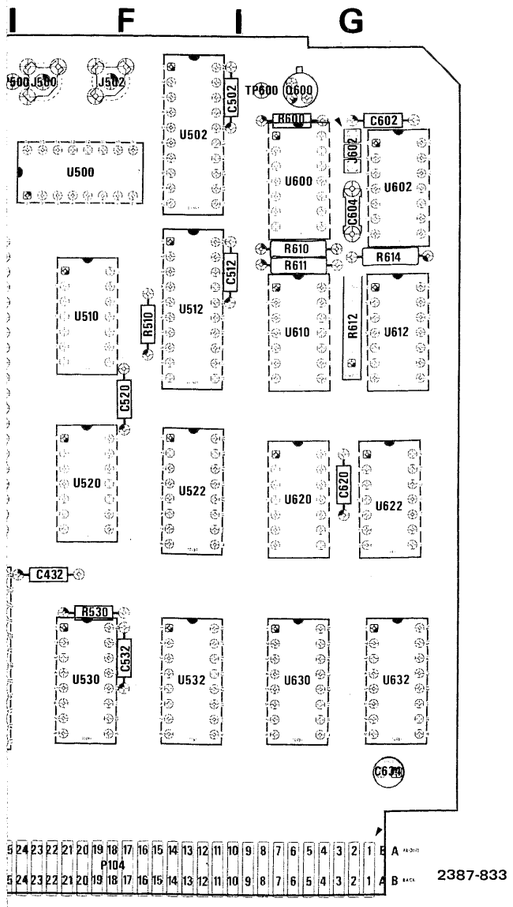


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

P/O A56 ASSY		
Circuit Number	**Schematic Location**	**Board Location**
C112	A5	B1
C124*	B3	B3
C130	D4	A3
C132	B5	B3
C134	D3	B3
C136*	A2	B3
C230	B5	C3
C232	A6	C3
C312	B5	D1
C330	B5	D3
C331	A6	D3
C410	C5	E1
C420	C5	E2
C432	A5	F3
C502	A5	F0
C512	B5	F1
C520	B5	F2
C532	B5	F3
C602	B5	G0
C620	C5	G2
C634	A5	G3
R010	G4	A1
R030	G4	A3
R130	A5	B3
R132	C4	B3
R134	D3	B3
R210	A5	C1
R232	B5	C3
R420B	A3	E2
R420C	F2	E2
R420D	D5	E2
R420E	D5	E2
R510	B5	F1
R530	B5	F3
R612B	G6	G1
TP002	D4	A0
TP004	B6	A0
TP012	D4	A1
TP232	H3	C3
TP322	A2	D3
TP500	B6	F0
TP600	F4	G0
U012A	D4	A1
U012B	E4	A1
U012C	C3	A1
U022A	D3	A2
U030A	G4	A3
U032A	E4	A3
U032B	D3	A3
U102A	F3	B0
U110A	C3	B1
U110B	D4	B1
U110D	B3	B1
P/O A56 ASSY ALSO SHOWN		
P/O A68 ASSY		
J104	A1	B0
A68 ASSY SHO		

*See Parts List for serial number ranges.



P/O A56 ASSY			IEEE 488 CONTROL 21		
Circuit Number	**Schematic Location**	**Board Location**	**Circuit Number**	**Schematic Location**	**Board Location**
C112	A5	B1	U112A	C3	B1
C124*	B3	B3	U112B	D4	B1
C130	D4	A3	U112C	E5	B1
C132	B5	B3	U112D	B3	B1
C134	D3	B3	U112F	G4	B1
C136*	A2	B3	U122A	B3	B2
C230	B5	C3	U122C	A3	B2
C232	A6	C3	U130A	C4	B3
C312	B5	D1	U130B	D3	B3
C330	B5	D3	U132A	E3	B3
C331	A6	D3	U132C	A2	B3
C410	C5	E1	U220C	B2	C2
C420	C5	E2	U220D	G4	C2
C432	A5	F3	U222A	B3	C2
C502	A5	F0	U222D	A3	C2
C512	B5	F1	U230A	G5	C3
C520	B5	F2	U230B	G5	C3
C532	B5	F3	U232A	G3	C3
C602	B5	G0	U232C	G3	C3
C620	C5	G2	U312	F5	D1
C634	A5	G3	U320A	C3	D2
R010	G4	A1	U320D	C3	D2
R030	G4	A3	U330A	G4	D3
R130	A5	B3	U400A	G4	E0
R132	C4	B3	U400B	G4	E0
R134	D3	B3	U420	B2	E2
R210	A5	C1	U510	G1	F1
R232	B5	C3	U520	G2	F2
R420B	A3	E2	U530	G2	F3
R420C	F2	E2	U532	G1	F3
R420D	D5	E2	U600A	B3	G0
R420E	D5	E2	U600C	F5	G0
R510	B5	F1	U602A	B4	G0
R530	B5	F3	U602B	B3	G1
R612B	G6	G1	U602B	F5	G0
TP002	D4	A0	U610A	F4	G1
TP004	B6	A0	U610B	F4	G1
TP012	D4	A1	U612B	G2	G2
TP232	H3	C3	U612C	D5	G2
TP322	A2	D3	U612D	D5	G1
TP500	B6	F0	U612E	E5	G2
TP600	F4	G0	U612F	G6	G1
U012A	D4	A1	U620A	D6	G2
U012B	E4	A1	U620B	F3	G2
U012C	C3	A1	U620C	E4	G2
U022A	D3	A2	U620D	E5	G2
U030A	G4	A3	U622A	E3	G2
U032A	E4	A3	U622B	E5	G2
U032B	D3	A3	U622C	D6	G2
U102A	F3	B0	U622D	D6	G2
U110A	C3	B1	U630	G5	G3
U110B	D4	B1	U632	G6	G3
U110D	B3	B1			

P/O A56 ASSY ALSO SHOWN ON 21 , 22

P/O A68 ASSY			IEEE 488 CONTROL 20		
J104	A1	B0	J104	H1	B0

A68 ASSY SHOWN IN FIG. 8-31

*See Parts List for serial number ranges.

A B C D E F G H

1 2 3 4 5 6

J104 A24 HD0 · A25 HD1 · A27 HD2 · A28 HD3 · A29 HD4 · A30 HD5 · A32 HD6 · A33 HD7 · A36 LSEND · A2 A5 B7 A9 B10 B13 A15 B16 B19 B22 A26 B29 A31 Vc · B1 +5.1V1 · B9 STROBE (UNUSED) · B2 +15V · B3 -15V · P/O MAIN INTERCON

U420 74LS374 (HD0–HD7 → PD0–PD7)

U132C 74LS132 · LSEND · C136 150 · TP322 · SEND

U220C 74LS00 · U122C 74LS04 · U222A 74LS32 · U222D 74LS32 · XMT-MPU · R-ATN · R420B 10K · +5.1V1

U112D 74LS04 · U602B 74LS10 · U320D · U320A 74LS08 · RST · CLP · U022A 74LS74 · C124 .0022 · CKSNT

U122A 74LS04 · U110D 74LS08 · U600A 74LS11 · U112A 74LS04 · U110A 74LS08 · U602A 74LS10 · DATA-OUT-EN · PFCA · SENT · NBAP · TALK-MPU

U012C 74LS02 · U130B 9602 · R134 10K · C134 105 · TP007 · U032B 74LS74 · U012B 74LS02 · U110B 74LS08 · U032A 74LS74 · U620C 74LS08 · U012A 74LS02 · U112B 74LS04 · U130A 9602 · R132 5.1K · C130 470 · R-NRFD · R-NDAC · TP012

U510 74LS242 · U520 74LS242 · R420C 10K · TALK-MPU · DATA-OUT-EN · U612B 74LS04

U532 MC3448 · U530 MC3448 · DIO1 DIO2 DIO3 DIO4 DIO5 DIO6 DIO7 DIO8 · AI3 AI2 AI1 AI0 AI7 AI8 AI9 A20 · +V4

U622A 74LS02 · R-NDAC · U132A 74LS132 · U620B 74LS08 · RST · CLRSNT · U102A 74LS74 · TALK-MPU · SENT · U610B 8T09 · U610A 8T09 · T-DAV · TP600 · EOI-MPU · DAV · EOI · DATA-OUT-EN

U232C 74S140 · PSENT · DSENT · Y SENT · A35 · TP232 · U232A 74S140 · R-REN · A14

U330A 74LS74 · DATACC · T-NDAC · U230B 74LS08 · U112F 74LS04 · BTNDAC · A23 · R010 390 · U220D 74LS00 · R-DAV · DATVAL · AH-EN · R-ATN · BUSY · T-NRFD · U400B 74LS00 · U400A 74LS00 · U230A 74LS08 · U030A 74LS266 · BTNRFD · A21 · R030 390

U612E 74LS04 · R-IFC · U600C 74LS11 · PFCA · U602B 74LS10 · DATA-OUT-EN · TALK-MPU · U612D 74LS04 · R420E 10K · U612C 74LS04 · R420D 10K · LISTEN-MPU · U112C 74LS04 · R-ATN · U622C 74LS02 · U620D 74LS08 · U622B 74LS02 · AH-EN · P/O U312 74LS368 · IFCL · U620A 74LS08 · U622D 74LS02

U630 MC3441 · R-EOI R-DAV R-NRFD T-NRFD R-NDAC T-NDAC AH-EN · EOI DAV NRFD NDAC · A8 A7 A6 A4

U632 MC3441 · R-ATN R-REN R-IFC SRQ-MPU · ATN REN IFC SRQ · A16 A22 A3 A1 · R612B 10K · T-SRQ · U612F 74LS04

TP004 · TP500 · +5.1V1

COMPONENT NUMBER EXAMPLE
Component Number: A23 A2 R1234
Assembly Number · Subassembly Number (if used) · Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

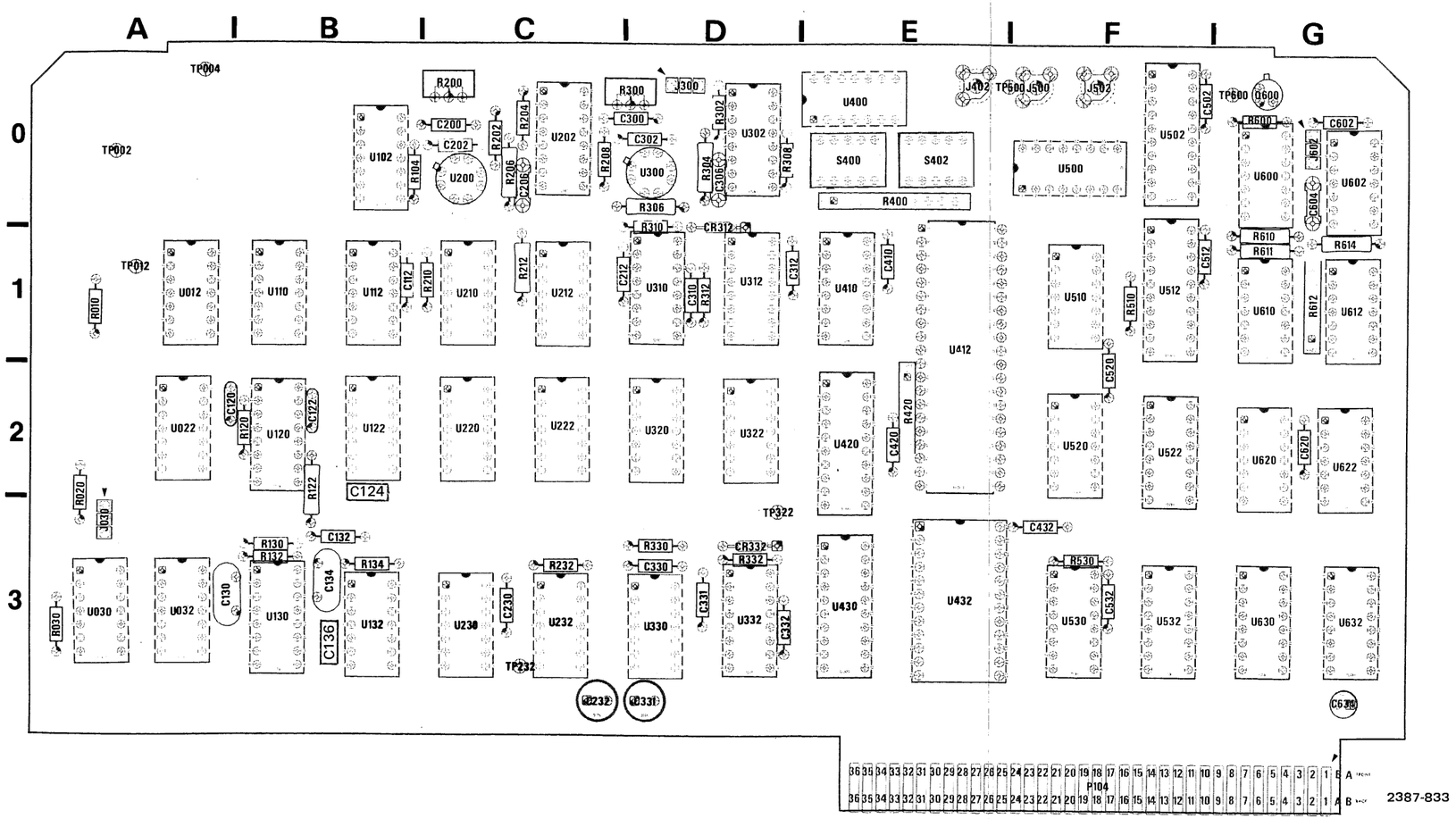
Static Sensitive Devices — See Maintenance Section

P/O IEEE-488 INTERFACE BD. A56

7612D

2387-835

IEEE 488 HANDSHAKE 21 Sc



2387-833

Fig. 8-23. IEEE 488 Interface circuit board, assembly A56.

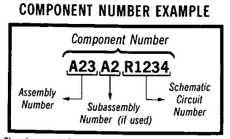
P/O A56 ASSY			IEEE 48
Circuit Number	**Schematic Location**	**Board Location**	**Circuit Number**
C120	C4	B2	R312
C122	C3	B2	R330
C200	F4	C0	R332
C202	G5	C0	R600
C206	G5	C0	R610
C212	F3	C1	R611
C300	F2	D0	R614
C306	G3	D0	U022B
C310	F2	D1	U030B
C331	F5	D3	U030C
C332	F4	D3	U030D
C604	G6	G0	U112E
CR312	F3	D0	U120A
CR332	F4	D2	U120B
P030	B6	A3	U122D
P300	F6	D0	U122E
P402	H3	E0	U122F
P500	H5	F0	U200
P502	G6	F0	U202
P602	G6	G0	U210A
Q600	G6	G0	U210B
R020	B5	A2	U212A
R104	G5	B0	U212B
R120	C3	B2	U222B
R122	C3	B2	U300
R200	F4	C0	U302
R202	G5	C0	U310
R204	F6	C0	U312
R206	G5	C0	U320C
R208	G3	C0	U322A
R212	F5	C1	U322B
R300	F2	D0	U322C
R302	F6	D0	U322D
R304	G3	D0	U330B
R306	F3	D0	U332
R308	G3	D0	U430
R310	F2	D0	U600B

A56 ASSY ALSO SHOWN ON 20

P/O A68 ASSY			IEEE 48
J104	A1	B0	J104

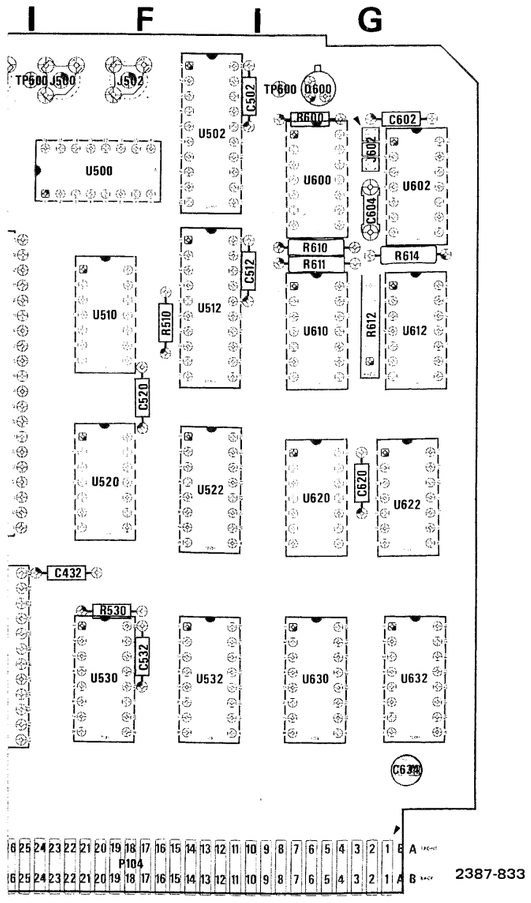
A68 ASSY SHOWN IN FIG. 8-3

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



P/O A56 ASSY			IEEE 488 HANDSHAKE ◇22		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C120	C4	B2	R312	F3	D1
C122	C3	B2	R330	F4	D3
C200	F4	C0	R332	F4	D3
C202	G5	C0	R600	G6	G0
C206	G5	C0	R610	F6	G1
C212	F3	C1	R611	F5	G1
C300	F2	D0	R614	G6	G1
C306	G3	D0	U022B	D3	A2
C310	F2	D1	U030B	B5	A3
C331	F5	D3	U030C	B5	A3
C332	F4	D3	U030D	B4	A3
C604	G6	G0	U112E	B4	C1
CR312	F3	D0	U120A	C4	B2
CR332	F4	D2	U120B	C3	B2
P030	B6	A3	U122D	C6	B2
P300	F6	D0	U122E	E4	B2
P402	H3	E0	U122F	D2	B2
P500	H5	F0	U200	G5	C0
P502	G6	F0	U202	F1	C0
P602	G6	G0	U210A	D2	C1
Q600	G6	G0	U210B	D3	C1
R020	B5	A2	U212A	E1	C1
R104	G5	B0	U212B	D2	C1
R120	C3	B2	U222B	D4	C2
R122	C3	B2	U300	G3	D0
R200	F4	C0	U302	H1	D0
R202	G5	C0	U310	F3	D1
R204	F6	C0	U312	G2	D1
R206	G5	C0	U320C	D4	D2
R208	G3	C0	U322A	B5	D2
R212	F5	C1	U322B	B5	D2
R300	F2	D0	U322C	B6	D2
R302	F6	D0	U322D	B5	D2
R304	G3	D0	U330B	E3	D3
R306	F3	D0	U332	F5	D3
R308	G3	D0	U430	C5	E3
R310	F2	D0	U600B	D6	G0

A56 ASSY ALSO SHOWN ON ◇20 , ◇22

P/O A68 ASSY			IEEE 488 HANDSHAKE ◇21		
J104	A1	B0	J104	H1	B0

A68 ASSY SHOWN IN FIG. 8-31

TYPE	+5.1V	COM
74LS00	14	7
74LS02	14	7
74LS04	14	7
74LS08	14	7
74LS10	14	7
74LS11	14	7
74LS32	14	7
74LS74	14	7
74LS132	14	7
74LS138	16	8
74S140	14	7
74LS240	20	10
74LS242	14	7
74LS266	14	7
74LS367	16	8
74LS368	16	8
74LS374	20	10
74393	14	7
8T09	14	7
9602	16	8
SIG2716	21,24	12
MC3441	16	8
MC3448	16	8
MC6820	20	1

U212A 74393 · U212B 74393 · U202 74LS367 · U302 74LS368 · U312 74LS368 · U122F 74LS04 · U210A 74LS74 · U210B 74LS74 · U022B 74LS74 · U330B 74LS74 · U120B 9602 · U120A 9602 · U222B 74LS32 · U320C 74LS08 · U122E 74LS04 · U112E 74LS04 · U030D 74LS266 · U030B 74LS266 · U030C 74LS266 · U322A 74LS266 · U322B 74LS266 · U322D 74LS266 · U322C 74LS266 · U122D 74LS04 · U600B 74LS11 · U430 74LS374 · U310 MC3410 · U332 MC3410 · U300 LF356 · U200 LF356 · Q600 · P030 · P300 · P602 · P402 · P500 · P502

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234 (Assembly Number · Subassembly Number (if used) · Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices — See Maintenance Section

P/O IEEE 488 INTERFACE BD. **A56**

2387-836

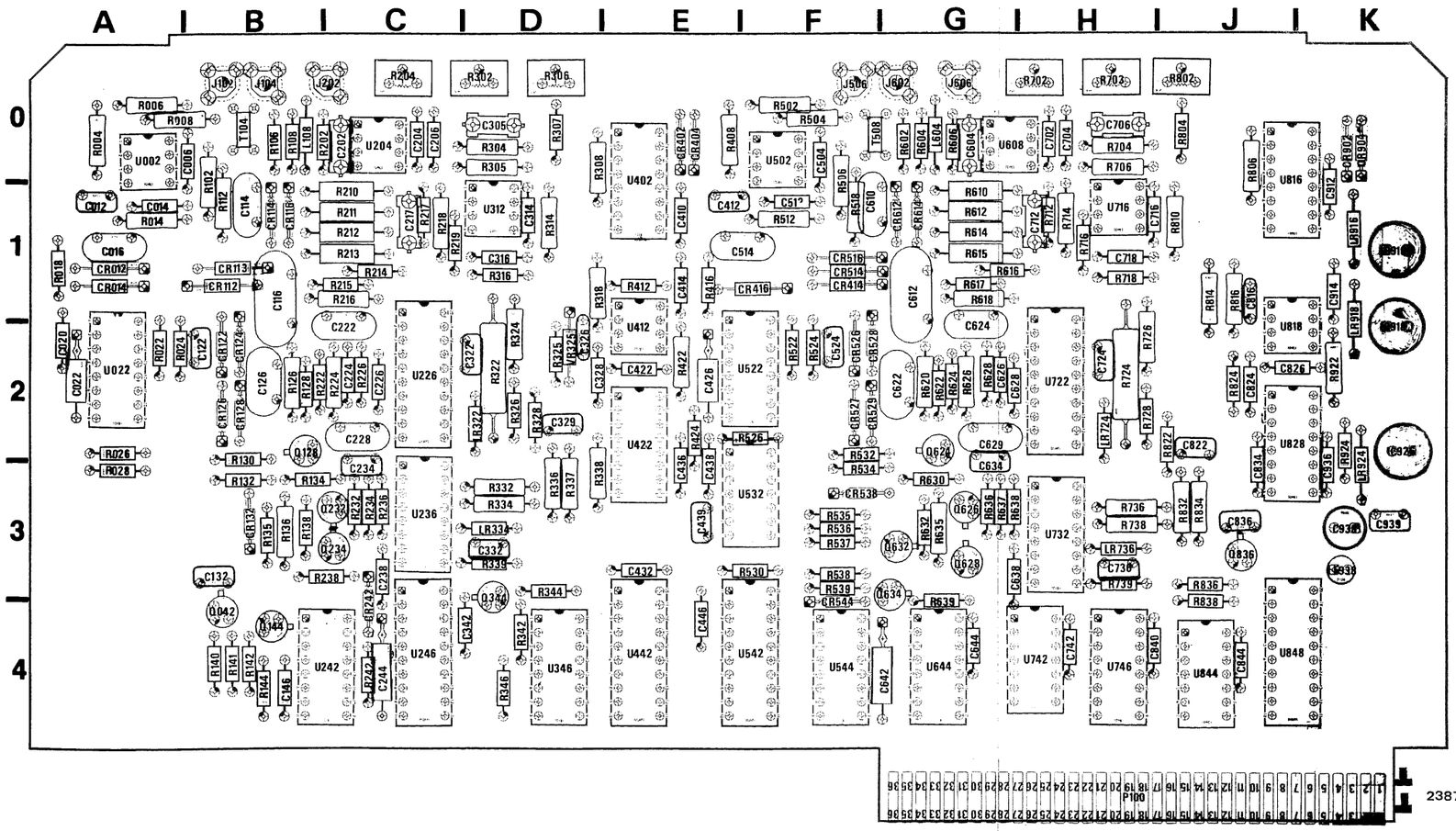


Fig. 8-24. Trigger circuit board, assembly A62.

TRIGGER A62

P/O A62 ASSY

Circuit Number	Schematic Location	Board Location	Circuit Number
C412	C2	E2	R539
C426	D2	E2	R602
C514	B3	F1	R604
C524	C4	F2	R606
C604	A4	G0	R610
C610	B4	F1	R612
C612	B5	G1	R614
C622	C5	G2	R615
C624	B4	G2	R616
C626	G6	G2	R617
C628	D4	G2	R618
C629	E6	G2	R620
C634	E4	G2	R622
C638	F5	H3	R624
C642	G4	G4	R626
C706	E2	H0	R628
C712	C3	H1	R630
C724	D3	H2	R632
C736	E4	H3	R635
C816	D1	J1	R636
C822	E5	J2	R637
C826	C2	J2	R638
C836	G5	J3	R639
C936	B1	K2	R702
CR414	C2	F1	R703
CR416	C2	E1	R704
CR514	C3	F1	R706
CR516	C3	F1	R712
CR526	C5	F2	R714
CR527	C5	F2	R716
CR528	C4	F2	R718
CR529	C4	F2	R724
CR538	E5	F3	R726
CR544	G4	F4	R728
CR612	B4	G1	R736
CR614	B4	G1	R738
CR902	D1	K0	R739
CR904	D1	K0	R802
E522	C3	F2	R804
L604	B4	G0	R806
L724	D3	H2	R810
L736	E4	H3	R814
P506	A2	F0	R816
P602	A3	G0	R822
P606	A4	G0	R824
Q624	E6	G2	R832
Q626	F4	G3	R834
Q628	F5	G3	R836
Q632	G4	G3	R838
Q634	G4	G3	R922
Q836	G5	J3	R924
R408	C2	E0	T508
R502	B2	F0	U502
R504	B2	F0	U522A
R506	B3	F0	U522B
R512	B3	F1	U522C
R518	B3	F1	U544A
R522	C4	F2	U608
R524	C4	F2	U716
R526	D2	F2	U722
R530	C3	F3	U732
R532	E5	F2	U746C
R534	E6	F3	U746E
R535	F5	F3	U816A
R536	G4	F3	U818
R537	G4	F3	U828
	G4	F3	

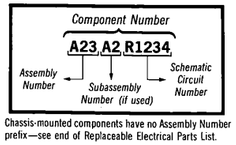
P/O A62 ASSY ALSO SHOWN ON 24

P/O A68 ASSY

J100	H4	B0	——

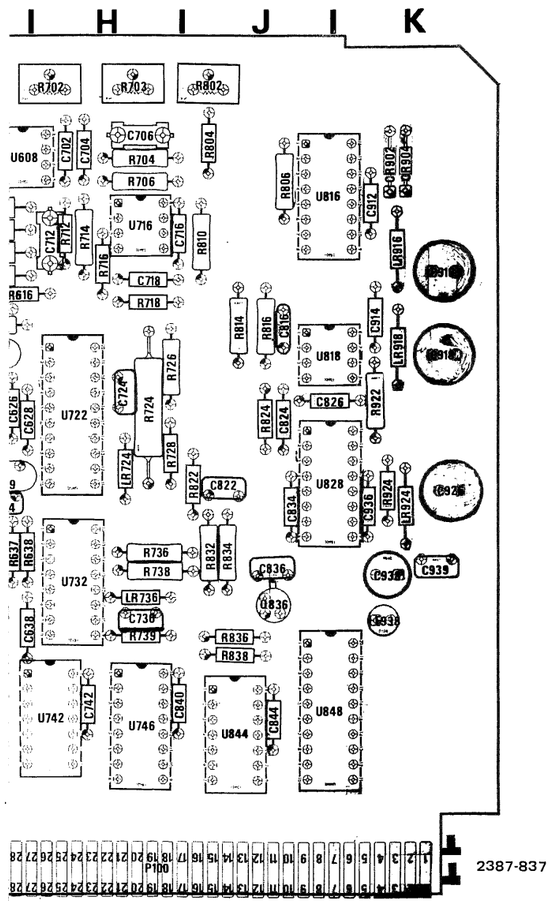
A68 ASSY SHOWN IN FIG. 8-

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

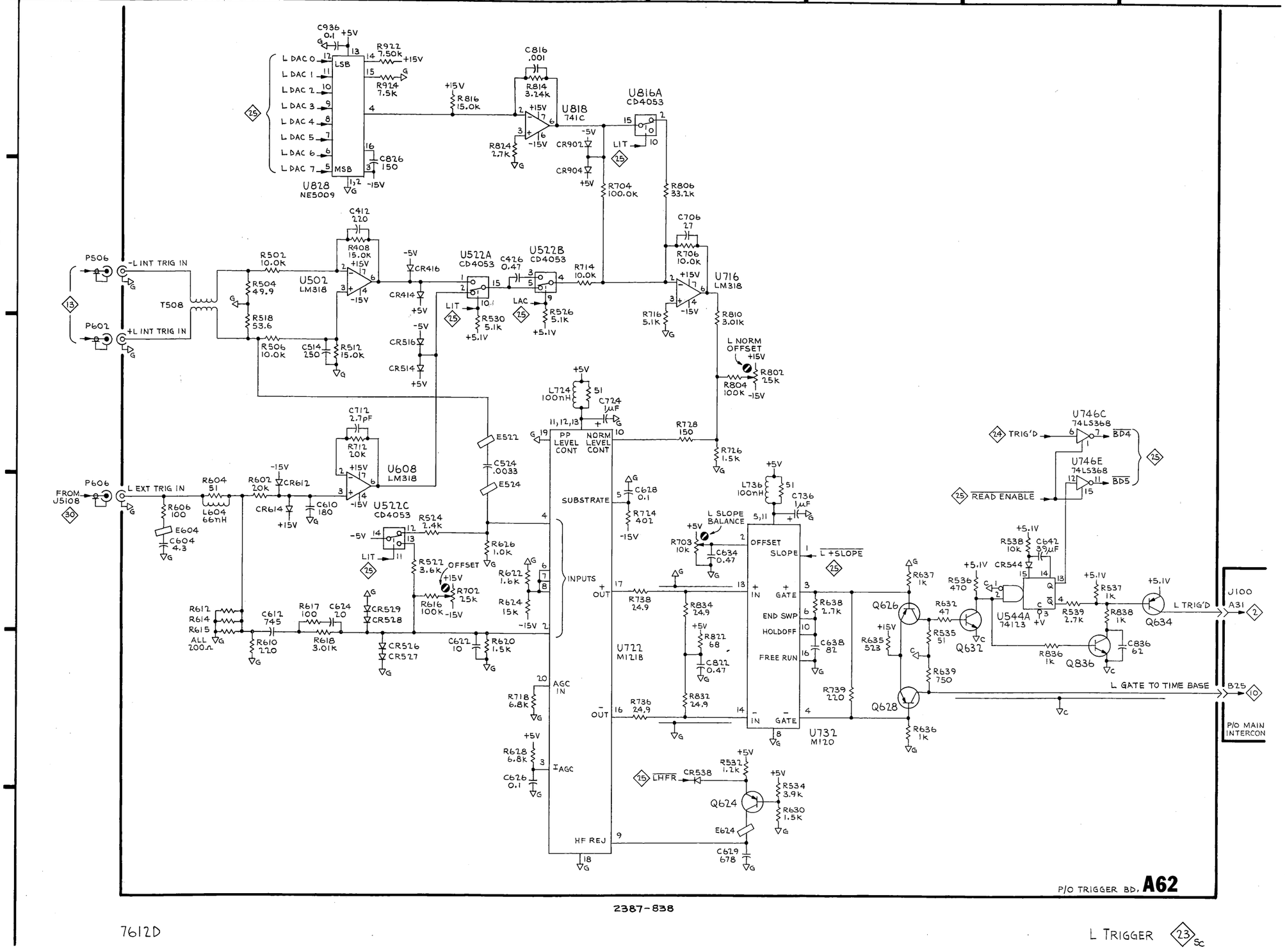


P/O A62 ASSY				L TRIGGER 23	
Circuit Number	**Schematic Location**	**Board Location**	**Circuit Number**	**Schematic Location**	**Board Location**
C412	C2	E2	R539	G4	F3
C426	D2	E2	R602	B4	G0
C514	B3	F1	R604	B4	G0
C524	C4	F2	R606	A4	G0
C604	A4	G0	R610	B5	G1
C610	B4	F1	R612	B4	G1
C612	B5	G1	R614	B4	G1
C622	C5	G2	R615	B5	G1
C624	B4	G2	R616	C4	G1
C626	G6	G2	R617	B4	G1
C628	D4	G2	R618	B5	G1
C629	E6	G2	R620	C5	G2
C634	E4	G2	R622	D4	G2
C638	F5	H3	R624	D4	G2
C642	G4	G4	R626	C4	G2
C706	E2	H0	R628	D5	G2
C712	C3	H1	R630	E6	G3
C724	D3	H2	R632	F4	G3
C736	E4	H3	R635	F5	G3
C816	D1	J1	R636	F5	G3
C822	E5	J2	R637	F4	G3
C826	C2	J2	R638	F4	G3
C836	G5	J3	R639	F5	G3
C936	B1	K2	R702	C4	H0
CR414	C2	F1	R703	E4	H0
CR416	C2	E1	R704	D2	H0
CR514	C3	F1	R706	E2	H0
CR516	C3	F1	R712	C3	H1
CR526	C5	F2	R714	D2	H1
CR527	C5	F2	R716	E3	H1
CR528	C4	F2	R718	D5	H1
CR529	C4	F2	R724	D4	H2
CR538	E5	F3	R726	E3	H2
CR544	G4	F4	R728	E3	H2
CR612	B4	G1	R736	D5	H3
CR614	B4	G1	R738	D4	H3
CR902	D1	K0	R739	F5	H3
CR904	D1	K0	R802	E3	J0
E522	C3	F2	R804	E4	J0
L604	B4	G0	R806	E2	J0
L724	D3	H2	R810	E3	J1
L736	E4	H3	R814	D1	J1
P506	A2	F0	R816	C1	J1
P602	A3	G0	R822	E5	J2
P606	A4	G0	R824	D1	J2
Q624	E6	G2	R832	E5	J3
Q626	F4	G3	R834	E4	J3
Q628	F5	G3	R836	G5	J3
Q632	G4	G3	R838	G4	J4
Q634	G4	G3	R922	C1	K2
Q836	G5	J3	R924	C1	K2
R408	C2	E0	T508	B2	F0
R502	B2	F0	U502	B2	F0
R504	B2	F0	U522A	C2	F2
R506	B3	F0	U522B	D2	F2
R512	B3	F1	U522C	C4	F2
R518	B3	F1	U544A	G4	F4
R522	C4	F2	U608	C4	G0
R524	C4	F2	U716	E2	H1
R526	D2	F2	U722	D5	H2
R530	C3	F3	U732	E5	H3
R532	E5	F2	U746C	G3	H4
R534	E6	F3	U746E	G4	H4
R535	F5	F3	U816A	D1	J0
R536	G4	F3	U818	D1	J1
R537	G4	F3	U828	B1	J2
	G4	F3			

P/O A62 ASSY ALSO SHOWN ON 24 , 25

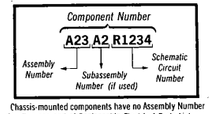
P/O A68 ASSY				L TRIGGER 23	
J100	H4	B0	——	——	——

A68 ASSY SHOWN IN FIG. 8-31



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

2387-838

7612D

L TRIGGER 23 Sc

L TRIGGER

23

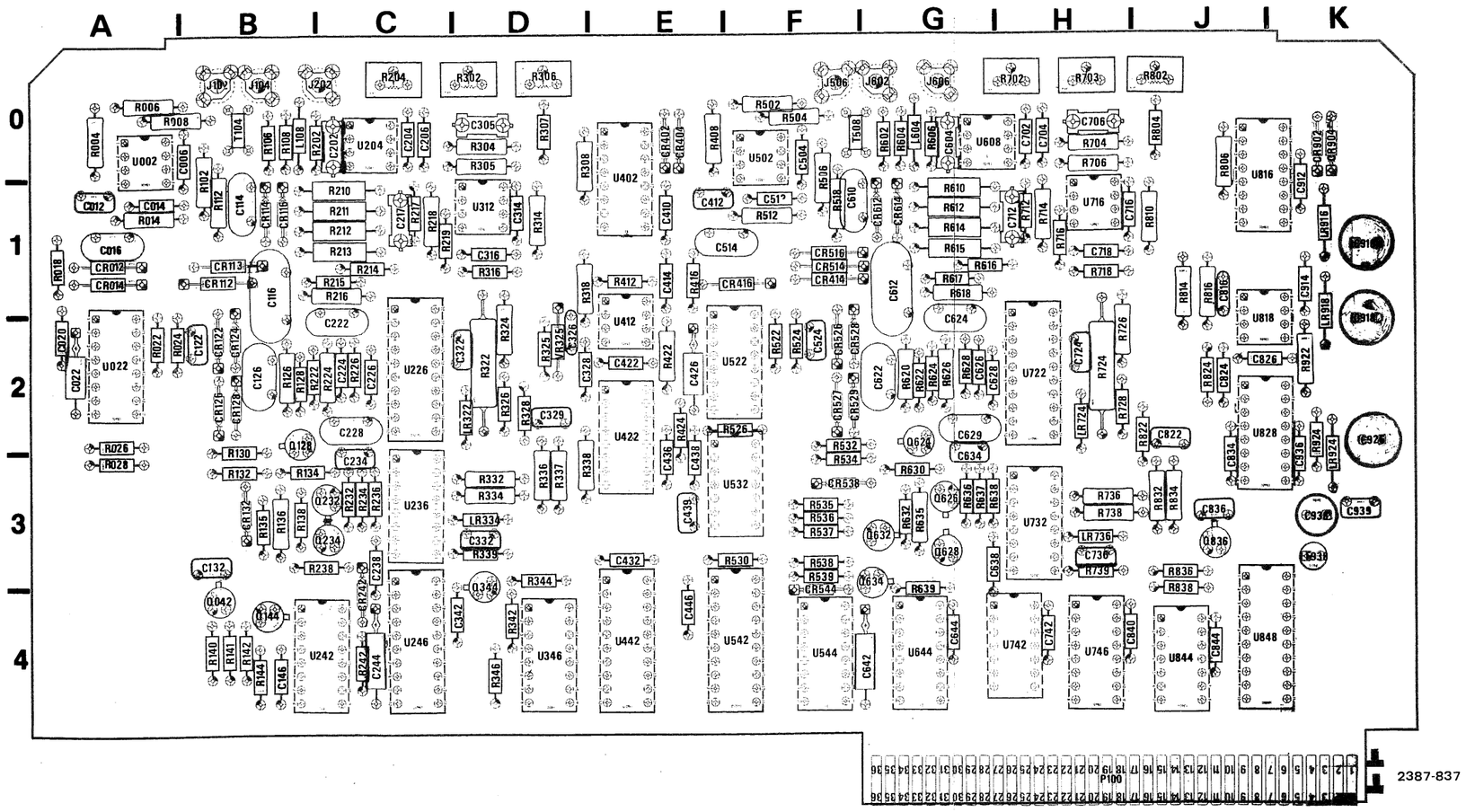
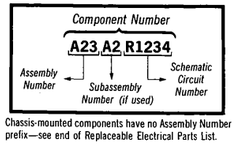


Fig. 8-25. Trigger circuit board, assembly A62.

TRIGGER A62

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

P/O A62 ASSY

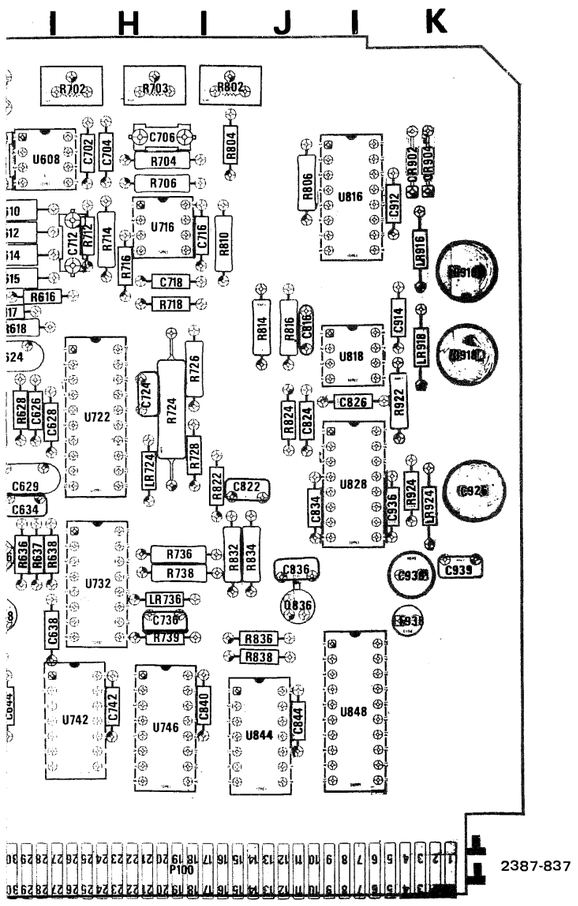
Circuit Number	Schematic Location	Board Location	Circuit Number
C012	C2	A1	R132
C016	B3	A1	R134
C022	D2	A2	R135
C114	B4	B1	R136
C116	B4	B1	R138
C122	D3	B2	R140
C126	C5	B2	R141
C132	G5	B3	R142
C202	A4	C0	R202
C217	C3	C1	R204
C222	C4	C2	R210
C224	D5	C2	R211
C226	D4	C2	R212
C228	E6	C2	R213
C234	E4	C3	R214
C238	F5	C3	R215
C244	G4	C4	R216
C305	E2	D0	R217
C322	D3	D2	R218
C326	D1	D2	R219
C329	E5	D2	R222
C332	E4	D3	R224
C422	C2	E2	R226
C436	C1	E3	R232
CR012	C2	A1	R234
CR014	C2	A1	R236
CR112	C3	B1	R238
CR113	C3	B1	R242
CR114	B4	B1	R302
CR116	B4	B1	R304
CR122	C5	B2	R305
CR124	C4	B2	R306
CR126	C5	B2	R307
CR128	C4	B2	R308
CR132	E5	B3	R314
CR242	G4	C4	R316
CR402	D1	E0	R318
CR404	D1	E0	R322
L108	B4	B0	R324
L322	D3	D2	R326
L334	E4	D3	R328
P102	A2	B0	R332
P104	A3	B0	R334
P202	A4	C0	R336
Q042	G5	B4	R337
Q128	E6	B2	R338
Q144	G4	B4	R339
Q232	F4	C3	R342
Q234	F5	C3	R344
Q344	H4	D4	R412
R004	C2	A0	R422
R006	B2	A0	R424
R008	B2	A0	T104
R014	C3	A1	U002
R022	C4	A2	U022A
R024	C4	A2	U022B
R026	D2	A2	U022C
R028	C2	A3	U204
R102	B3	B0	U226
R106	B4	B0	U236
R108	B4	B0	U242A
R112	B3	B1	U312
R126	D5	B2	U402A
R128	D4	B2	U412
R130	E5	B2	U422

P/O A62 ASSY ALSO SHOWN ON 2

P/O A68 ASSY

J100	H4	B0	——

A68 ASSY SHOWN IN FIG. 8



P/O A62 ASSY				R TRIGGER ◇24	
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C012	C2	A1	R132	E5	B3
C016	B3	A1	R134	E6	B3
C022	D2	A2	R135	F4	B3
C114	B4	B1	R136	F4	B3
C116	B4	B1	R138	F4	B3
C122	D3	B2	R140	G5	B4
C126	C5	B2	R141	G4	B4
C132	G5	B3	R142	G4	B4
C202	A4	C0	R202	A4	C0
C217	C3	C1	R204	C4	C0
C222	C4	C2	R210	B5	C1
C224	D5	C2	R211	B4	C1
C226	D4	C2	R212	B4	C1
C228	E6	C2	R213	B4	C1
C234	E4	C3	R214	C4	C1
C238	F5	C3	R215	B4	C1
C244	G4	C4	R216	B4	C1
C305	E2	D0	R217	C3	C1
C322	D3	D2	R218	D2	C1
C326	D1	D2	R219	E2	C1
C329	E5	D2	R222	D4	B2
C332	E4	D3	R224	D4	C2
C422	C2	E2	R226	D5	C2
C436	C1	E3	R232	F5	C3
CR012	C2	A1	R234	F4	C3
CR014	C2	A1	R236	F4	C3
CR112	C3	B1	R238	F5	C3
CR113	C3	B1	R242	G4	C4
CR114	B4	B1	R302	E4	D0
CR116	B4	B1	R304	D2	D0
CR122	C5	B2	R305	E2	D0
CR124	C4	B2	R306	E3	D0
CR126	C5	B2	R307	E3	D0
CR128	C4	B2	R308	E2	D0
CR132	E5	B3	R314	E2	D1
CR242	G4	C4	R316	D5	D1
CR402	D1	E0	R318	D1	D1
CR404	D1	E0	R322	D4	D2
L108	B4	B0	R324	E3	D2
L322	D3	D2	R326	E3	D2
L334	E4	D3	R328	E5	D2
P102	A2	B0	R332	D5	D3
P104	A3	B0	R334	D4	D3
P202	A4	C0	R336	E5	D3
Q042	G5	B4	R337	E4	D3
Q128	E6	B2	R338	D1	D3
Q144	G4	B4	R339	F5	C3
Q232	F4	C3	R342	G4	D4
Q234	F5	C3	R344	H4	D3
Q344	H4	D4	R412	D1	E1
R004	C2	A0	R422	C1	E2
R006	B2	A0	R424	C1	E2
R008	B2	A0	T104	B2	B0
R014	C3	A1	U002	C2	A2
R022	C4	A2	U022A	C2	A2
R024	C4	A2	U022B	D2	A2
R026	D2	A2	U022C	C4	A2
R028	C2	A3	U204	C4	C0
R102	B3	B0	U226	D4	C2
R106	B4	B0	U236	E5	C3
R108	B4	B0	U242A	G4	C4
R112	B3	B1	U312	E2	D1
R126	D5	B2	U402A	D1	E0
R128	D4	B2	U412	D1	E2
R130	E5	B2	U422	C1	E2

P/O A62 ASSY ALSO SHOWN ON ◇23 , ◇25

P/O A68 ASSY				R TRIGGER ◇24	
J100	H4	B0	——	——	——

A68 ASSY SHOWN IN FIG. 8-31

A B C D E F G H

1 2 3 4 5 6

C436 0.1 +15V
R DAC 0
R DAC 1
R DAC 2
R DAC 3
R DAC 4
R DAC 5
R DAC 6
R DAC 7
LSB
MSB
R421 7.50K +15V
R424 7.5K
C422 150
-15V
U422 N5009
C376 .001
R318 3.24K
+15V R338 15.0K
U412 741C
R412 2.7K
U402A CD4053
-5V CR402 CR404 +5V
R1T
R304 100.0K
R308 33.2K
C305 27
R305 10.0K
U312 LM318
R314 3.01K
R219 5.1K
R NORM OFFSET
R306 25k
R307 100K
C012 220
R004 15.0K
U002 LM318
P107 -R INT TRIG IN
P104 +R INT TRIG IN
T104
R006 10.0K
R008 49.9
R112 53.6
R102 10.0K
C016 250
R014 15.0K
CR012 CR013 CR014
U022A CD4053
C021 0.47
R028 5.1K
U022B CD4053
R218 10.0K
RAC
R026 5.1K
+5.1V
CR113 CR112
E120 C122 .0033 E122
C217 2.7pF
R217 20K
U204 LM318
P202 FROM J5109
R EXT TRIG IN
R201 100
L108 66nH
E201 C201 4.3
R108 51
R106 20K
CR114 CR116
C114 180
U022C CD4053
R074 2.4K
R022 3.6K
R214 100K
R204 25K
OFFSET
R211 R212 R213 ALL 100Ω
R210 220
C116 745
R215 100
R216 3.01K
C222 20
CR128 CR124 CR122 CR126
C126 10
R126 1.5K
R178 1.6K
R222 15K
INPUTS
AGC IN
R316 6.8K
R226 6.8K
I AGC
C224 0.1
L372 100nH
51
C322 1µF
PP LEVEL CONT
NORM LEVEL CONT
R326 150
R324 1.5K
L334 100nH
C332 1µF
SUBSTRATE
C226 0.1
R322 402
R SLOPE BALANCE
R302 10K
C234 0.47
HF REJ
C228 678
RHFR CR132
R130 1.2K
R132 3.9K
R134 1.5K
Q128
E128
U226 M1218
R334 24.9
R337 24.9
R328 68
C329 0.47
R336 24.9
R332 24.9
OFFSET
SLOPE
R + SLOPE
GATE
END SWP
HOLDOFF
FREE RUN
U236 M120
R236 2.7K
C238 82
R339 220
Q232 Q234
R136 523
R234 1K
R138 47
R135 51
R238 750
R131 1K
R242 10K
C244 39µF
CR242
U242A 74123
TRIG'D
R342 2.7K
R344 1K
R141 1K
C132 62
Q042
R140 1K
Q144
Q344
R147 470
R GATE
R TRIG'D
J100
A30
B27
P/O MAIN INTERCON

P/O TRIGGER BD. **A62**

2387-839

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23,A2,R1234
Assembly Number · Subassembly Number (if used) · Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TRIGGER A62

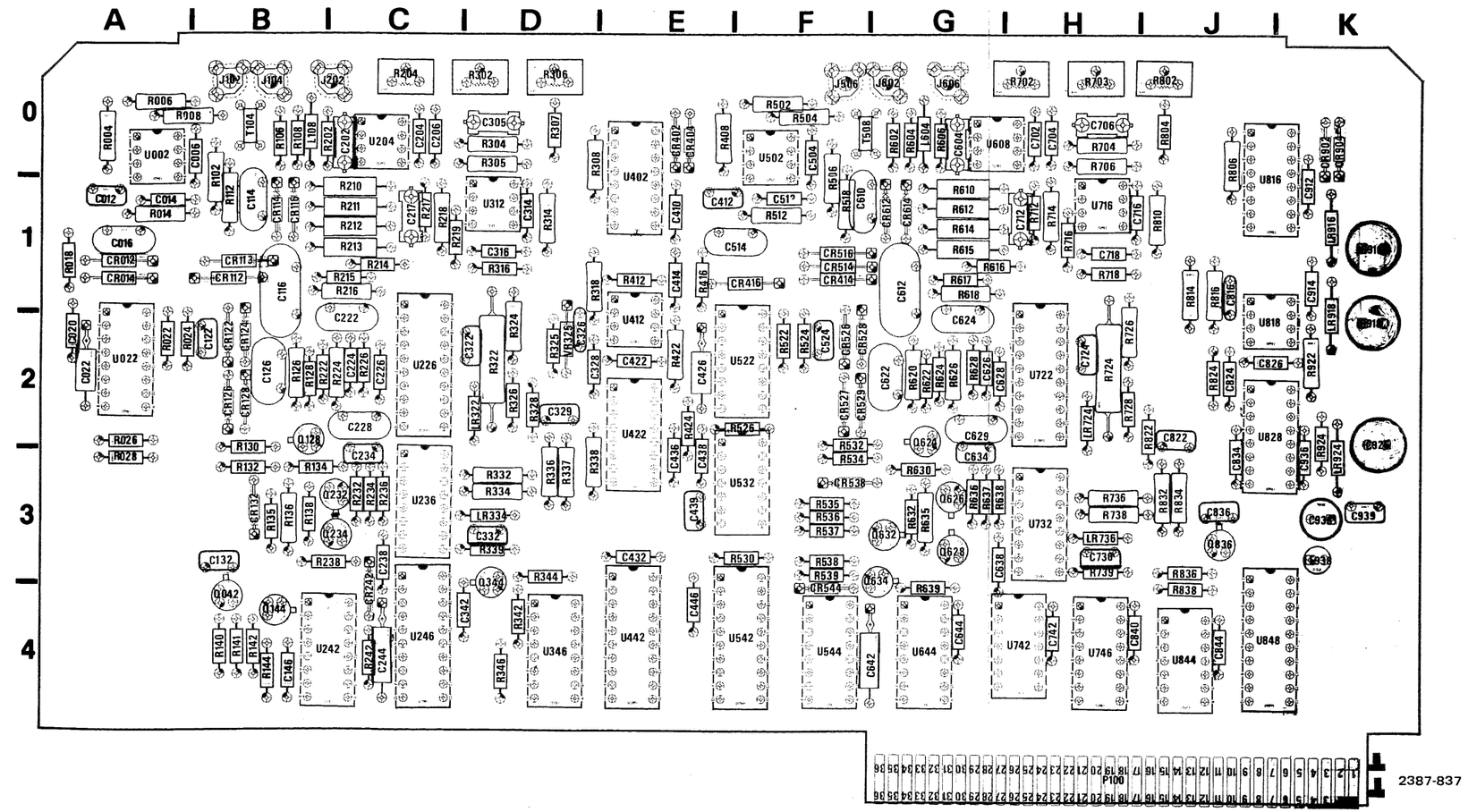
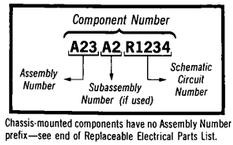


Fig. 8-26. Trigger circuit board, assembly A62.

P/O A62 ASSY			TRIG
Circuit Number	Schematic Location	Board Location	Circuit Number
C006	E5	A0	C916
C014	F6	A1	C918
C020	E6	A2	C926
C146	E5	B4	C938
C204	F6	C0	C939
C206	E5	C0	F938
C314	F5	D1	L916
C316	G6	D1	L918
C328	G6	D2	L924
C342	E5	D4	R144
C410	E6	E1	R325
C414	F5	E1	R346
C432	F5	E3	U246
C438	E6	E3	U346B
C439	G4	E3	U442
C446	F5	E4	U532C
C504	F5	F0	U542
C512	F6	F1	U644
C644	F5	G4	U742A
C702	F6	H0	U742B
C704	F5	H0	U742C
C716	G5	H1	U742D
C718	G6	H1	U742E
C742	F5	H4	U742F
C824	G6	J2	U844B
C834	G6	J3	U844C
C840	G5	J4	U844E
C844	G5	J4	U844F
C912	E6	K1	U848
C914	G5	K1	VR325
P/O A62 ASSY ALSO SHOWN ON 23			

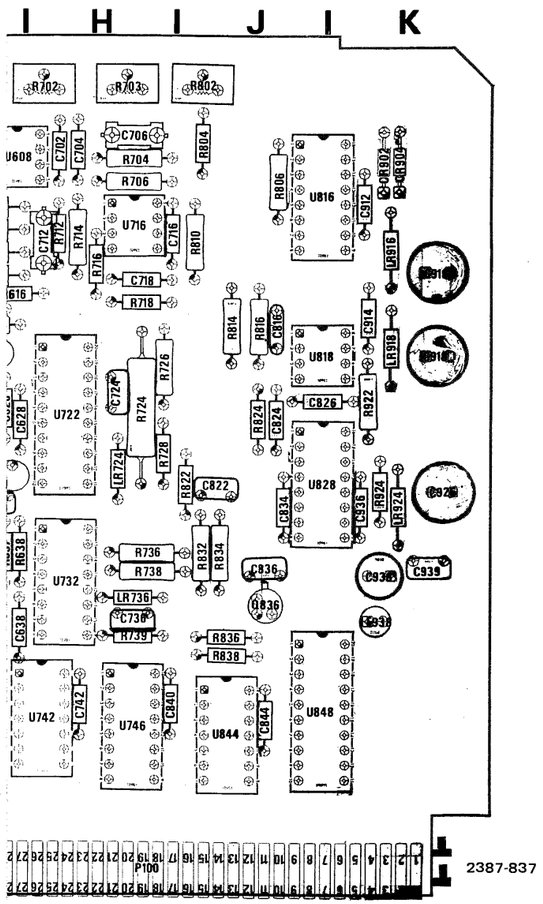
P/O A68 ASSY			TRIG
J100	A1	B0	J100
A68 ASSY SHOWN IN FIG. 8			

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

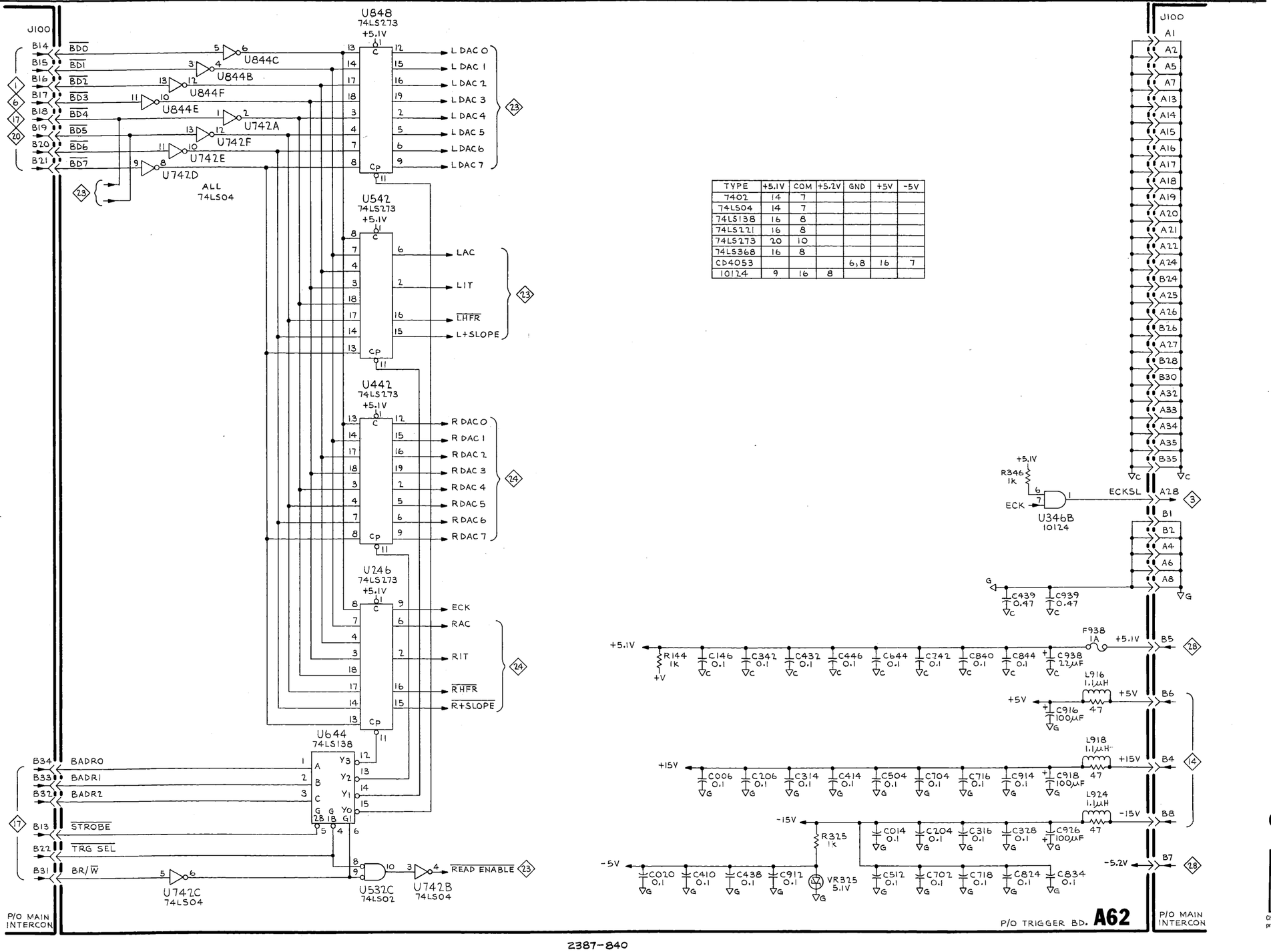


P/O A62 ASSY			TRIGGER CONTROL 25		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C006	E5	A0	C916	G5	K1
C014	F6	A1	C918	G5	K2
C020	E6	A2	C926	G6	K2
C146	E5	B4	C938	G5	K3
C204	F6	C0	C939	G4	K3
C206	E5	C0	F938	G4	K3
C314	F5	D1	L916	G5	K1
C316	G6	D1	L918	G5	K1
C328	G6	D2	L924	G5	K2
C342	E5	D4	R144	E5	B4
C410	E6	E1	R325	F6	D2
C414	F5	E1	R346	G3	D4
C432	F5	E3	U246	C4	C4
C438	E6	E3	U346B	G4	D4
C439	G4	E3	U442	C3	E4
C446	F5	E4	U532C	C6	F3
C504	F5	F0	U542	C2	F4
C512	F6	F1	U644	C5	G4
C644	F5	G4	U742A	B1	H4
C702	F6	H0	U742B	C6	H4
C704	F5	H0	U742C	B6	H4
C716	G5	H1	U742D	B2	H4
C718	G6	H1	U742E	B1	H4
C742	F5	H4	U742F	B1	H4
C824	G6	J2	U844B	B1	J4
C834	G6	J3	U844C	B1	J4
C840	G5	J4	U844E	B1	J4
C844	G5	J4	U844F	B1	J4
C912	E6	K1	U848	C1	K4
C914	G5	K1	VR325	F6	D2

P/O A62 ASSY ALSO SHOWN ON 23 , 24

P/O A68 ASSY			TRIGGER CONTROL 25		
J100	A1	B0	J100	H1	B0

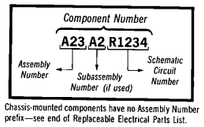
A68 ASSY SHOWN IN FIG. 8-31



TYPE	+5.1V	COM	+5.2V	GND	+5V	-5V
7402	14	7				
74LS04	14	7				
74LS138	16	8				
74LS221	16	8				
74LS273	20	10				
74LS368	16	8				
CD4053				6,8	16	7
10124	9	16	8			

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

2387-840

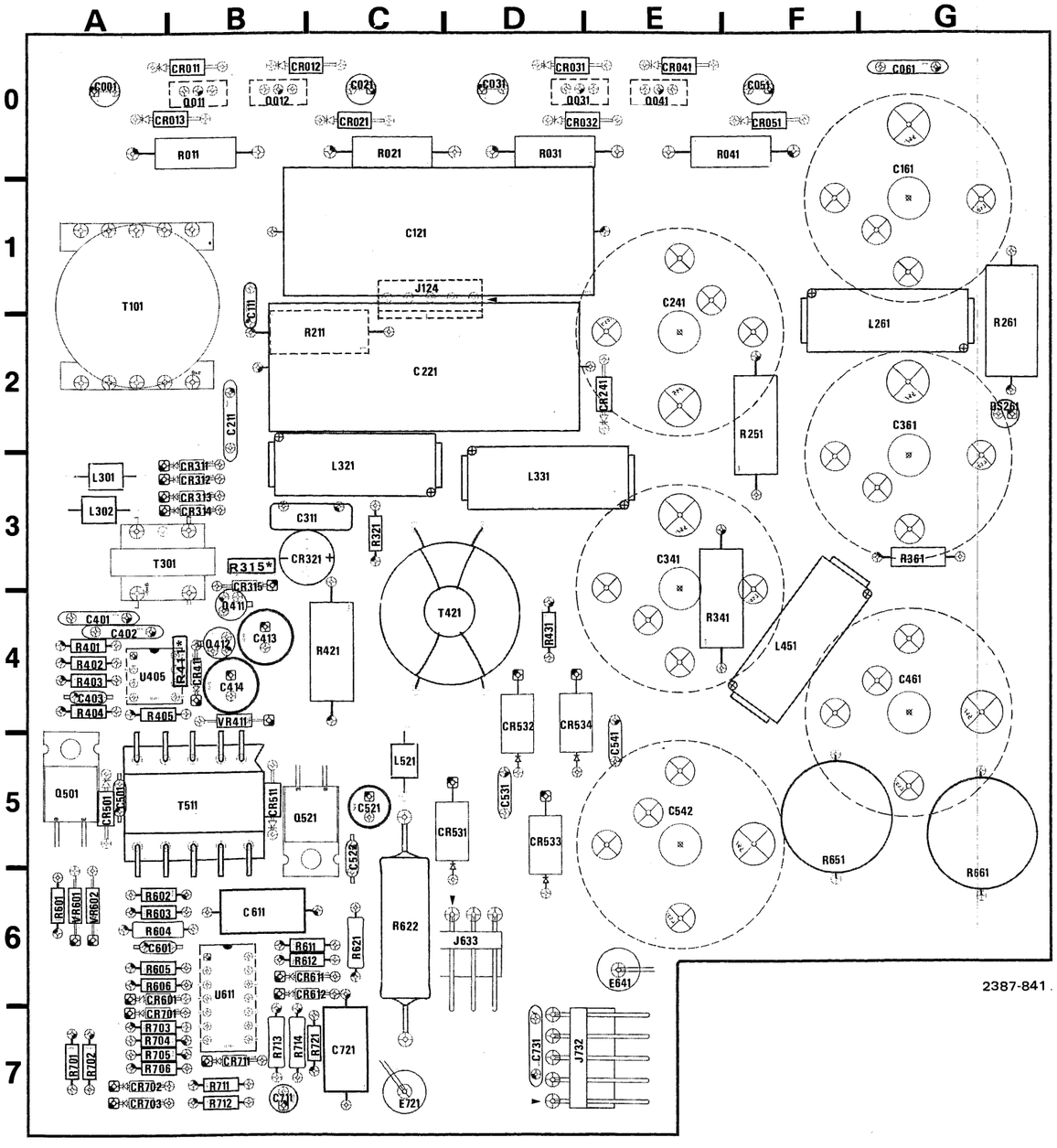
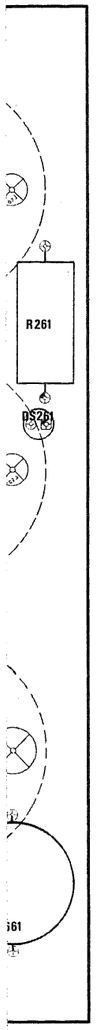


Fig. 8-27. Line circuit board, assembly A80.

A80 ASSY			LINE INPUT/FAN 26		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
B5020	H2	CHASSIS	L302	E5	A3
C001	G3	A0	L321	F3	C3
C021	G4	C0	L331	F3	D3
C031	G4	D0	L451	E3	F4
C051	G5	F0	L521	F6	C5
C061	D3	G0	P124	H5	C1
C111	G6	B1	P633	H2	D6
C121	F3	C1	P732	A3	D7
C161	E3	G1	Q012	H4	B0
C211	G5	B2	Q031	G4	D0
C221	G6	C2	Q041	G5	E0
C241	E3	E1	Q411	D5	B4
C261	D3	G2	Q412	D5	B4
C311	F5	B3	Q412	D5	B4
C341	E3	E3	Q501	E2	A5
C361	D3	G2	Q521	D2	B5
C401	D5	A4	R011	G4	B0
C402	D5	A4	R021	G4	C0
C403	D5	A4	R031	G4	D0
C413	E5	B4	R041	G5	E0
C414	E5	B4	R211	G6	C2
C461	D3	G4	R251	E3	F2
C501	E2	A5	R315*	D5	B4
C521	F6	C5	R321	F6	C3
C522	D2	C5	R341	E3	E4
C531	B3	D5	R361	D3	G3
C541	B3	E5	R401	D5	A4
C542	E3	E5	R402	D5	A4
C601	C2	A6	R403	D5	A4
C611	C3	B6	R404	C5	A4
C711	G6	B7	R405	C5	A4
C721	B2	C7	R405	E3	G2
C731	C3	D7	R411*	D5	B4
CR011	H3	B0	R421	C5	C4
CR012	H4	B0	R431	F3	D4
CR013	G4	A0	R601	G6	A6
CR021	G4	C0	R602	C2	A6
CR031	H4	D0	R603	D2	A6
CR032	G4	D0	R604	C3	A6
CR041	G5	E0	R605	D2	A6
CR051	G5	F0	R606	C2	A6
CR241	F6	E2	R611	E1	B6
CR311	E5	B3	R612	D2	B6
CR312	E5	B3	R621	B2	C6
CR313	E5	B3	R622	F6	C6
CR314	E5	B3	R651	C3	F5
CR315*	D5	B4	R661	C3	G5
CR321	C5	B4	R701	C2	A7
CR411*	D5	B4	R702	C2	A7
CR501	F2	A5	R703	D2	A7
CR511	F2	B5	R704	D2	A7
CR531	C3	D5	R705	C2	A7
CR532	C3	D5	R706	D2	A7
CR533	C3	D5	R711	E1	B7
CR534	C3	D5	R712	D2	B7
CR601	C2	A6	R713	B2	B7
CR611	B2	B6	R714	B2	B7
CR612	B2	B6	R721	B2	B7
CR701	C2	A7	S5021	A3	CHASSIS
CR702	D2	A7	S5022	A2	CHASSIS
CR703	D2	A7	T101	F4	A1
CR711	C2	B7	T301	E5	A3
DS261	D3	G2	T421	F3	D4
E641	B3	E6	T511	D2	B5
E721	B3	C7	T5020	A2	CHASSIS
F5020	A2	CHASSIS	U405	D5	A4
FL5020	A1	CHASSIS	U611A	C2	B6
J020	F4	D7	U611B	D2	B6
J020	F5	D7	U611C	B2	B6
L261	E3	G2	U611D	D2	B6
L301	E5	A3	VR411	C5	B4
			VR601	G6	A6
			VR602	G6	A6

*See Parts List for serial number ranges.



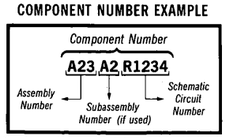
A80 ASSY — **LINE INPUT/FAN** (26)

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
B5020	H2	CHASSIS	L302	E5	A3
C001	G3	A0	L321	F3	C3
C021	G4	C0	L331	F3	D3
C031	G4	D0	L451	E3	F4
C051	G5	F0	L521	F6	C5
C061	D3	G0	P124	H5	C1
C111	G6	B1	P633	H2	D6
C121	F3	C1	P732	A3	D7
C161	E3	G1	Q012	H4	B0
C211	G5	B2	Q031	G4	D0
C221	G6	C2	Q041	G5	E0
C241	E3	E1	Q411	D5	B4
C261	D3	G2	Q412	D5	B4
C311	F5	B3	Q412	D5	B4
C341	E3	E3	Q501	E2	A5
C361	D3	G2	Q521	D2	B5
C401	D5	A4	R011	G4	B0
C402	D5	A4	R021	G4	C0
C403	D5	A4	R031	G4	D0
C413	E5	B4	R041	G5	E0
C414	E5	B4	R211	G6	C2
C461	D3	G4	R251	E3	F2
C501	E2	A5	R315*	D5	B4
C521	F6	C5	R321	F6	C3
C522	D2	C5	R341	E3	E4
C531	B3	D5	R361	D3	G3
C541	B3	E5	R401	D5	A4
C542	E3	E5	R402	D5	A4
C601	C2	A6	R403	D5	A4
C611	C3	B6	R404	C5	A4
C711	G6	B7	R405	C5	A4
C721	B2	C7	R405	E3	G2
C731	C3	D7	R411*	D5	B4
CR011	H3	B0	R421	C5	C4
CR012	H4	B0	R431	F3	D4
CR013	G4	A0	R601	G6	A6
CR021	G4	C0	R602	C2	A6
CR031	H4	D0	R603	D2	A6
CR032	G4	D0	R604	C3	A6
CR041	G5	E0	R605	D2	A6
CR051	G5	F0	R606	C2	A6
CR241	F6	E2	R611	E1	B6
CR311	E5	B3	R612	D2	B6
CR312	E5	B3	R621	B2	C6
CR313	E5	B3	R622	F6	C6
CR314	E5	B3	R651	C3	F5
CR315*	D5	B4	R661	C3	G5
CR321	C5	B4	R701	C2	A7
CR411*	D5	B4	R702	C2	A7
CR501	F2	A5	R703	D2	A7
CR511	F2	B5	R704	D2	A7
CR531	C3	D5	R705	C2	A7
CR532	C3	D5	R706	D2	A7
CR533	C3	D5	R711	E1	B7
CR534	C3	D5	R712	D2	B7
CR601	C2	A6	R713	B2	B7
CR611	B2	B6	R714	B2	B7
CR612	B2	B6	R721	B2	B7
CR701	C2	A7	S5021	A3	CHASSIS
CR702	D2	A7	S5022	A2	CHASSIS
CR703	D2	A7	T101	F4	A1
CR711	C2	B7	T301	E5	A3
DS261	D3	G2	T421	F3	D4
E641	B3	E6	T511	D2	B5
E721	B3	C7	T5020	A2	CHASSIS
F5020	A2	CHASSIS	U405	D5	A4
FL5020	A1	CHASSIS	U611A	C2	B6
J020	F4	D7	U611B	D2	B6
J020	F5	D7	U611C	B2	B6
L261	E3	G2	U611D	D2	B6
L301	E5	A3	VR411	C5	B4
			VR601	G6	A6
			VR602	G6	A6

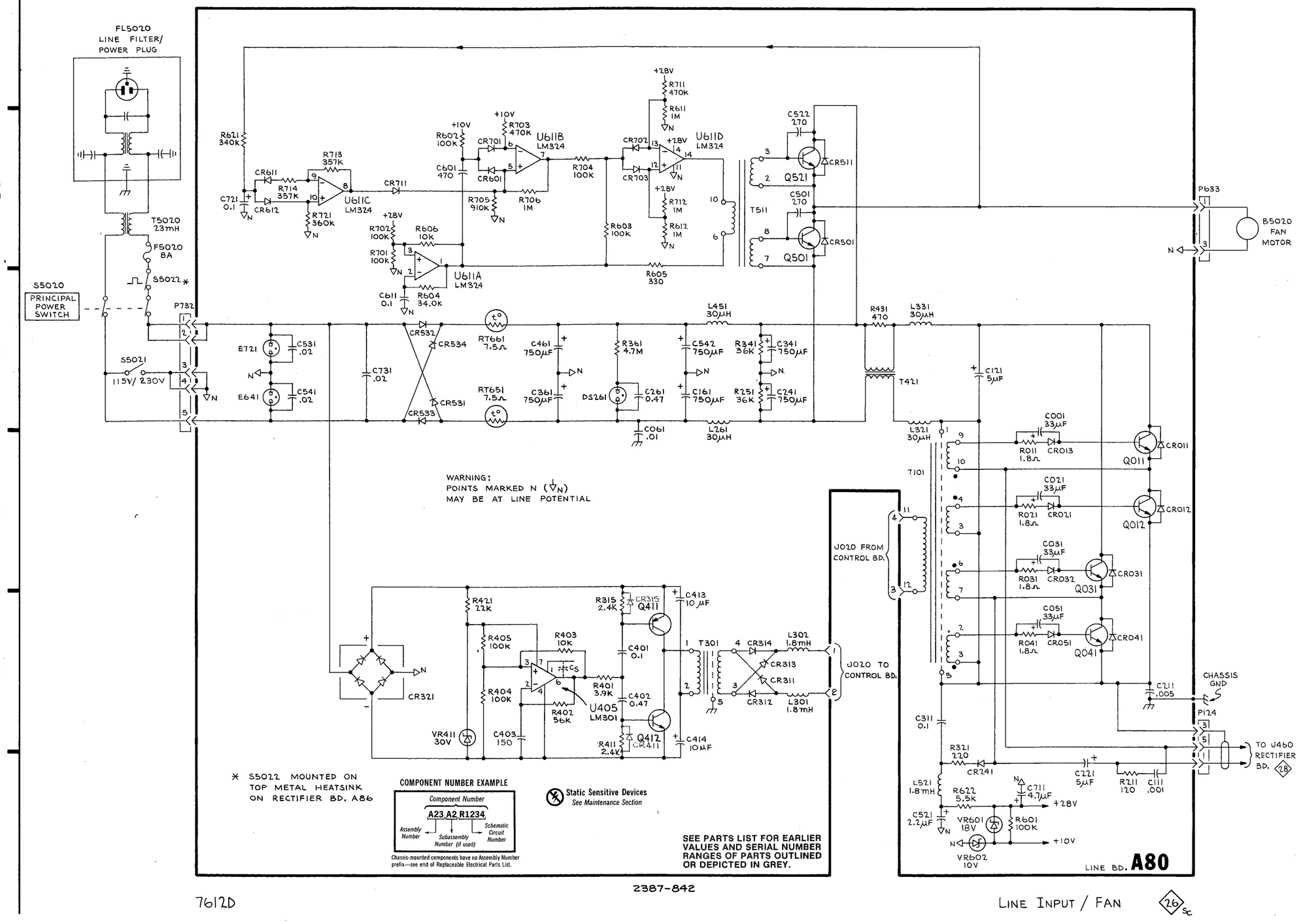
***See Parts List for serial number ranges.**

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



2387-842

7612D

LINE INPUT / FAN 26 Sc

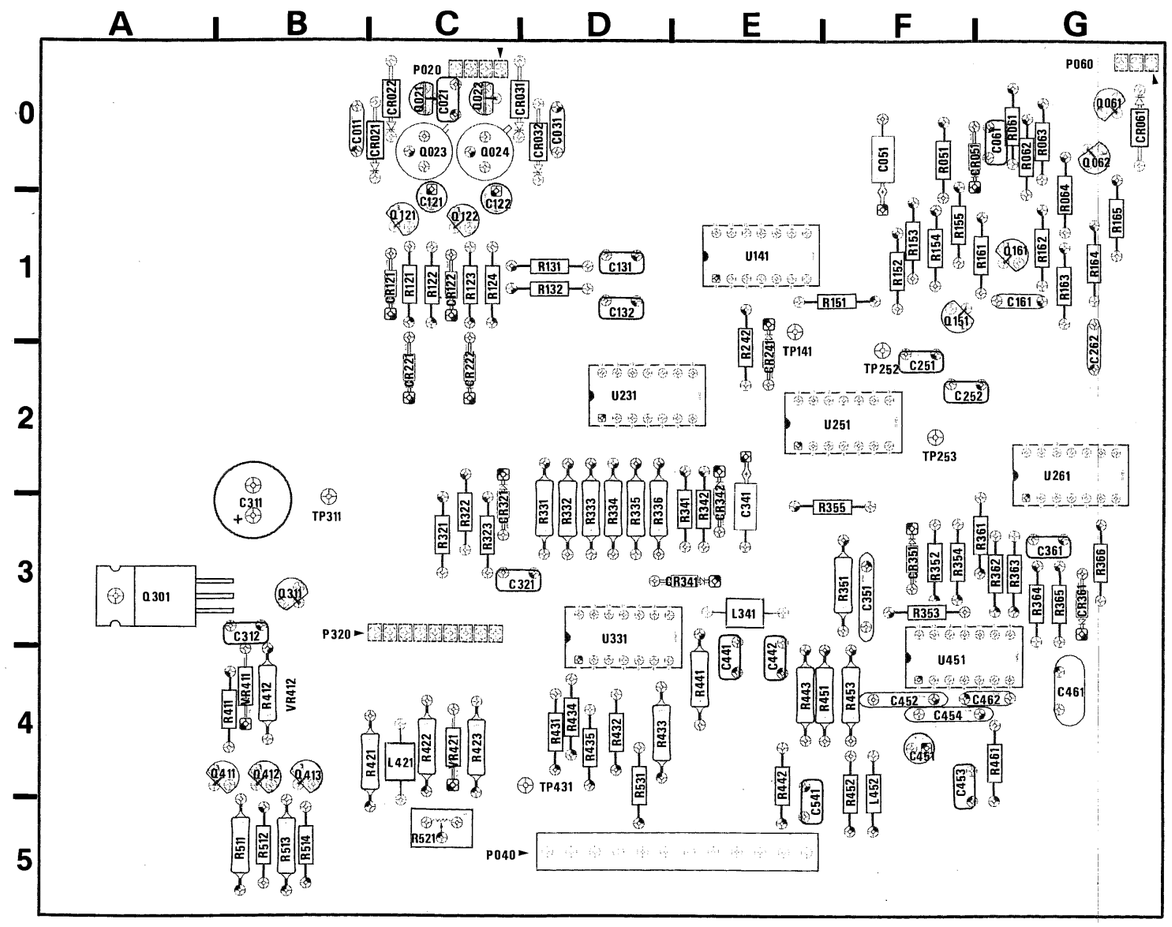


Fig. 8-28. Control circuit board, assembly A82.

CONTROL A82

A82 ASSY

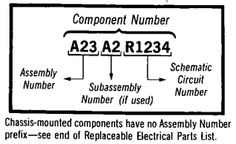
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circ Num
C011	H2	B0	P320	H5	C4	R36
C021	H2	C0	Q021	H2	C0	R36
C031	H2	D0	Q022	H3	C0	R36
C051	F1	H0	Q023	H1	C0	R36
C061	B3	F0	Q024	H2	C0	R4
C121	G1	C1	Q061	E3	G0	R4
C122	G2	C1	Q062	D3	G1	R4
C131	G2	D1	Q121	H1	C1	R4
C132	G1	D1	Q122	H2	C1	R4
C161	C2	G1	Q151	B2	H1	R4
C221	G2	C2	Q161	C3	G1	R4
C251	C2	H2	Q301	C5	A3	R4
C252	C5	F2	Q311	C5	B3	R4
C262	C2	G2	Q411	B5	B4	R4
C311	C5	B3	Q412	B5	B4	R4
C312	C5	B3	Q413	B5	B5	R4
C321	B2	D3	R051	B3	F0	R4
C341	C4	E3	R061	A3	G0	R4
C351	F4	F3	R062	B3	G0	R4
C361	D3	G3	R063	A3	G0	R4
C441	D3	E4	R064	D2	G1	R4
C442	F2	E4	R121	G2	C1	R5
C451	F4	F4	R122	G2	C1	R5
C452	F3	F4	R123	H3	C1	R5
C453	F4	F4	R124	G2	C1	R5
C454	F3	G4	R131	G2	D1	R5
C461	E1	G4	R132	G1	D1	R5
C462	F3	G4	R151	C2	H1	TP
C541	F4	E5	R152	F1	H1	TP
CR021	H1	C0	R153	C3	F1	TP
CR022	H2	C0	R154	B3	F1	TP
CR031	H3	D0	R155	B3	F1	TP
CR032	H2	D0	R161	B2	H1	U1
CR051	B3	F0	R162	C2	G1	U1
CR061	E2	G0	R163	D2	G1	U2
CR121	G1	C1	R164	C2	G1	U2
CR122	G2	C1	R165	D2	G1	U2
CR222	G3	C2	R242	C3	E2	U2
CR241	C3	E2	R321	A2	C3	U2
CR321	B2	C3	R322	B2	C3	U2
CR341	D4	E3	R323	A2	C3	U2
CR342	F3	E3	R331	E5	D3	U2
CR351	E1	H3	R332	D5	D3	U2
CR361	E1	G3	R333	E4	D3	U2
J5118	E2	CHASSIS	R334	D4	D4	U3
J5119	A3	CHASSIS	R335	D3	D3	U3
L341	D3	E3	R336	D3	D3	U3
L421	G5	C4	R341	F3	E3	U3
L452	F4	F5	R342	F3	E3	U4
P020	H2	C0	R351	F4	F3	U4
P040	E3	D5	R352	E1	F3	U4
P040	F5	D5	R353	E1	H3	U4
P060	A3	G0	R354	E1	H3	VR
P060	E2	G0	R355	F2	F3	VR
P320	A2	C3	R361	E1	H3	VR
P320	E5	C3	R362	D2	G3	

P/O A68 ASSY

P500	A2	G0	P500	H6	G0	P50

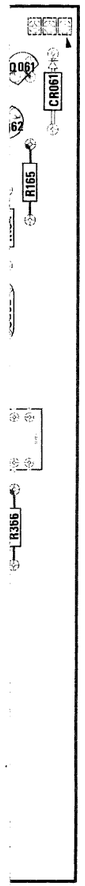
A68 ASSY SHOWN IN FIG. 8-31

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



2387-843

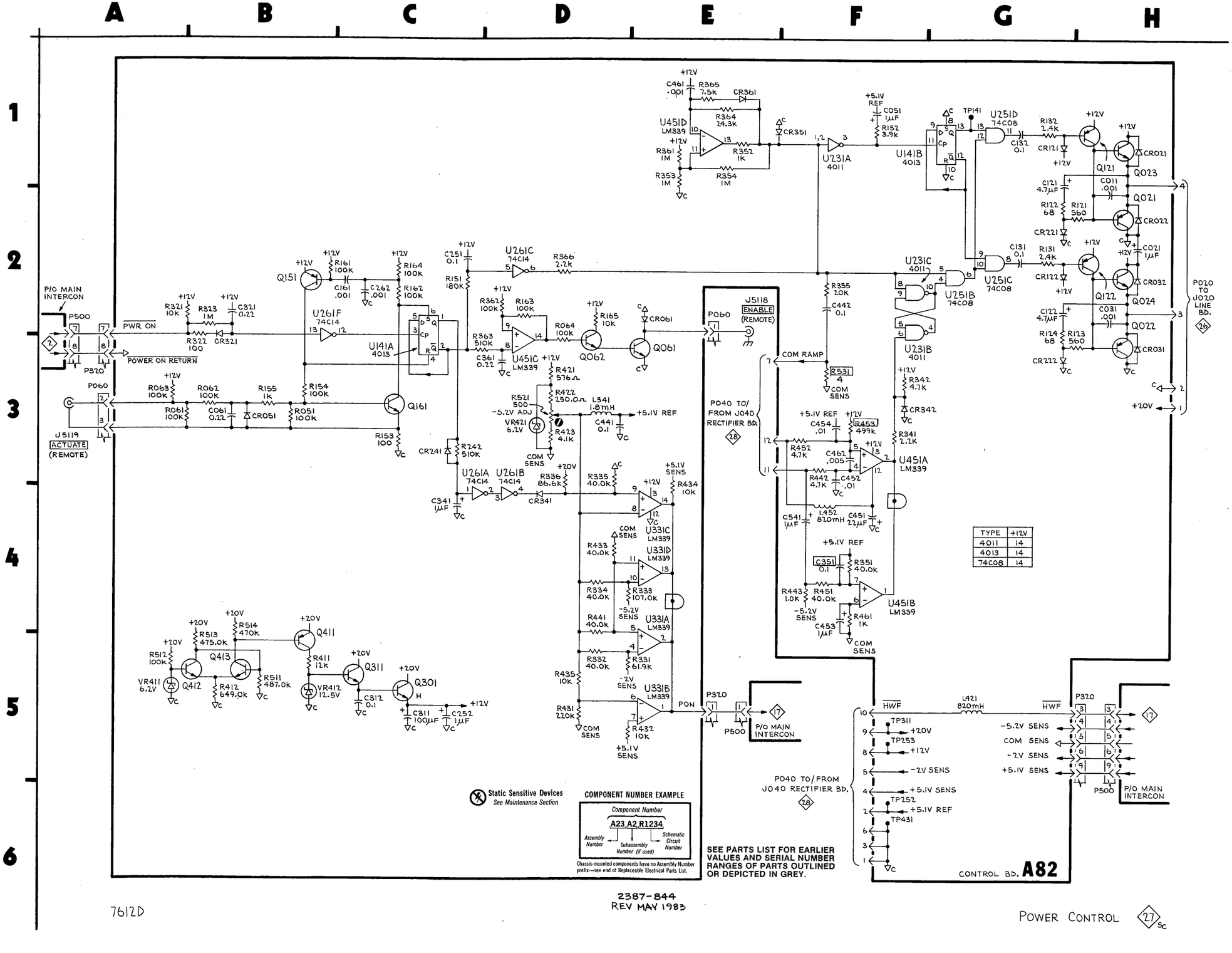
A82 ASSY — **POWER CONTROL** 27

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C011	H2	B0	P320	H5	C4	R363	D3	G3
C021	H2	C0	Q021	H2	C0	R364	E1	G3
C031	H2	D0	Q022	H3	C0	R365	E1	G3
C051	F1	H0	Q023	H1	C0	R366	D2	G3
C061	B3	F0	Q024	H2	C0	R411	B5	B4
C121	G1	C1	Q061	E3	G0	R412	B5	B4
C122	G2	C1	Q062	D3	G1	R421	D3	C4
C131	G2	D1	Q121	H1	C1	R422	D3	C4
C132	G1	D1	Q122	H2	C1	R423	D3	C4
C161	C2	G1	Q151	B2	H1	R431	D5	D4
C221	G2	C2	Q161	C3	G1	R432	E5	D4
C251	C2	H2	Q301	C5	A3	R433	D4	D4
C252	C5	F2	Q311	C5	B3	R434	E4	D4
C262	C2	G2	Q411	B5	B4	R435	D5	D4
C311	C5	B3	Q412	B5	B4	R441	D4	E4
C312	C5	B3	Q413	B5	B5	R442	F3	E4
C321	B2	D3	R051	B3	F0	R443	F4	E4
C341	C4	E3	R061	A3	G0	R451	F4	E4
C351	F4	F3	R062	B3	G0	R452	F3	F4
C361	D3	G3	R063	A3	G0	R453	F3	F4
C441	D3	E4	R064	D2	G1	R461	F4	G4
C442	F2	E4	R121	G2	C1	R511	B5	B5
C451	F4	F4	R122	G2	C1	R512	A5	B5
C452	F3	F4	R123	H3	C1	R513	B5	B5
C453	F4	F4	R124	G2	C1	R514	B5	B5
C454	F3	G4	R131	G2	D1	R521	D3	C5
C461	E1	G4	R132	G1	D1	R531	F3	D4
C462	F3	G4	R151	C2	H1	TP141	G1	E1
C541	F4	E5	R152	F1	H1	TP252	F6	F2
CR021	H1	C0	R153	C3	F1	TP253	F5	F2
CR022	H2	C0	R154	B3	F1	TP311	F5	B3
CR031	H3	D0	R155	B3	F1	TP431	F6	D4
CR032	H2	D0	R161	B2	H1	U141A	C3	E1
CR051	B3	F0	R162	C2	G1	U141B	G1	E1
CR061	E2	G0	R163	D2	G1	U231A	F1	D2
CR121	G1	C1	R164	C2	G1	U231B	F2	D2
CR122	G2	C1	R165	D2	G1	U231C	F2	D2
CR222	G3	C2	R242	C3	E2	U251B	G2	F2
CR241	C3	E2	R321	A2	C3	U251C	G2	F2
CR321	B2	C3	R322	B2	C3	U251D	G1	H2
CR341	D4	E3	R323	A2	C3	U261A	D4	G2
CR342	F3	E3	R331	E5	D3	U261B	D4	G2
CR351	E1	H3	R332	D5	D3	U261C	D2	G2
CR361	E1	G3	R333	E4	D3	U261F	B2	G2
J5118	E2	CHASSIS	R334	D4	D4	U331	D4	D3
J5119	A3	CHASSIS	R335	D3	D3	U331A	E4	D3
L341	D3	E3	R336	D3	D3	U331B	E5	D3
L421	G5	C4	R341	F3	E3	U331D	E4	D3
L452	F4	F5	R342	F3	E3	U451A	F3	F4
P020	H2	C0	R351	F4	F3	U451B	F4	F4
P040	E3	D5	R352	E1	F3	U451C	D2	F4
P040	F5	D5	R353	E1	H3	U451D	E1	F4
P060	A3	G0	R354	E1	H3	VR411	A5	B4
P060	E2	G0	R355	F2	F3	VR412	B5	B4
P320	A2	C3	R361	E1	H3	VR421	D3	C4
P320	E5	C3	R362	D2	G3			

P/O A68 ASSY — **POWER CONTROL** 27

P500	A2	G0	P500	H6	G0	P500	E5	G0

A68 ASSY SHOWN IN FIG. 8-31



TYPE	+12V
4011	14
4013	14
74C08	14

2387-844
REV MAY 1983

7612D

POWER CONTROL 27 Sc

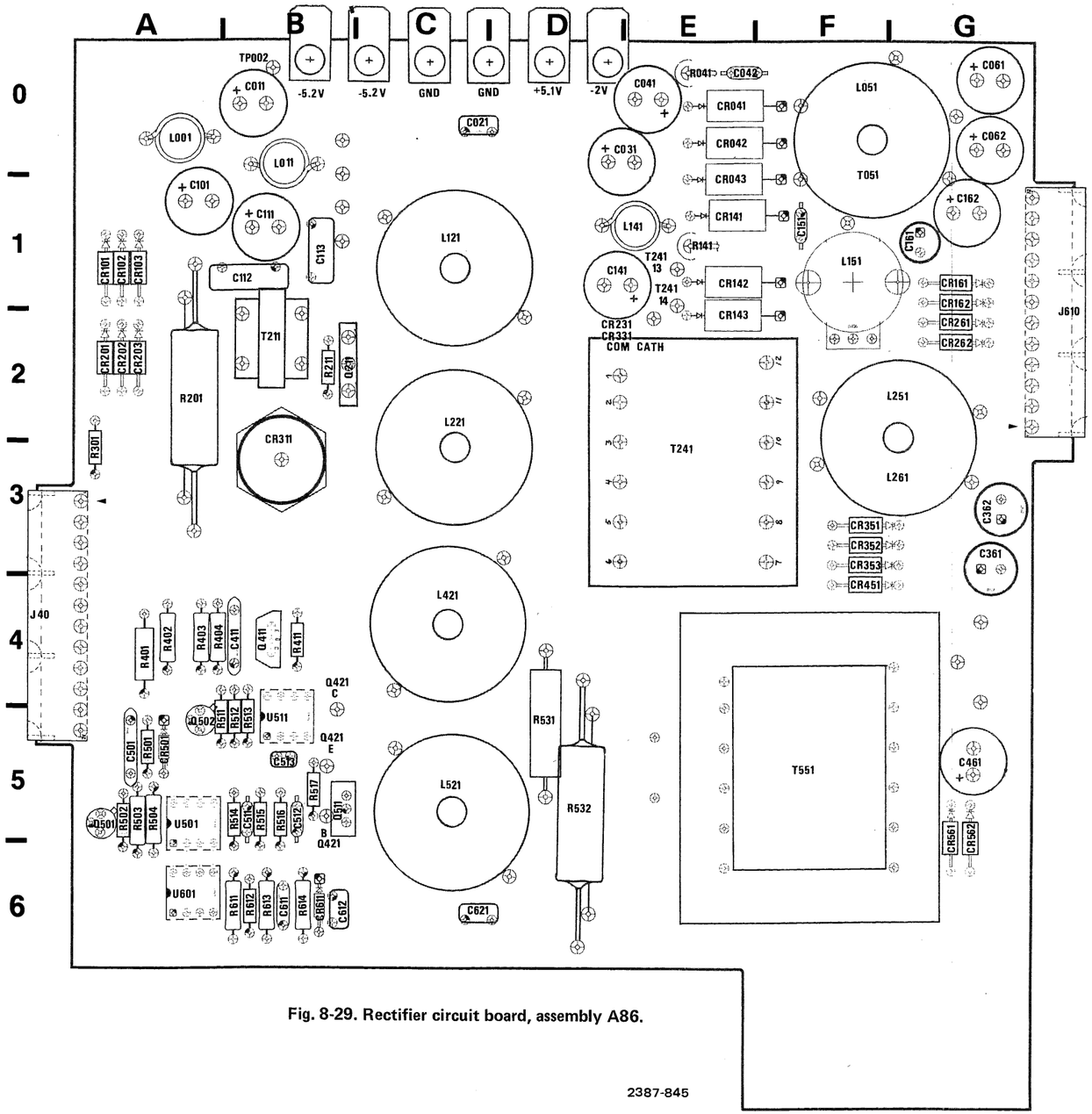
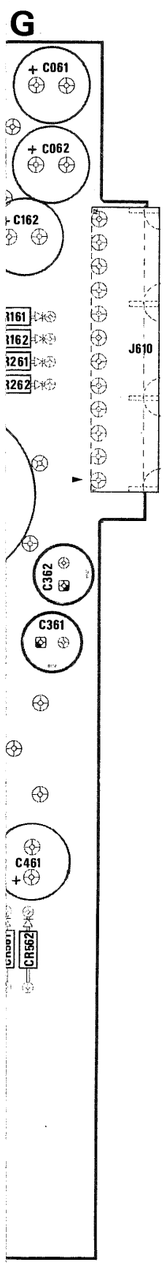


Fig. 8-29. Rectifier circuit board, assembly A86.

2387-845

A86 ASSY			INVERTER RECTIFIER 28		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C011	B2	B0	J040	A4	A4
C021	H5	C0	J040	A5	A4
C031	B6	D0	J040	C1	A4
C041	B3	E0	J040	H4	A4
C042	G3	E0	L001	B6	A0
C061	H3	G0	L011	B2	B0
C062	H4	G1	L051	G3	F0
C101	B6	A1	L121	C2	C1
C111	B2	B1	L141	B3	E1
C112	C6	B1	L151	G1	F1
C113	C2	B1	L221	C2	C2
C141	B3	D1	L251	G2	G3
C151	G3	F1	L261	G2	G3
C161	H2	G1	L421	C6	C4
C162	H3	G1	L521	C3	C5
C361	H2	G3	Q211	E6	HEAT SINK
C362	H2	G3	Q411	E5	B4
C411	C2	B4	Q421	E3	HEAT SINK
C461	F4	G5	Q501	D5	A5
C501	D4	A5	Q502	D3	A5
C511	C5	B5	Q511	E2	HEAT SINK
C512	C3	B5	R041	G3	E0
C513	D3	B5	R111	C2	HEAT SINK
C533	E2	HEAT SINK	R201	C6	A2
C534	E2	HEAT SINK	R211	E5	B2
C611	C5	B6	R301	B3	A3
C612	D2	B6	R401	D5	A4
C621	H5	D6	R402	B3	A4
CR041	G3	E0	R403	C3	A4
CR042	G3	E0	R404	C2	A4
CR043	G3	E1	R411	E5	B4
CR101	E4	A1	R501	D4	A5
CR102	E4	A1	R502	C5	A5
CR103	E4	A1	R503	C5	A5
CR141	G3	E1	R504	C5	A5
CR142	G3	E1	R511	D3	B5
CR143	G3	E2	R512	D3	B5
CR161	G1	G1	R513	D2	B5
CR162	G2	G2	R514	D5	B5
CR201	E4	A2	R515	B5	B5
CR202	E4	A2	R516	B5	B5
CR203	E4	A2	R517	E3	B5
CR231	E2	E2	R531	E2	D5
CR261	G2	G2	R532	C3	D5
CR262	G2	G2	R533	E2	HEAT SINK
CR311	E5	HEAT SINK	R534	E2	HEAT SINK
CR321	D3	HEAT SINK	R611	C3	B6
CR331	E3	E2	R612	C3	B6
CR351	G2	F3	R613	C3	B6
CR352	G2	F3	R614	D2	B6
CR353	G2	F3	T051	G3	F0
CR451	G2	F4	T211	E4	B2
CR501	D3	A5	T241	F2	E3
CR531	E2	HEAT SINK	T551	E2	F5
CR561	F3	G5	U501	D5	A5
CR562	F2	G6	U511	D2	B5
CR611	D2	B6	U601B	C5	A6
CR631	E2	HEAT SINK	U610A	C3	A6
J040	A3	A4			

P/O A86 ASSY			INVERTER RECTIFIER 28		
C320	A6	D2	C420	A3	E2
A68 ASSY SHOWN IN FIG. 8-31					



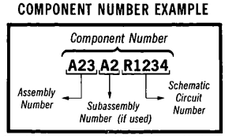
A86 ASSY			INVERTER RECTIFIER 28		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C011	B2	B0	J040	A4	A4
C021	H5	C0	J040	A5	A4
C031	B6	D0	J040	C1	A4
C041	B3	E0	J040	H4	A4
C042	G3	E0	L001	B6	A0
C061	H3	G0	L011	B2	B0
C062	H4	G1	L051	G3	F0
C101	B6	A1	L121	C2	C1
C111	B2	B1	L141	B3	E1
C112	C6	B1	L151	G1	F1
C113	C2	B1	L221	C2	C2
C141	B3	D1	L251	G2	G3
C151	G3	F1	L261	G2	G3
C161	H2	G1	L421	C6	C4
C162	H3	G1	L521	C3	C5
C361	H2	G3	Q211	E6	HEAT SINK
C362	H2	G3	Q411	E5	B4
C411	C2	B4	Q421	E3	HEAT SINK
C461	F4	G5	Q501	D5	A5
C501	D4	A5	Q502	D3	A5
C511	C5	B5	Q511	E2	HEAT SINK
C512	C3	B5	R041	G3	E0
C513	D3	B5	R111	C2	HEAT SINK
C533	E2	HEAT SINK	R201	C6	A2
C534	E2	HEAT SINK	R211	E5	B2
C611	C5	B6	R301	B3	A3
C612	D2	B6	R401	D5	A4
C621	H5	D6	R402	B3	A4
CR041	G3	E0	R403	C3	A4
CR042	G3	E0	R404	C2	A4
CR043	G3	E1	R411	E5	B4
CR101	E4	A1	R501	D4	A5
CR102	E4	A1	R502	C5	A5
CR103	E4	A1	R503	C5	A5
CR141	G3	E1	R504	C5	A5
CR142	G3	E1	R511	D3	B5
CR143	G3	E2	R512	D3	B5
CR161	G1	G1	R513	D2	B5
CR162	G2	G2	R514	D5	B5
CR201	E4	A2	R515	B5	B5
CR202	E4	A2	R516	B5	B5
CR203	E4	A2	R517	E3	B5
CR231	E2	E2	R531	E2	D5
CR261	G2	G2	R532	C3	D5
CR262	G2	G2	R533	E2	HEAT SINK
CR311	E5	HEAT SINK	R534	E2	HEAT SINK
CR321	D3	HEAT SINK	R611	C3	B6
CR331	E3	E2	R612	C3	B6
CR351	G2	F3	R613	C3	B6
CR352	G2	F3	R614	D2	B6
CR353	G2	F3	T051	G3	F0
CR451	G2	F4	T211	E4	B2
CR501	D3	A5	T241	F2	E3
CR531	E2	HEAT SINK	T551	E2	F5
CR561	F3	G5	U501	D5	A5
CR562	F2	G6	U511	D2	B5
CR611	D2	B6	U601B	C5	A6
CR631	E2	HEAT SINK	U610A	C3	A6
J040	A3	A4			

P/O A86 ASSY			INVERTER RECTIFIER 28		
C320	A6	D2	C420	A3	E2

A68 ASSY SHOWN IN FIG. 8-31

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A B C D E F G H

1 2 3 4 5 6

J040 TO P040 CONTROL BD. 27

FROM P124 LINE BD. 26

J040-5 FROM P040 CONTROL BD. 27

J040-7 FROM P040 CONTROL BD. 27

J040-4 FROM P040 CONTROL BD. 27

P/O MAIN INTERCON

J450 TO/FROM P450 REG. BD. 29

J040 FROM P040 CONTROL BD. 27

CHASSIS GND

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23,A2,R1234
Assembly Number · Subassembly Number (if used) · Schematic Circuit Number

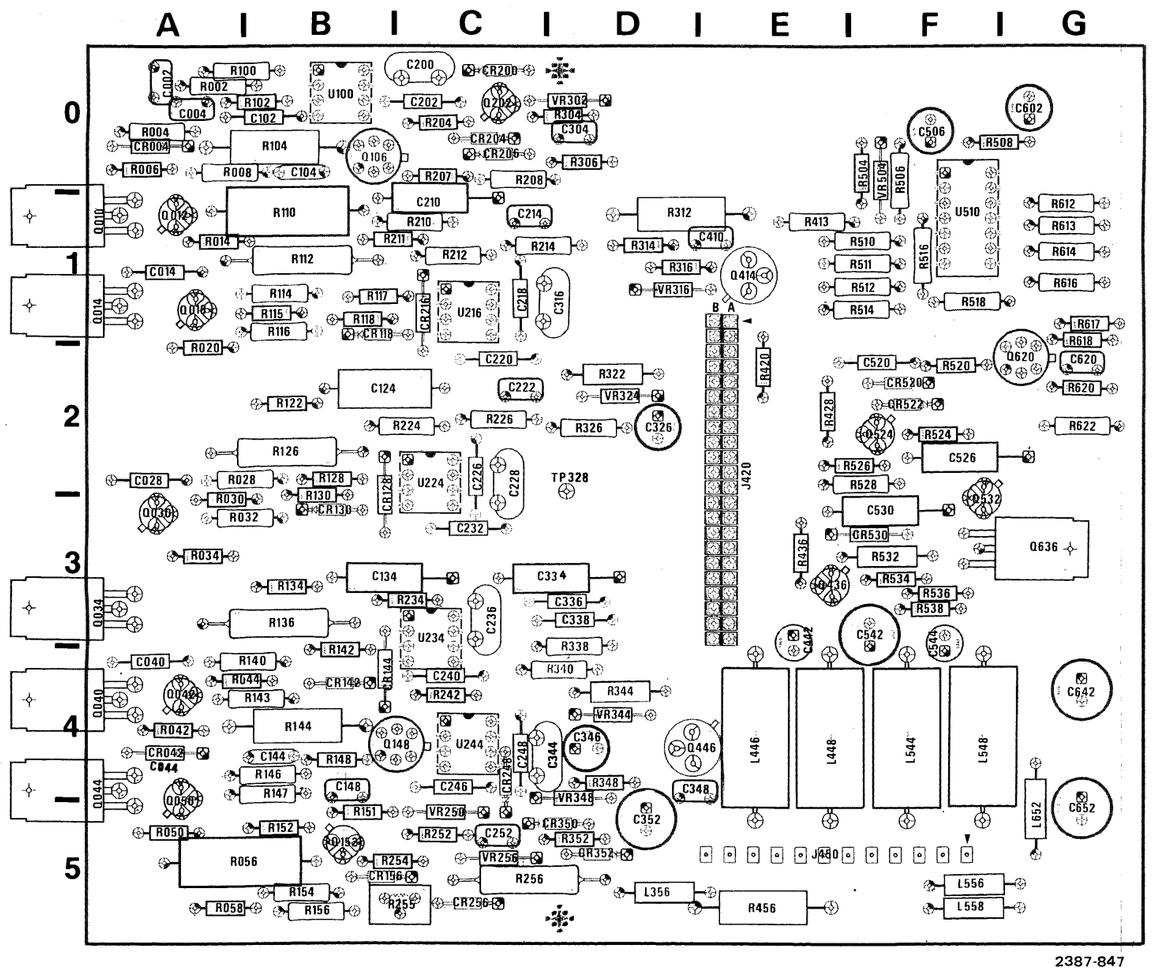
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

RECTIFIER BD. A86

2387-846
REV MAY 1983

76120

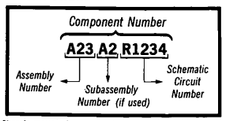
INVERTER RECTIFIER 28 Sc



2387-847

Fig. 8-30. Regulator circuit board, assembly A88.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A88 ASSY

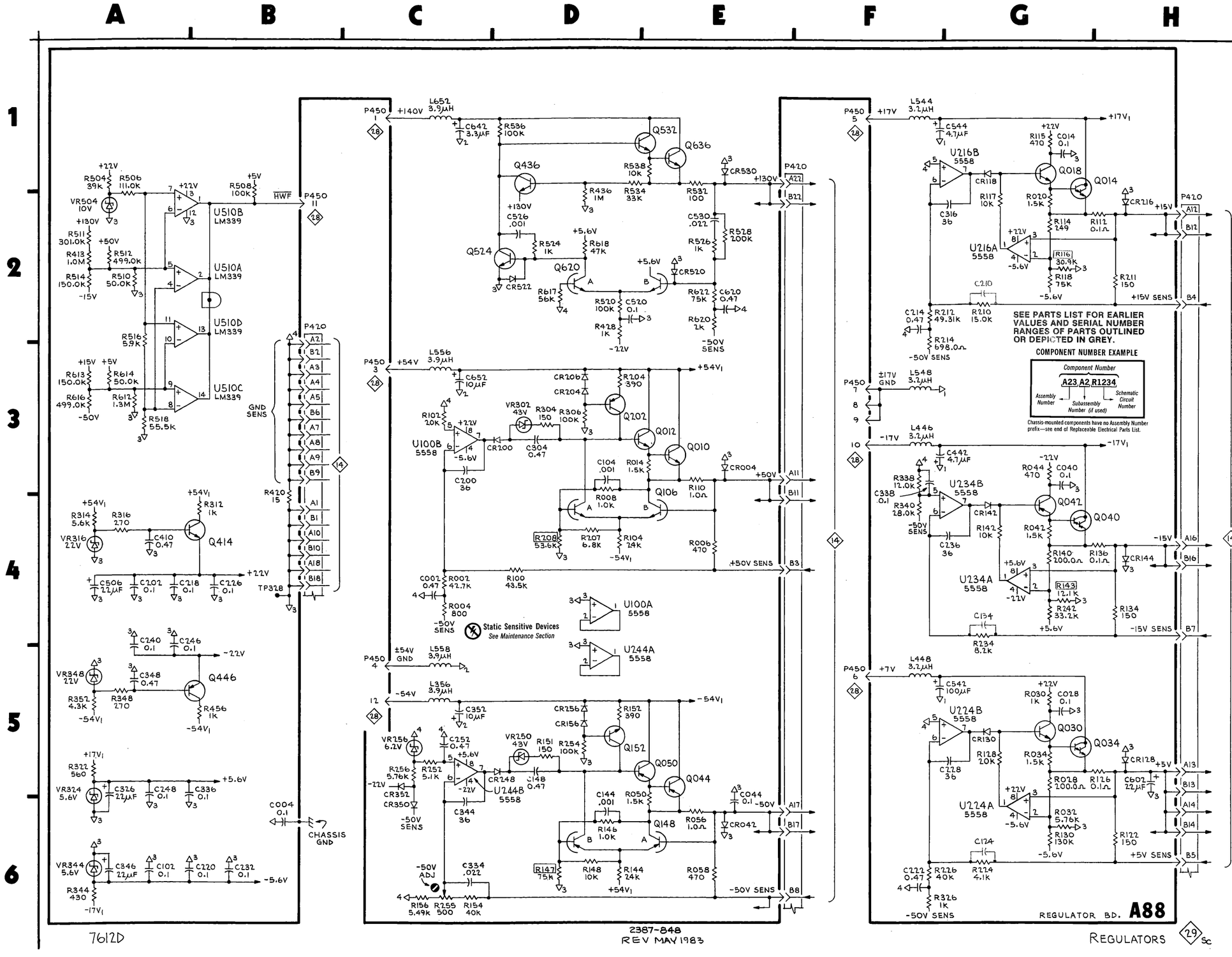
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number
C002	C4	A0	L652	C1	G5	R210
C004	B6	A0	P420	B3	E2	R211
C014	G1	A1	P420	E1	E2	R212
C028	G5	A2	P420	H2	E2	R214
C040	G4	A4	P450	B1	E5	R224
C044	E6	A4	P450	B3	E5	R226
C102	A6	B0	P450	B5	E5	R234
C104	D3	B0	P450	E1	E5	R242
C124*	G6	B2	P450	F4	E5	R252
C134*	G4	B3	P450	F5	E5	R254
C144	D6	B4	Q010	E4	A1	R255
C148	C5	B4	Q012	D3	A1	R256
C200	C3	C0	Q014	G2	A1	R304
C202	A4	C0	Q018	G1	A1	R306
C210*	G2	C1	Q030	G5	A3	R312
C214	F2	C1	Q034	G5	A3	R314
C218	B4	C1	Q040	G4	A4	R316
C220	B6	C2	Q042	G4	A4	R322
C222	F6	C2	Q044	E5	A4	R326
C226	G5	C2	Q050	D5	A5	R338
C228	F5	C2	Q106	D4	B0	R340
C232	G6	C3	Q148	E6	B4	R344
C236	F4	C3	Q152	D5	B5	R348
C240	A5	C4	Q202	D3	C0	R352
C246	B5	C5	Q414	A4	E1	R413
C248	A5	C4	Q436	C1	E3	R420
C252	C5	C5	Q446	A5	D4	R428
C304	C3	D0	Q524	C2	F2	R456
C316	F2	D1	Q532	D1	F3	R504
C326	A5	D2	Q620	C2	G2	R506
C334	C6	D3	Q636	D1	G3	R508
C336	B5	D3	R002	C4	A0	R510
C338	F4	D3	R004	C4	A0	R511
C344	C6	C4	R006	D4	A0	R512
C346	A6	D4	R008	D4	A0	R514
C348	A5	D4	R014	D4	A1	R516
C352	C5	D5	R020	G2	A1	R518
C410	A4	E1	R028	G5	A2	R520
C442	F4	E4	R030	G5	A3	R524
C506	B1	F0	R032	G6	A3	R526
C520	D2	F2	R034	G5	A3	R528
C526	C2	F2	R042	G4	A4	R532
C526	C2	F2	R044	G3	A4	R534
C530	D2	F3	R050	D6	A5	R536
C542	F5	F4	R056	E6	A5	R538
C544	F1	F4	R058	E6	A5	R612
C602	H6	G0	R100	C4	A0	R613
C620	D2	G2	R102	C3	B0	R614
C642	C1	G4	R104	D4	B0	R616
C652	C3	G5	R110	E4	B1	R617
CR004	E4	A0	R112	G2	B1	R618
CR042	E6	A4	R114	G2	B1	R620
CR118	F1	B1	R115	G1	B1	R622
CR128	G6	B3	R116	G2	B1	TP328
CR130	F5	B3	R117	G2	B1	U100A
CR142	F4	B4	R118	G2	B1	U100B
CR144	H4	B4	R122	G6	B2	U216A
CR156	D5	B5	R126	G5	B2	U216B
CR200	C3	C0	R128	G6	B2	U224A
CR204	D3	C0	R130	G6	B3	U224B
CR206	D3	C0	R134	H4	B3	U234A
CR216	H2	C1	R136	G4	B3	U234B
CR248	C5	C4	R140	G4	B4	U244A
CR256	D5	C5	R142	G4	B4	U244B
CR350	C6	D5	R143	G4	B4	U510A
CR352	C6	D5	R144	D6	B4	U510B
CR520	D2	F2	R146	D6	B5	U510C
CR522	C2	F2	R147	D6	B5	U510D
CR530	E1	F3	R148	D5	B4	VR250
L356	C5	D5	R151	D5	B5	VR256
L446	F4	E4	R152	D5	B5	VR302
L448	F5	E4	R154	C6	B5	VR316
L544	F1	F4	R156	C6	B5	VR324
L548	F4	F4	R204	D3	C0	VR344
L556	C3	F5	R207	D4	C0	VR348
L558	C5	F5	R208	D4	C0	VR504

*See Parts List for serial number ranges.

A88 ASSY — **REGULATOR** 29

Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
C002	C4	A0	L652	C1	G5	R210	G2	C1
C004	B6	A0	P420	B3	E2	R211	H2	C1
C014	G1	A1	P420	E1	E2	R212	F2	C1
C028	G5	A2	P420	H2	E2	R214	F4	C1
C040	G4	A4	P450	B1	E5	R224	G6	C2
C044	E6	A4	P450	B3	E5	R226	F6	C2
C102	A6	B0	P450	B5	E5	R234	G5	C3
C104	D3	B0	P450	E1	E5	R242	G4	C4
C124*	G6	B2	P450	F4	E5	R252	C5	C5
C134*	G4	B3	P450	F5	E5	R254	D5	B5
C144	D6	B4	Q010	E4	A1	R255	C6	B5
C148	C5	B4	Q012	D3	A1	R256	C6	C5
C200	C3	C0	Q014	G2	A1	R304	D3	D0
C202	A4	C0	Q018	G1	A1	R306	D3	D0
C210*	G2	C1	Q030	G5	A3	R312	A4	D1
C214	F2	C1	Q034	G5	A3	R314	A4	D1
C218	B4	C1	Q040	G4	A4	R316	A4	D1
C220	B6	C2	Q042	G4	A4	R322	A5	D2
C222	F6	C2	Q044	E5	A4	R326	F6	D2
C226	G5	C2	Q050	D5	A5	R338	F4	D4
C228	F5	C2	Q106	D4	B0	R340	F4	D4
C232	G6	C3	Q148	E6	B4	R344	A6	D4
C236	F4	C3	Q152	D5	B5	R348	A5	D4
C240	A5	C4	Q202	D3	C0	R352	A5	D5
C246	B5	C5	Q414	A4	E1	R413	A2	E1
C248	A5	C4	Q436	C1	E3	R420	A4	E2
C252	C5	C5	Q446	A5	D4	R428	D2	E2
C304	C3	D0	Q524	C2	F2	R456	A5	E5
C316	F2	D1	Q532	D1	F3	R504	A2	F0
C326	A5	D2	Q620	C2	G2	R506	A2	F0
C334	C6	D3	Q636	D1	G3	R508	B2	F0
C336	B5	D3	R002	C4	A0	R510	A2	F1
C338	F4	D3	R004	C4	A0	R511	A2	F1
C344	C6	C4	R006	D4	A0	R512	A2	F1
C346	A6	D4	R008	D4	A0	R514	A2	F1
C348	A5	D4	R014	D4	A1	R516	A1	F1
C352	C5	D5	R020	G2	A1	R518	A3	F1
C410	A4	E1	R028	G5	A2	R520	D2	F2
C442	F4	E4	R030	G5	A3	R524	C2	F2
C506	B1	F0	R032	G6	A3	R526	D2	F2
C520	D2	F2	R034	G5	A3	R528	D2	F2
C526	C2	F2	R042	G4	A4	R532	D1	F3
C526	C2	F2	R044	G3	A4	R534	D1	F3
C530	D2	F3	R050	D6	A5	R536	C1	F3
C542	F5	F4	R056	E6	A5	R538	D1	F3
C544	F1	F4	R058	E6	A5	R612	A3	G1
C602	H6	G0	R100	C4	A0	R613	A3	G1
C620	D2	G2	R102	C3	B0	R614	A3	G1
C642	C1	G4	R104	D4	B0	R616	A3	G1
C652	C3	G5	R110	E4	B1	R617	D2	G1
CR004	E4	A0	R112	G2	B1	R618	D2	G2
CR042	E6	A4	R114	G2	B1	R620	D2	G2
CR118	F1	B1	R115	G1	B1	R622	D2	G2
CR128	G6	B3	R116	G2	B1	TP328	A5	D2
CR130	F5	B3	R117	G2	B1	U100A	D4	B0
CR142	F4	B4	R118	G2	B1	U100B	C3	B0
CR144	H4	B4	R122	G6	B2	U216A	G2	C1
CR156	D5	B5	R126	G5	B2	U216B	F1	C1
CR200	C3	C0	R128	G6	B2	U224A	G6	C4
CR204	D3	C0	R130	G6	B3	U224B	F5	C4
CR206	D3	C0	R134	H4	B3	U234A	G4	C3
CR216	H2	C1	R136	G4	B3	U234B	F4	C3
CR248	C5	C4	R140	G4	B4	U244A	D5	C4
CR256	D5	C5	R142	G4	B4	U244B	C5	C4
CR350	C6	D5	R143	G4	B4	U510A	B2	F1
CR352	C6	D5	R144	D6	B4	U510B	A2	F1
CR520	D2	F2	R146	D6	B5	U510C	B3	F1
CR522	C2	F2	R147	D6	B5	U510D	B2	F1
CR530	E1	F3	R148	D5	B4	VR250	C5	C5
L356	C5	D5	R151	D5	B5	VR256	C5	C5
L446	F4	E4	R152	D5	B5	VR302	C3	D0
L448	F5	E4	R154	C6	B5	VR316	A4	D1
L544	F1	F4	R156	C6	B5	VR324	A5	D2
L548	F4	F4	R204	D3	C0	VR344	A6	D4
L556	C3	F5	R207	D4	C0	VR348	A5	D4
L558	C5	F5	R208	D4	C0	VR504	A2	F0

*See Parts List for serial number ranges.

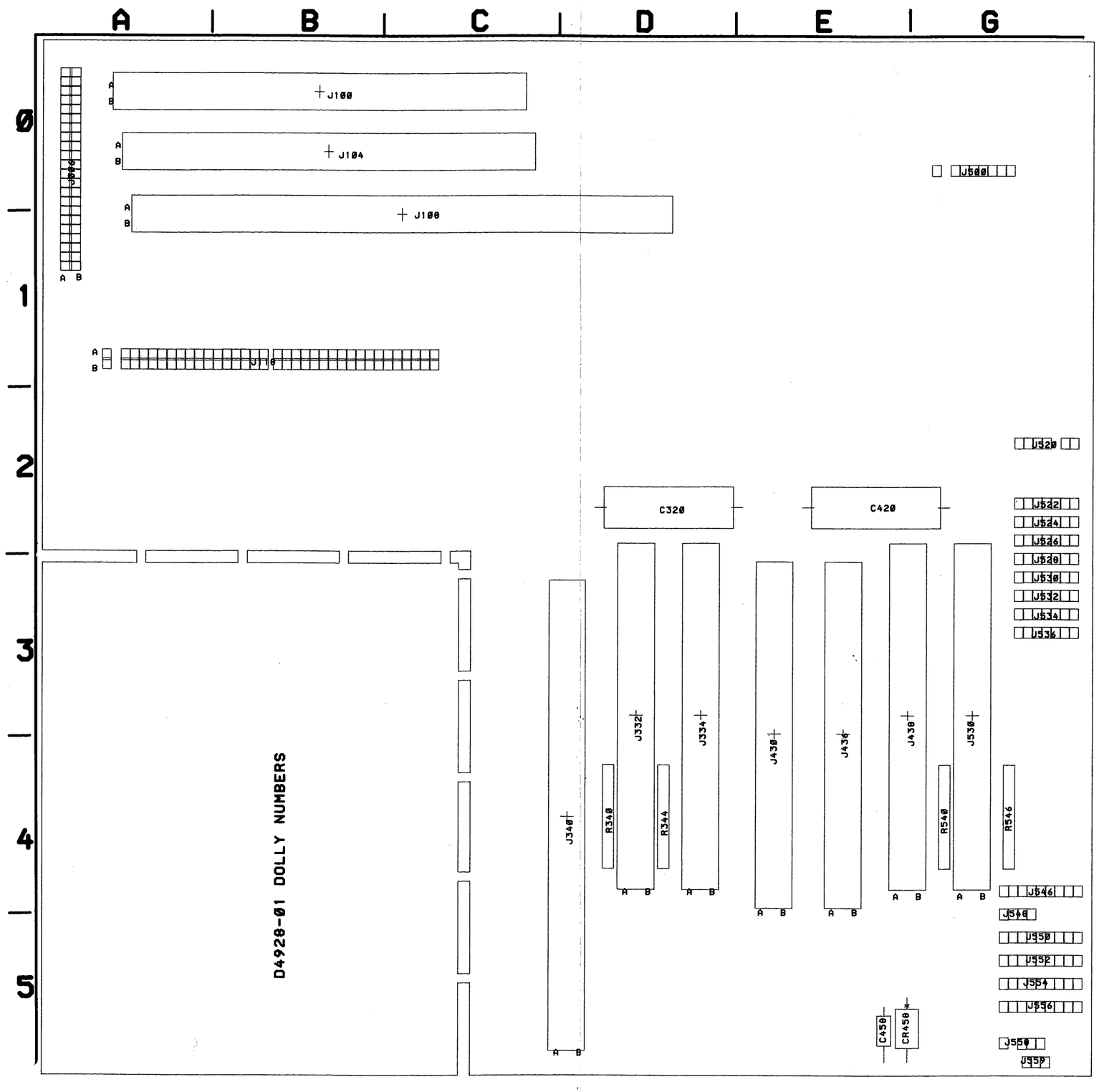


7612D

2387-848
REV MAY 1983

REGULATORS 29 Sc

MAIN INTERCONNECT A68

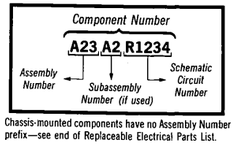


P/O A68 ASSY

Circuit Number	Schematic Location
DS5114	D6
DS5115	D6
J5001	B1
J5002	B1
J5003	B2
J5004	B2
J5101	C1
J5102	C1
J5103	C2
P006	C3

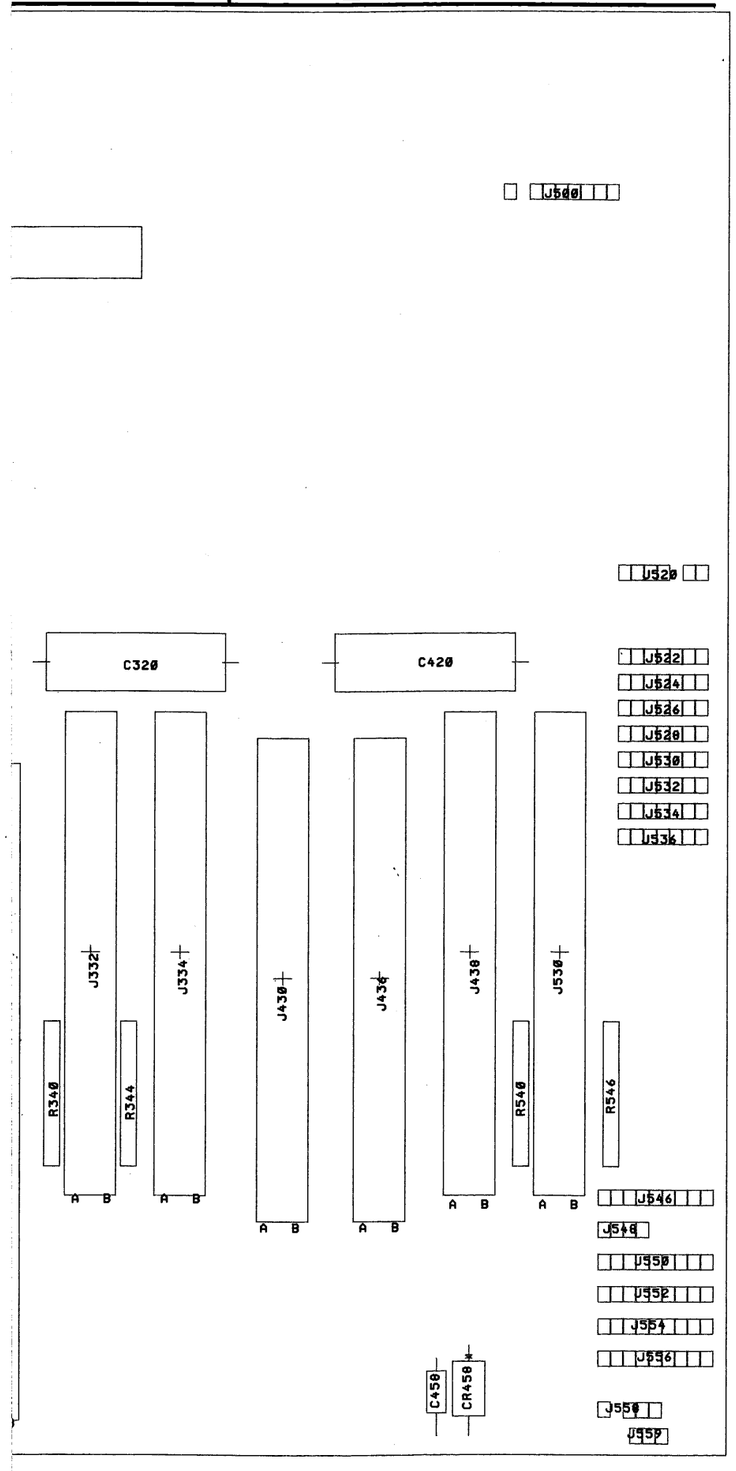
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

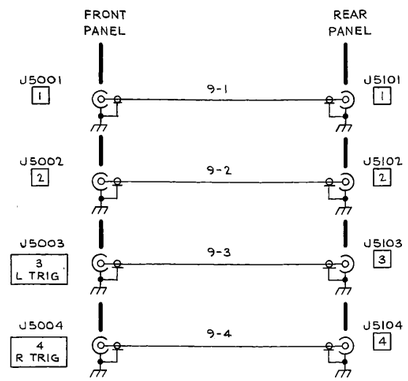
Fig. 8-31. Main Interconnect circuit board, assembly A68.

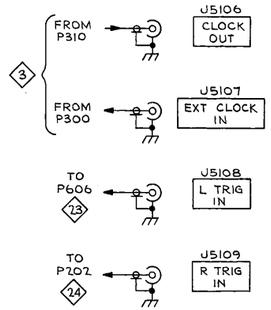


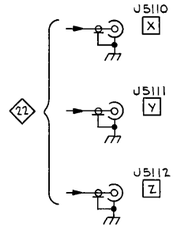
2387-849

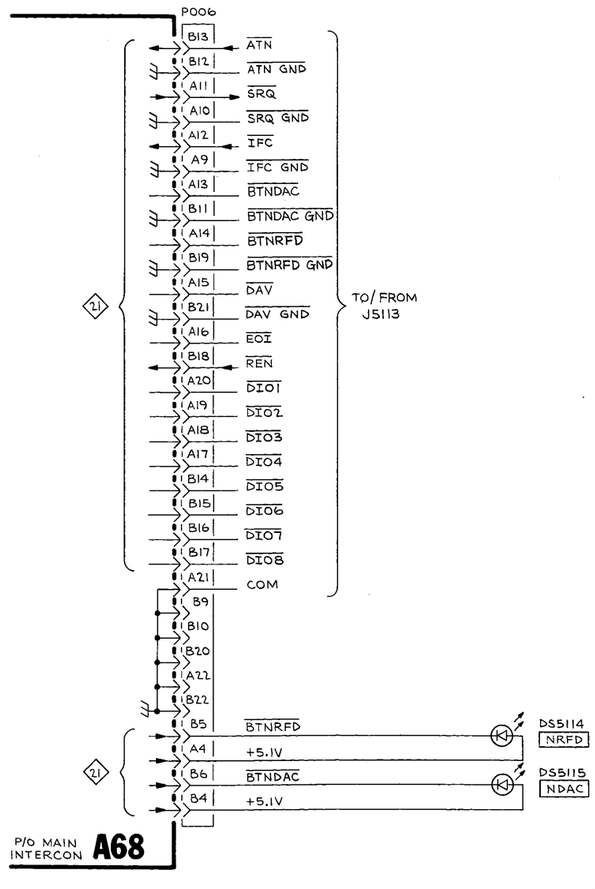
P/O A68 ASSY			REAR PANEL 30		
Circuit Number	Schematic Location	Board Location	Circuit Number	Schematic Location	Board Location
DS5114	D6	CHASSIS	J5104	C2	CHASSIS
DS5115	D6	CHASSIS	J5106	E1	CHASSIS
J5001	B1	CHASSIS	J5107	E1	CHASSIS
J5002	B1	CHASSIS	J5108	E2	CHASSIS
J5003	B2	CHASSIS	J5109	E2	CHASSIS
J5004	B2	CHASSIS	J5110	G1	CHASSIS
J5101	C1	CHASSIS	J5111	G1	CHASSIS
J5102	C1	CHASSIS	J5112	G2	CHASSIS
J5103	C2	CHASSIS	J5113	F3	CHASSIS
P006	C3	A0			

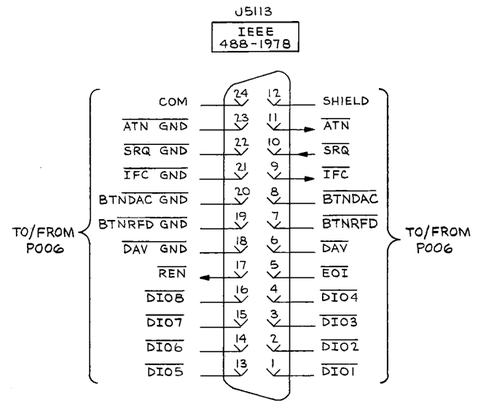
oard, assembly A68.











2387-850

7612D

REAR PANEL 30 Sc

REAR PANEL 30

MAIN INTERCONNECT (A68) SIGNALS

SIGNAL	PINOUT				
A:CS0	J332 B7(7)	J430 B9(10)†	J334 B7(7)		
A:CS1	J332 A7(7)	J334 A7(7)	J430 A9(10)†		
A:CS2	J332 B6(7)	J334 B6(7)	J430 B8(10)†		
A:CS3	J332 A6(7)	J334 A6(7)	J430 A8(10)†		
A:CS4	J332 B4(7)	J334 B4(7)	J430 B7(10)†		
A:CS5	J332 A4(7)	J334 A4(7)	J430 A7(10)†		
A:CS6	J332 B3(7)		J334 B3(7)	J430 B6(10)†	
A:CS7	J332 A3(7)	J334 A3(7)	J430 A6(10)†		
A:DADR0	J332 B11(7)	J334 B11(7)	J430 B13(10)†		
A:DADR1	J332 A11(7)	J334 A11(7)	J430 A13(10)†		
A:DADR2	J332 B10(7)	J334 B10(7)	J430 B12(10)†		
A:DADR3	J332 A10(7)	J334 A10(7)	J430 A12(10)†		
A:DADR4	J332 B9(7)	J334 B9(7)	J430 B11(10)†		
A:DADR5	J332 A9(7)	J334 A9(7)	J430 A11(10)†		
A:DADR6	J332 B8(7)	J334 B8(7)	J430 B10(10)†		
A:DADR7	J332 A8(7)	J334 A8(7)	J430 A10(10)†		
A:DI0	J522 3(4)†	J332 B28(7)			
A:DI0	J522 2(4)†	J332 A28(7)			
A:DI1	J524 5(4)†	J332 B27(7)			
A:DI1	J524 6(4)†	J332 A27(7)			
A:DI2	J522 5(4)†	J332 B26(7)			
A:DI2	J522 6(4)†	J332 A26(7)			
A:DI3	J524 3(4)†	J332 B25(7)			
A:DI3	J524 2(4)†	J332 A25(7)			
A:DI4	J526 3(4)†	J334 B28(7)			
A:DI4	J526 2(4)†	J334 A28(7)			
A:DI5	J528 5(4)†	J334 B27(7)			
A:DI5	J528 6(4)†	J334 A27(7)			
A:DI6	J526 5(4)†	J334 B26(7)			
A:DI6	J526 6(4)†	J334 A26(7)			
A:DI7	J528 3(4)†	J334 B25(7)			
A:DI7	J528 2(4)†	J334 A25(7)			
A:DN	J340 A31(5)	J430 A18(8)†			
A:DTM	J340 A19(5)†	J430 A3(10)			
A:NPTN	J340 A30(5)†	J430 B15(8)			
A:PGM	J340 A18(5)†	J430 A2(8)			
A:PTNADV	J340 A16(5)†	J430 B2(8)			
A:PTNRST	J340 A15(5)†	J430 B1(8)			
A:RD	J340 A20(5)†	J430 B5(9)			
A:SEGADV	J340 A45(5)†	J430 B28(8)			
A:SEGLNG	J340 A37(5)†	J430 B19(8)			
A:SEGRST	J340 A44(5)†	J430 A28(8)			
A:SEL	J430 A4(10)	J332 B2(7)	J334 B2(7)	J334 A2(7)	J332 A2(7)
A:SEL	J430 A27(10)	J340 A21(5)			
A:SI	J340 A43(5)†	J430 B27(9)			
A:TRIG	J430 A1(10)	J436 B4(10)†			
A:WE	J332 A12(7)	J334 A12(7)	J430 B16(10)†	J332 B12(7)	J334 B12(7)
A:AQI	J340 A3(5)†	J108 A17(17)			
ALSB	J332 A23(7)	J332 A22(7)			
ANALOG DATA	J118 B33(14)†	J108 A50(19)			
ATN	J104 A16(21)	J006 B13(30)†			
B:AQI	J340 B2(5)†	J108 A16(18)			
B:CS0	J436 B9(10)†	J438 B7(7)	J530 B7(7)		
B:CS1	J436 A9(10)†	J438 A7(7)	J530 A7(7)		
B:CS2	J436 B8(10)†	J438 B6(7)	J530 B6(7)		
B:CS3	J436 A8(10)†	J438 A6(7)	J530 A6(7)		
B:CS4	J436 B7(10)†	J438 B4(7)	J530 B4(7)		
B:CS5	J436 A7(10)†	J438 A4(7)	J530 A4(7)		
B:CS6	J436 B6(10)†	J438 B3(7)	J530 B3(7)		
B:CS7	J436 A6(10)†	J438 A3(7)	J530 A3(7)		
B:DADR0	J436 B13(10)†	J438 B11(7)	J530 B11(7)		
B:DADR1	J436 A13(10)†	J438 A11(7)	J530 A11(7)		
B:DADR2	J436 B12(10)†	J438 B10(7)	J530 B10(7)		
B:DADR3	J436 A12(10)†	J438 A10(7)	J530 A10(7)		
B:DADR4	J436 B11(10)†	J438 B9(7)	J530 B9(7)		
B:DADR5	J436 A11(10)†	J438 A9(7)	J530 A9(7)		
B:DADR6	J436 B10(10)†	J438 B8(7)	J530 B8(7)		
B:DADR7	J436 A10(10)†	J438 A8(7)	J530 A8(7)		
B:DI0	J530 3(4)†	J438 B28(7)			
B:DI0	J530 2(4)†	J438 A28(7)			
B:DI1	J532 5(4)†	J438 B27(7)			
B:DI1	J532 6(4)†	J438 A27(7)			
B:DI2	J530 5(4)†	J438 B26(7)			
B:DI2	J530 6(4)†	J438 A26(7)			
B:DI3	J532 3(4)†	J438 B25(7)			
B:DI3	J532 2(4)†	J438 A25(7)			
B:DI4	J534 3(4)†	J530 B28(7)			
B:DI4	J534 2(4)†	J530 A28(7)			
B:DI5	J536 5(4)†	J530 B27(7)			
B:DI5	J536 6(4)†	J530 A27(7)			
B:DI6	J534 5(4)†	J530 B26(7)			
B:DI6	J534 6(4)	J530 A26(7)			
B:DI7	J536 3(4)†	J530 B25(7)			
B:DI7	J536 2(4)†	J530 A25(7)			
B:DN	J340 B30(5)	J436 A18(8)			
B:DTM	J340 B18(5)†	J436 A3(10)			
B:NPTN	J340 B29(5)†	J436 B15(8)			
B:PGM	J340 B17(5)†	J436 A2(8)			
B:PTNADV	J340 B16(5)†	J436 B2(8)			
B:PTNRST	J340 B15(5)†	J436 B1(8)			
B:RD	J340 B19(5)†	J436 B5(9)			
B:SEGADV	J340 B45(5)†	J436 B28(8)			
B:SEGLNG	J340 B36(5)†	J436 B19(8)			
B:SEGRST	J340 B44(5)†	J436 A28(8)			
B:SEL	J436 A4(10)	J530 B2(7)	J438 B2(7)	J438 A2(7)	J530 A2(7)
	J530 B2(7)				
B:SE1	J340 B21(5)†	J436 A27(10)			
B:SI	J340 B42(5)†	J436 B27(9)			
B:TRIG	J430 B4(10)†	J436 A1(10)			
B:WE	J438 A12(7)	J530 A12(7)	J530 B12(7)	J438 B12(7)	J436 B16(10)
BADR0	J340 B14(5)	J108 B48(17)†	J104 B35(20)	J100 B34(25)	J554 1(1)
BADR1	J340 A14(5)	J108 B47(17)†	J104 B34(20)	J100 B33(25)	J552 9(1)
BADR2	J340 B12(5)	J108 B45(17)†	J104 B33(20)	J100 B32(25)	J552 7(1)
BADR3	J340 A13(5)	J108 B44(17)†	J104 B32(20)	J552 5(1)	
BADR4	J340 B11(5)	J108 B42(17)†	J104 B31(20)		J552 3(1)
BADR5	J340 A12(5)	J108 B41(17)†	J104 B30(20)	J552 1(1)	
BADR6	J108 B39(17)†	J104 B28(20)			
BADR7	J108 B38(17)†	J104 B27(20)			
BADR8	J108 B36(17)†	J104 B26(20)			
BADR9	J108 B35(17)†	J104 B25(20)			
BADR10	J108 B34(17)†	J104 B24(20)			
BD0	J340 B6(6)	J108 B19(17)	J104 B11(20)	J100 B14(25)	J118 A20(14)
	J556 9(1)				
BD1	J340 A5(6)	J108 B20(17)	J104 B12(20)	J100 B15(25)	J556 7(1)
BD2	J340 B7(6)	J108 B22(17)	J100 B16(25)	J104 B14(20)	J556 6(1)
BD3	J340 A6(6)	J108 B23(17)	J104 B15(20)	J100 B17(25)	J556 4(1)
BD4	J340 B8(6)	J104 B17(20)	J108 B25(17)	J100 B18(5)	J556 3(1)
BD5	J340 A8(6)	J108 B26(17)	J104 B18(20)	J100 B19(25)	J556 1(1)
BD6	J104 B20(20)	J100 B20(25)	J554 4(1)		
	J340 B10(6)	J108 B28(17)			
BD7	J340 A9(6)	J108 B29(17)	J104 B21(20)	J100 B21(25)	J554 3(1)
BEOP	J430 B18(10)	J436 A19(10)			
BLSB	J438 A23(7)	J438 A22(7)			
BR/W	J340 A10(5)	J108 B50(17)†	J100 B31(25)	J104 B36(20)	J554 9(1)
BTNDAC	J104 A23(21)†	J006 B6(30)			
BTNRFD	J104 A21(21)†	J006 B5(30)			
CK2	J108 A19(17)†	J104 B6(20)			
COM SENS	J500 5(27)				

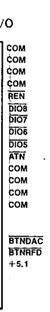
†Signal source

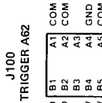
*Unused Signal

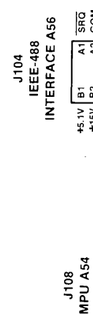
SIGNAL	PINOUT		
$\overline{\text{DAV}}$	J104 A7(21)	J006 A15(30)	
$\overline{\text{DI01}}$	J104 A13(21)†	J006 A20(30)	
$\overline{\text{DI02}}$	J104 A12(21)†	J006 A19(30)	
$\overline{\text{DI03}}$	J104 A11(21)†	J006 A18(30)	
$\overline{\text{DI04}}$	J104 A10(21)†	J006 A17(30)	
$\overline{\text{DI05}}$	J104 A17(21)†	J006 B14(30)	
$\overline{\text{DI06}}$	J104 A18(21)	J006 B15(30)	
$\overline{\text{DI07}}$	J104 A19(21)	J006 B16(30)	
$\overline{\text{DI08}}$	J104 A20(21)	J006 B17(30)	
DO0	J340 A36(6)	J438 A18(7)†	J332 A18(7)
DO1	J340 A35(6)	J332 A16(7)†	J438 A16(7)
DO2	J340 A33(6)	J332 A15(7)†	J438 A15(7)
DO3	J340 A32(6)	J332 A13(7)†	J438 A13(7)
DO4	J340 B35(6)	J334 B18(7)†	J530 B18(7)†
DO5	J340 B34(6)	J334 B16(7)†	J530 B16(7)†
DO6	J340 B33(6)	J334 B15(7)†	J530 B15(7)
DO7	J340 B32(6)	J334 B13(7)†	J530 B13(7)†
ECKSL	J100 A28(25)†	J546 5(3)	
ED0	J340 A38(6)†	J430 A21(8)	J436 A21(8)
ED1	J340 B38(6)†	J430 B21(8)	J436 B21(8)
ED2	J340 A39(6)†	J430 A22(8)	J436 A22(8)
ED3	J340 B39(6)†	J430 B22(8)	J436 B22(8)
ED4	J340 A41(6)†	J430 A23(8)	J436 A23(8)
ED5	J340 B40(6)†	J430 B23(8)	J436 B23(8)
ED6	J340 A42(6)†	J430 A24(8)	J436 A24(8)
ED7	J340 B41(6)†	J430 B24(18)†	J436 B24(8)†
$\overline{\text{EOI}}$	J104 A8(21)	J006 A16(30)	
FPI	J108 A10(18)	J554 6(1)	
$\overline{\text{FPSEL}}$	J108 B17(17)†	J550 7(1)	
$\overline{\text{HALT}}$*	J108 A47(17)		
HD0	J340 B24(6)†	J104 A24(21)	
HD1	J340 A25(6)†	J104 A25(21)	
HD2	J340 B25(6)†	J104 A27(21)	
HD3	J340 A26(6)†	J104 A28(21)	
HD4	J340 B27(6)†	J104 A29(21)	
HD5	J340 A27(6)†	J104 A30(21)	
HD6	J340 B28(6)†	J104 A32(21)	
HD7	J340 A29(6)†	J104 A33(21)	
$\overline{\text{HWF}}$	J108 B10(17)	J500 3(27)†	
$\overline{\text{IFC}}$	J104 A3(21)†	J006 A12(30)†	
IOI	J108 A18(18)†	J104 B5(20)†	
L:GATE	J436 B3(10)	J100 B25(23)†	
L:TRIG'D	J100 A31(25)†	J550 4(2)	
$\overline{\text{LSEND}}$	J340 B23(5)†	J104 A36(21)	
$\overline{\text{MEMSEL 0}}$*	J108 A6(17)		
$\overline{\text{MEMSEL 1}}$*	J108 B12(17)		
$\overline{\text{MEMSEL 2}}$*	J108 B7(17)		
$\overline{\text{MEMSEL 6}}$*	J108 B5(17)		
$\overline{\text{MEMSEL 7}}$*	J108 A7(17)		
MPUCLK	J340 B1(5)†	J108 B8(17)	
$\overline{\text{NDAC}}$	J104 A4(21)	J006 A13(30)	
$\overline{\text{NRFD}}$	J104 A6(21)	J006 A14(30)	
PON	J108 B11(17)	J500 1(27)†	
$\overline{\text{POWER ON}}$	J500 7(27)	J550 1(2)†	
$\overline{\text{POWER RETURN}}$	J500 8(27)†	J550 2(2)	
R:GATE	J430 B3(10)	J100 B27(24)†	
R:TRIG'D	J100 A30(24)†	J550 5(2)	

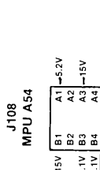
2387-851

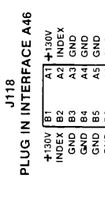
SIGNAL	PINOUT			
R-REN	J108 A21(18)	J104 A14(21)†		
REN	J104 A22(21)	J006 B18(30)		
RORST	J118 A23(14)	J108 A24(19)†		
ROT	J118 A24(14)	J108 A25(19)†		
RST	J340 A4(5)	J104 B4(20)	J550 9(1)	J108 A14(17)†
RTL	J108 B6			
SHIFT	J118 A22(14)	J108 A23(19)†		
SRQ	J104 A1(21)†	J006 A11(30)		
STROBE	J340 B4(5)	J100 B13(25)	J108 B31(7)†	J554 8(1)
	J104 B9(21)			
TIMESLOT	J118 A21(14)	J108 A22(19)†		
TLTRSEL	J340 B3(5)	J108 B13(17)†		
TRGSEL	J108 B14(17)†	J100 B22(25)		
VMA*	J108 B15(17)			
XMTI	J340 A2(5)†	J108 A20(18)		
YSENT	J340 A23(5)	J104 A35(21)†		
7KATN	J118 B25(14)	J108 A37(19)†		
7KDAV	J118 A31(14)	J108 A42(19)†		
7KDI01	J118 A28(14)	J108 A33(19)		
7KDI02	J118 B23(14)	J108 A31(19)		
7KDI03	J118 A27(14)	J108 A32(19)		
7KDI04	J118 B22(14)	J108 A30(19)		
7KDI05	J118 A34(14)	J108 A45(19)		
7KDI06	J118 A35(14)	J108 A46(19)		
7KDI07	J118 A32(14)	J108 A43(19)		
7KDI08	J118 A33(14)	J108 A44(19)		
7KEOI	J118 A25(14)	J108 A26(19)†		
7KIFC	J118 B26(14)	J108 A38(19)†		
7KLVADR	J118 B32(14)	J108 A29(19)†		
7KNDAC	J118 A29(14)†	J108 A34(19)		
7KNRFD	J118 A30(14)†	J108 A40(19)		
7KREN	J118 B24(14)	J108 A36(19)†		
7KRVADR	J118 B31(14)	J108 A28(19)†		
7KSND	J118 B27(14)†	J108 A39(19)		
7KSRQ	J118 A26(14)†	J108 A27(19)		
10MSEL	J108 B33(17)†	J104 B23(20)		
10RSEL	J108 B16(17)†	J104 B8(20)		
+5V	J118 B14(14)	J118 A14(14)	J100 B6(25)	
	J520 3(11)	J546 4(3)	J558 3(4)	
+5.1V	J340 A50(6)	J118 B13(14)	J108 B3(19)	J104 B1(21) J100 B5(25)
	J118 A12(14)	J108 B4(19)	J118 B12(14)	J118 A13(14) J100 B5(25)
	J548 1(2)	J006 A4(30)	J006 B4(30)	J548 3(2) J548 2(2)
+5.1 SENS	J500 9(27)			
+15V	J118 B10(14)	J118 A10(14)	J108 B1(19)	J104 B2(21) J100 B4(25)
	J520 2(11)	J546 7(7)		
+50V	J118 B9(14)	J118 A9(14)	J520 1(11)	
+130V	J118 B1(14)	J118 A1(14)	J558 1(12)	
-2V	J340 B50(6)	J322 A30(7)	J334 A30(7)	J332 B30(7) J334 B30(7)
	J430 A30(8)	J436 A30(8)	J430 B30(8)	J436 B30(8) J438 A30(8)
	J530 A30(8)	J438 B30(8)	J530 B30(8)	J546 2(3)
-2 SENS	J500 6(27)			
-5.2V	J340 B48(6)	J118 B16(14)	J108 A1†	J100 B7(25) J118 A16(14)
	J332 A33(7)	J436 A33(8)	J334 A33(7)	J438 A33(8) J430 A33(8)
	J530 A33(8)	J332 A32(7)	J436 A32(8)	J334 A32(7) J438 B33(8)
	J430 B33(8)	J530 B33(8)	J332 B33(7)	J436 B33(8) J334 B33(7)
	J438 B32(8)	J430 A32(8)	J530 A32(8)	J332 B32(7) J436 B32(8)
	J334 B32(7)	J438 A32(8)	J430 B32(8)	J530 B32(8) J546 1(3)
-5.2 SENS	J500 4(27)			
-15V	J340 A48(6)	J118 B17(14)	J108 A3†	J104 B3(21) J118 A17(14)
	J100 B8(25)	J520 6(4)	J546 9(3)	J559 2(4)
-50V	J118 B18(14)	J118 A18(14)	J520 7(11)	
-12V	J559 1	J558 4		

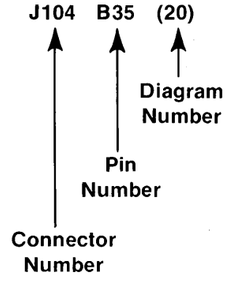


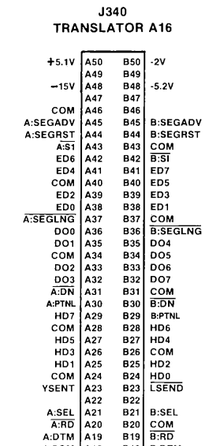


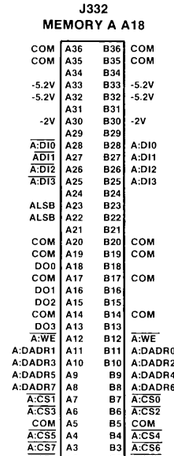


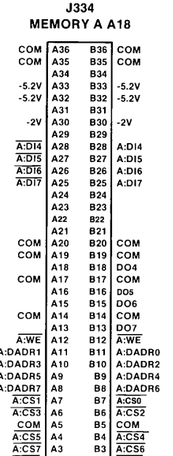












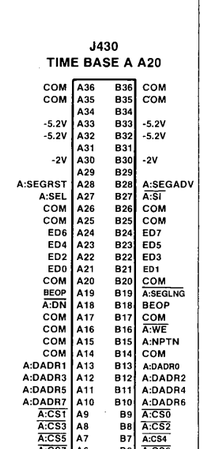


Fig. 8-32. Main Interconn

MAIN INTERCONNECT (A68) CONNECTORS

J100 TRIGGER A62

GND	B1	A1	COM
GND	B2	A2	COM
	B3	A3	
+15V	B4	A4	GND
+5.1V	B5	A5	COM
+5V	B6	A6	GND
−5.2	B7	A7	COM
−15V	B8	A8	GND
	B9	A9	
	B10	A10	
	B11	A11	
	B12	A12	
STROBE	B13	A13	COM
BD0	B14	A14	COM
BD1	B15	A15	COM
BD2	B16	A16	COM
BD3	B17	A17	COM
BD4	B18	A18	COM
BD5	B19	A19	COM
BD6	B20	A20	COM
BD7	B21	A21	COM
TRG SEL	B22	A22	COM
	B23	A23	
COM	B24	A24	COM
L:GATE	B25	A25	COM
COM	B26	A26	COM
R:GATE	B27	A27	COM
COM	B28	A28	ECKSL
	B29	A29	
COM	B30	A30	R:TRIG'D
BR W	B31	A31	L:TRIG'D
BADR2	B32	A32	COM
BADR1	B33	A33	COM
BADR0	B34	A34	COM
COM	B35	A35	COM
	B36	A36	

J104 IEEE-488 INTERFACE A56

+5.1V	B1	A1	SRQ
+15V	B2	A2	COM
-15V	B3	A3	IFC
RST	B4	A4	NDAC
IOI	B5	A5	COM
CK2	B6	A6	NRFD
COM	B7	A7	DAV
I0RSEL	B8	A8	EOI
STROBE	B9	A9	COM
COM	B10	A10	DIO4
BD0	B11	A11	DIO3
BD1	B12	A12	DIO2
COM	B13	A13	DIO1
BD2	B14	A14	R-REN
BD3	B15	A15	COM
COM	B16	A16	ATN
BD4	B17	A17	DIO5
BD5	B18	A18	DIO6
COM	B19	A19	DIO7
BD6	B20	A20	DIO8
BD7	B21	A21	BTNRFD
COM	B22	A22	REN
10MSEL	B23	A23	BTNDAC
BADR10	B24	A24	HD0
BADR9	B25	A25	HD1
BADR8	B26	A26	COM
BADR7	B27	A27	HD2
BADR6	B28	A28	HD3
COM	B29	A29	HD4
BADR5	B30	A30	HD5
BADR4	B31	A31	COM
BADR3	B32	A32	HD6
BADR2	B33	A33	HD7
BADR1	B34	A34	COM
BADR0	B35	A35	YSENT
BR W	B36	A36	LSEND

J108 MPU A54

+15V	B1	A1	−5.2V
	B2	A2	
+5.1V	B3	A3	−15V
+5.1V	B4	A4	
(NC)MEMSEL6	B5	A5	COM
(NC)RTL	B6	A6	MEMSEL0 (NC)
(NC)MEMSEL2	B7	A7	MEMSEL7 (NC)
MPUCLK	B8	A8	
COM	B9	A9	
HWF	B10	A10	FPI
PON	B11	A11	
(NC)MEMSEL1	B12	A12	COM
TLTRSEL	B13	A13	
TRGSEL	B14	A14	RST
(NC) VMA	B15	A15	COM
I0RSEL	B16	A16	B:AQI
FPSEL	B17	A17	A:AQI
COM	B18	A18	IOI
BD0	B19	A19	CK2
BD1	B20	A20	XMTI
COM	B21	A21	R-REN
BD2	B22	A22	TIMESLOT
BD3	B23	A23	SHIFT
COM	B24	A24	RORST
BD4	B25	A25	ROT
BD5	B26	A26	7KEOI
COM	B27	A27	7KSRQ
BD6	B28	A28	7KRVADR
BD7	B29	A29	7KLVADR
COM	B30	A30	7KDIO4
STROBE	B31	A31	7KDIO2
COM	B32	A32	7KDIO3
10MSEL	B33	A33	7KDIO1
BADR10	B34	A34	7KNDAC
BADR9	B35	A35	COM
BADR8	B36	A36	7KREN
COM	B37	A37	7KATN
BADR7	B38	A38	7KIFC
BADR6	B39	A39	7KSND
COM	B40	A40	7KNRFD
BADR5	B41	A41	COM
BADR4	B42	A42	7KDAV
COM	B43	A43	7KDIO7
BADR3	B44	A44	7KDIO8
BADR2	B45	A45	7KDIO5
COM	B46	A46	7KDIO6
BADR1	B47	A47	HALT(NC)
BADR0	B48	A48	GND
COM	B49	A49	COM
BR/W	B50	A50	ANALOG DATA

J118 PLUG IN INTERFACE A46

+130V	B1	A1	+130V
INDEX	B2	A2	INDEX
GND	B3	A3	GND
GND	B4	A4	GND
GND	B5	A5	GND
GND	B6	A6	GND
GND	B7	A7	GND
GND	B8	A8	GND
+50V	B9	A9	+50V
+15V	B10	A10	+15V
COM	B11	A11	COM
+5.1V	B12	A12	+5.1V
+5.1V	B13	A13	+5.1V
+5V	B14	A14	+5V
GND	B15	A15	GND
−5.2V	B16	A16	−5.2V
−15V	B17	A17	−15V
−50V	B18	A18	−50V
	B19	A19	
	B20	A20	BD0
GND	B21	A21	TIMESLOT
7KDIO4	B22	A22	SHIFT
7KDIO2	B23	A23	RORST
7KREN	B24	A24	ROT
7KATN	B25	A25	7KEOI
7KIFC	B26	A26	7KSRQ
7KSND	B27	A27	7KDIO3
GND	B28	A28	7KDIO1
GND	B29	A29	7KNDAC
GND	B30	A30	7KNRFD
7KRVADR	B31	A31	7KDAV
7KLVADR	B32	A32	7KDIO7
ANALOG DATA	B33	A33	7KDIO8
	B34	A34	7KDIO5
	B35	A35	7KDIO6
	B36	A36	

J104 B35 (20)

Connector Number — Pin Number — Diagram Number

J340 TRANSLATOR A16

+5.1V	A50	B50	-2V
	A49	B49	
−15V	A48	B48	-5.2V
	A47	B47	
COM	A46	B46	
A:SEGADV	A45	B45	B:SEGADV
A:SEGRST	A44	B44	B:SEGRST
A:SI	A43	B43	COM
ED6	A42	B42	B:SI
ED4	A41	B41	ED7
COM	A40	B40	ED5
ED2	A39	B39	ED3
ED0	A38	B38	ED1
A:SEGLNG	A37	B37	COM
DO0	A36	B36	B:SEGLNG
DO1	A35	B35	DO4
COM	A34	B34	DO5
DO2	A33	B33	DO6
DO3	A32	B32	DO7
A:DN	A31	B31	COM
A:PTNL	A30	B30	B:DN
HD7	A29	B29	B:PTNL
COM	A28	B28	HD6
HD5	A27	B27	HD4
HD3	A26	B26	COM
HD1	A25	B25	HD2
COM	A24	B24	HD0
YSENT	A23	B23	LSEND
	A22	B22	
A:SEL	A21	B21	B:SEL
A:RD	A20	B20	COM
A:DTM	A19	B19	B:RD
A:PGM	A18	B18	B:DTM
COM	A17	B17	B:PGM
A:PTNADV	A16	B16	B:PTNADV
A:PTNRST	A15	B15	B:PTNRST
BADR1	A14	B14	BADR0
BADR3	A13	B13	COM
BADR5	A12	B12	BADR2
NC	A11	B11	BADR4
BR W	A10	B10	BD6
BD7	A9	B9	COM
BD5	A8	B8	BD4
COM	A7	B7	BD2
BD3	A6	B6	BD0
BD1	A5	B5	COM
RST	A4	B4	STROBE
A:AQ1	A3	B3	TLTRSEL
XMTI	A2	B2	B:AQI
COM	A1	B1	MPU CLK

J332 MEMORY A A18

COM	A36	B36	COM
COM	A35	B35	COM
	A34	B34	
-5.2V	A33	B33	-5.2V
-5.2V	A32	B32	-5.2V
	A31	B31	
-2V	A30	B30	-2V
	A29	B29	
A:DI0	A28	B28	A:DI0
ADI1	A27	B27	A:DI1
A:DI2	A26	B26	A:DI2
A:DI3	A25	B25	A:DI3
	A24	B24	
ALSB	A23	B23	
ALSB	A22	B22	
	A21	B21	
COM	A20	B20	COM
COM	A19	B19	COM
DO0	A18	B18	
COM	A17	B17	COM
DO1	A16	B16	
DO2	A15	B15	
COM	A14	B14	COM
DO3	A13	B13	
A:WE	A12	B12	A:WE
A:DADR1	A11	B11	A:DADR0
A:DADR3	A10	B10	A:DADR2
A:DADR5	A9	B9	A:DADR4
A:DADR7	A8	B8	A:DADR6
A:CS1	A7	B7	A:CS0
A:CS3	A6	B6	A:CS2
COM	A5	B5	COM
A:CS5	A4	B4	A:CS4
A:CS7	A3	B3	A:CS6
A:SEL	A2	B2	A:SEL
COM	A1	B1	COM

J334 MEMORY A A18

COM	A36	B36	COM
COM	A35	B35	COM
	A34	B34	
-5.2V	A33	B33	-5.2V
-5.2V	A32	B32	-5.2V
	A31	B31	
-2V	A30	B30	-2V
	A29	B29	
A:DI4	A28	B28	A:DI4
A:DI5	A27	B27	A:DI5
A:DI6	A26	B26	A:DI6
A:DI7	A25	B25	A:DI7
	A24	B24	
	A23	B23	
	A22	B22	
	A21	B21	
COM	A20	B20	COM
COM	A19	B19	COM
	A18	B18	DO4
COM	A17	B17	COM
	A16	B16	DO5
	A15	B15	DO6
COM	A14	B14	COM
	A13	B13	DO7
A:WE	A12	B12	A:WE
A:DADR1	A11	B11	A:DADR0
A:DADR3	A10	B10	A:DADR2
A:DADR5	A9	B9	A:DADR4
A:DADR7	A8	B8	A:DADR6
A:CS1	A7	B7	A:CS0
A:CS3	A6	B6	A:CS2
COM	A5	B5	COM
A:CS5	A4	B4	A:CS4
A:CS7	A3	B3	A:CS6
A:SEL	A2	B2	A:SEL
COM	A1	B1	COM

J430 TIME BASE A A20

COM	A36	B36	COM
COM	A35	B35	COM
	A34	B34	
-5.2V	A33	B33	-5.2V
-5.2V	A32	B32	-5.2V
	A31	B31	
-2V	A30	B30	-2V
	A29	B29	
A:SEGRST	A28	B28	A:SEGADV
A:SEL	A27	B27	A:SI
COM	A26	B26	COM
COM	A25	B25	COM
ED6	A24	B24	ED7
ED4	A23	B23	ED5
ED2	A22	B22	ED3
ED0	A21	B21	ED1
COM	A20	B20	COM
BEOP	A19	B19	A:SEGLNG
A:DN	A18	B18	BEOP
COM	A17	B17	COM
COM	A16	B16	A:WE
COM	A15	B15	A:NPTN
COM	A14	B14	COM
A:DADR1	A13	B13	A:DADR0
A:DADR3	A12	B12	A:DADR2
A:DADR5	A11	B11	A:DADR4
A:DADR7	A10	B10	A:DADR6
A:CS1	A9	B9	A:CS0
A:CS3	A8	B8	A:CS2
A:CS5	A7	B7	A:CS4
A:CS7	A6	B6	A:CS6
COM	A5	B5	A:RD
A:SEL	A4	B4	B:TRIG OUT
A:DTM	A3	B3	R:GATE IN
A:PGM	A2	B2	A:PTNADV
A:TRIG	A1	B1	A:PTNRST

J436 TIME BASE B A20

COM	A36	B36	COM
COM	A35	B35	COM
	A34	B34	
-5.2V	A33	B33	-5.2V
-5.2V	A32	B32	-5.2V
	A31	B31	
-2V	A30	B30	-2V
	A29	B29	
B:SEGRST	A28	B28	B:SEGADV
B:SEL	A27	B27	B:SI
COM	A26	B26	COM
COM	A25	B25	COM
ED6	A24	B24	ED7
ED4	A23	B23	ED5
ED2	A22	B22	ED3
ED0	A21	B21	ED1
COM	A20	B20	COM
BEOP	A19	B19	B:SEGLNG
B:DN	A18	B18	BEOP
COM	A17	B17	COM
COM	A16	B16	B:WE
COM	A15	B15	B:NPTN
COM	A14	B14	COM
B:DADR1	A13	B13	B:DADR0
B:DADR3	A12	B12	B:DADR2
B:DADR5	A11	B11	B:DADR4
B:DADR7	A10	B10	B:DADR6
B:CS1	A9	B9	B:CS0
B:CS3	A8	B8	B:CS2
B:CS5	A7	B7	BCS4
B:CS7	A6	B6	B:CS6
COM	A5	B5	B:RD
B:SEL	A4	B4	A:TRIG OUT
B:DTM	A3	B3	L:GATE IN
B:PGM	A2	B2	B:PTNADV
B:TRIG	A1	B1	B:PTNRST

J438 MEMORY B A18

COM	A36	B36	COM
COM	A35	B35	COM
	A34	B34	
-5.2V	A33	B33	-5.2V
-5.2V	A32	B32	-5.2V
	A31	B31	
-2V	A30	B30	-2V
	A29	B29	
B:DI0	A28	B28	B:DI0
B:DI1	A27	B27	B:DI1
B:DI2	A26	B26	B:DI2
B:DI3	A25	B25	B:DI3
	A24	B24	
BLSB	A23	B23	
BLSB	A22	B22	
	A21	B21	
COM	A20	B20	COM
COM	A19	B19	COM
DO0	A18	B18	
COM	A17	B17	COM
DO1	A16	B16	
DO2	A15	B15	
COM	A14	B14	COM
DO3	A13	B13	
B:WE	A12	B12	B:WE
B:DADR1	A11	B11	B:DADR0
B:DADR3	A10	B10	B:DADR2
B:DADR5	A9	B9	B:DADR4
B:DADR7	A8	B8	B:DADR6
B:CS1	A7	B7	B:CS0
B:CS3	A6	B6	B:CS2
COM	A5	B5	COM
B:CS5	A4	B4	B:CS4
B:CS7	A3	B3	B:CS6
B:SEL	A2	B2	B:SEL
COM	A1	B1	COM

J530 MEMORY B A18

COM	A36	B36	COM
COM	A35	B35	COM
	A34	B34	
-5.2V	A33	B33	-5.2V
-5.2V	A32	B32	-5.2V
	A31	B31	
-2V	A30	B30	-2V
	A29	B29	
B:DI4	A28	B28	B:DI4
B:DI5	A27	B27	B:DI5
B:DI6	A26	B26	B:DI6
B:DI7	A25	B25	B:DI7
	A24	B24	
	A23	B23	
	A22	B22	
	A21	B21	
COM	A20	B20	COM
COM	A19	B19	COM
	A18	B18	DO4
COM	A17	B17	COM
	A16	B16	DO5
	A15	B15	DO6
COM	A14	B14	COM
	A13	B13	D07
B:WE	A12	B12	B:WE
B:DADR1	A11	B11	B:DADR0
B:DADR3	A10	B10	B:DADR2
B:DADR5	A9	B9	B:DADR4
B:DADR7	A8	B8	B:DADR6
B:CS1	A7	B7	B:CS0
B:CS3	A6	B6	B:CS2
COM	A5	B5	COM
B:CS5	A4	B4	B:CS4
B:CS7	A3	B3	B:CS6
B:SEL	A2	B2	B:SEL
COM	A1	B1	COM

J500 CONTROL

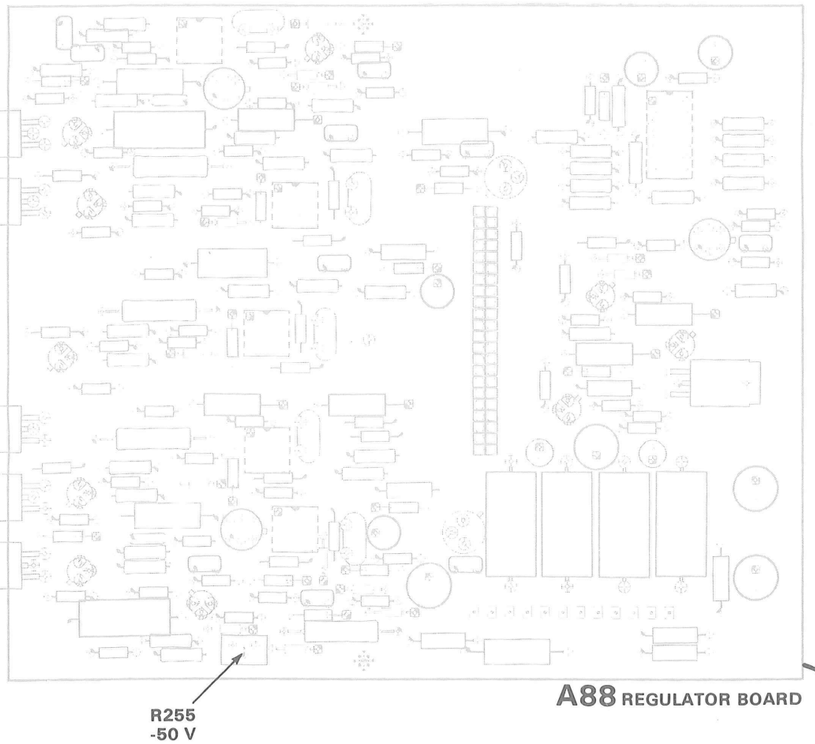
1	PON
2	INDEX
3	HWF
4	-5.2 SENS
5	COM SENS
6	-2 SENS
7	POWER ON
8	POWER ON RETURN
9	+5.1 SENS

Single-row connectors

J520	+50V	+15V	+5V	GND		-15V	-50V		
J522	COM	A:DIO	A:DIO	COM	A:DI2	A:DI2	COM		
J524	COM	A:DI3	A:DI3	COM	A.DI1	A:DI1	COM		
J526	COM	A:DI4	A:DI4	COM	A:DI6	A:DI6	COM		
J528	COM	A:DI7	A:DI7	COM	A:DI5	A:DI5	COM		
J530	COM	B:DIO	B:DIO	COM	B:DI2	B:DI2	COM		
J532	COM	B:DI3	B:DI3	COM	B:DI1	B:DI1	COM		
J534	COM	B:DI4	B:DI4	COM	B:DI6	B:DI6	COM		
J536	COM	B:DI7	B:DI7	COM	B:DI5	B:DI5	COM		
J546	-5.2V	-2V	COM	+5V	ECKSL	COM	+15V	GND	-15V
J548	+5.1V	+5.1V	+5.1V	COM					
J550	POWER ON	POWER ON RET	COM	L:TRIG'D	R:TRIG'D	COM	FPSEL	COM	RST
J552	BADR5	COM	BADR4	COM	BADR3	COM	BADR2	COM	BADR1
J554	BADR0	COM	BD7	BD6	COM	FPI	COM	STROBE	BR/W
J556	BD5	COM	BD4	BD3	COM	BD2	BD1	COM	BD0
J558	+130V	INDEX	+5V	-12V	GND				
J559	-12V	-15V	GND						

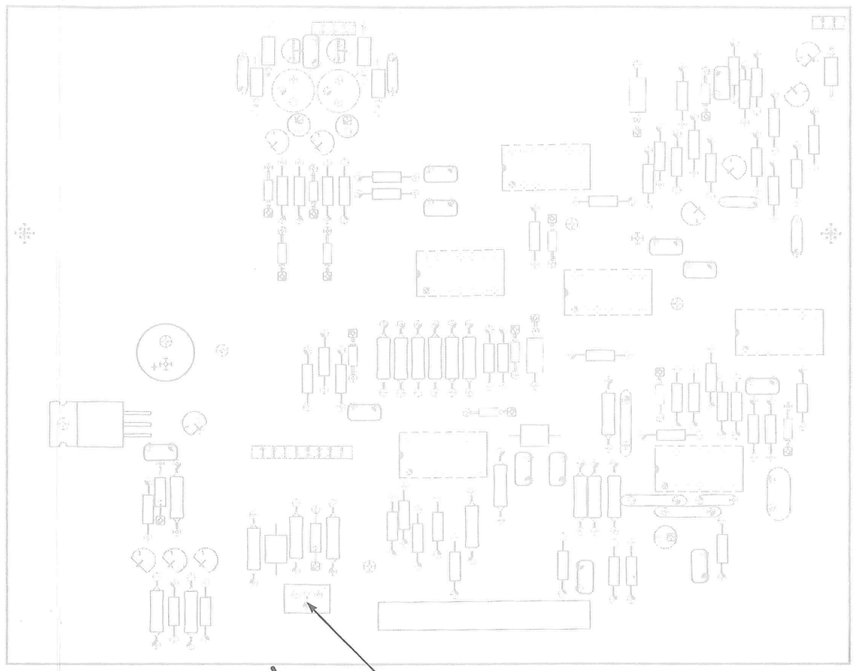
Fig. 8-32. Main Interconnect (A68) connectors.

2387-852



A88 REGULATOR BOARD

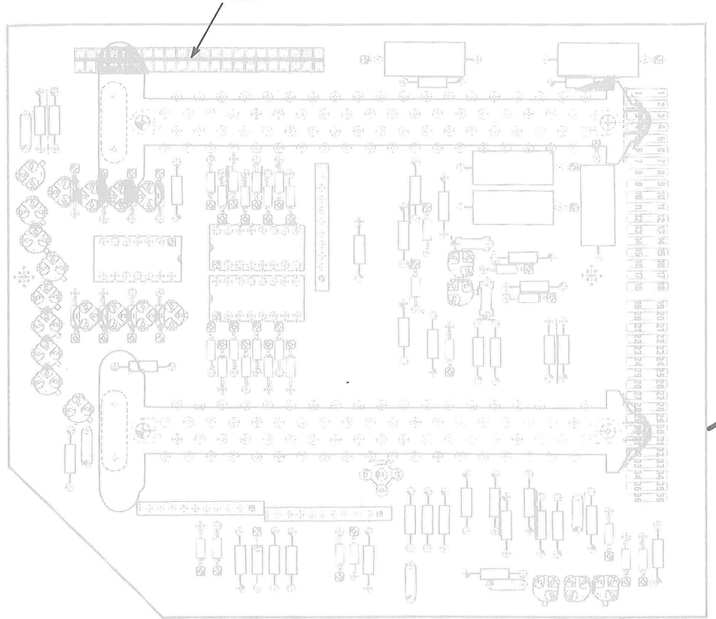
R255
-50 V



A82 CONTROL BOARD

R521
-5.2 V

J100



A46 PLUG-IN INTERFACE BOARD

A88 and A82 are located in the L. V. Power Supply—adjustments can be reached through holes in the bottom panel of L. V. Power Supply.

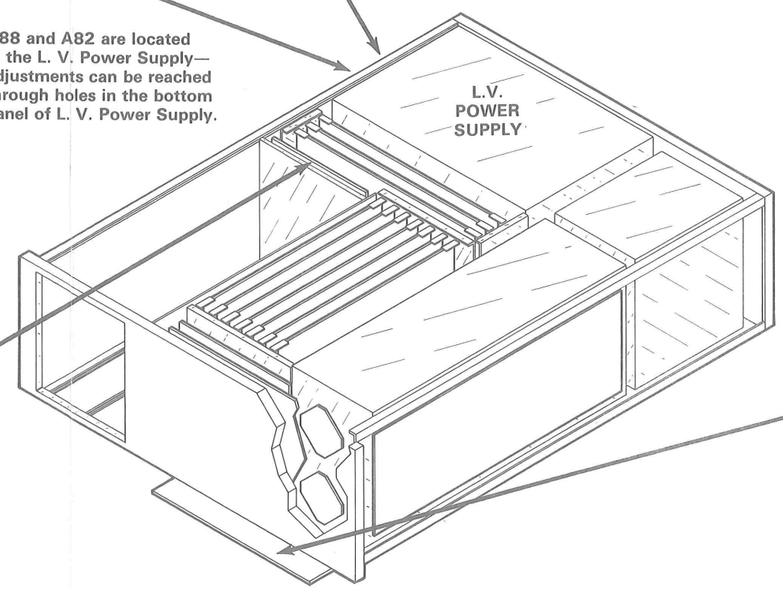
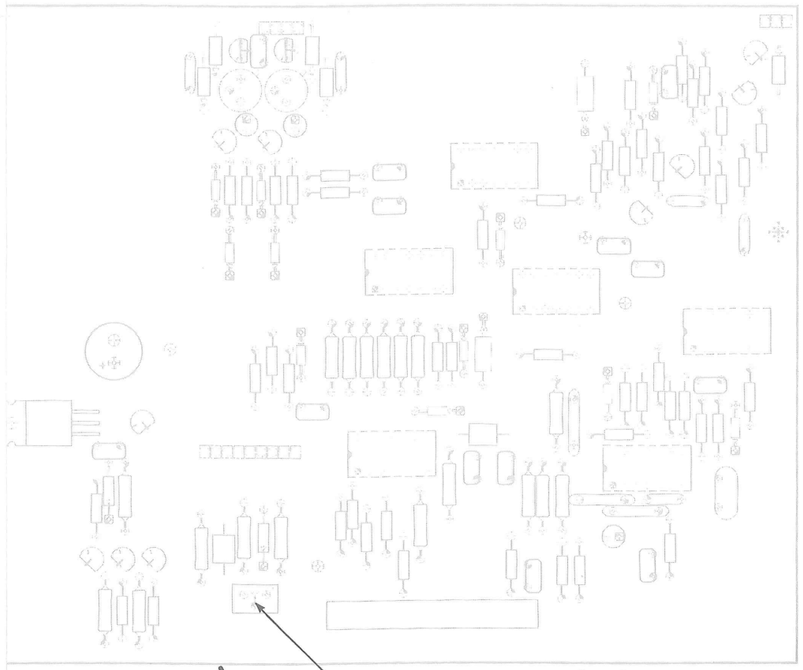


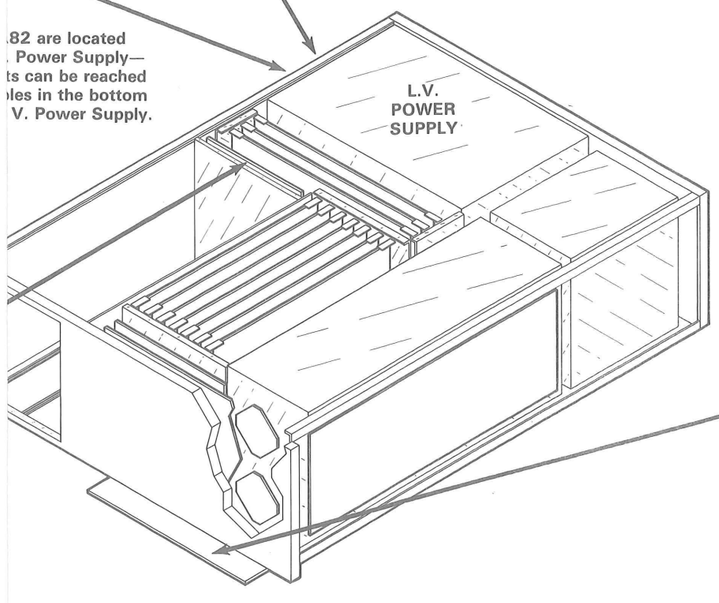
Fig 8-33. Test Point and Adjustment Locations A.

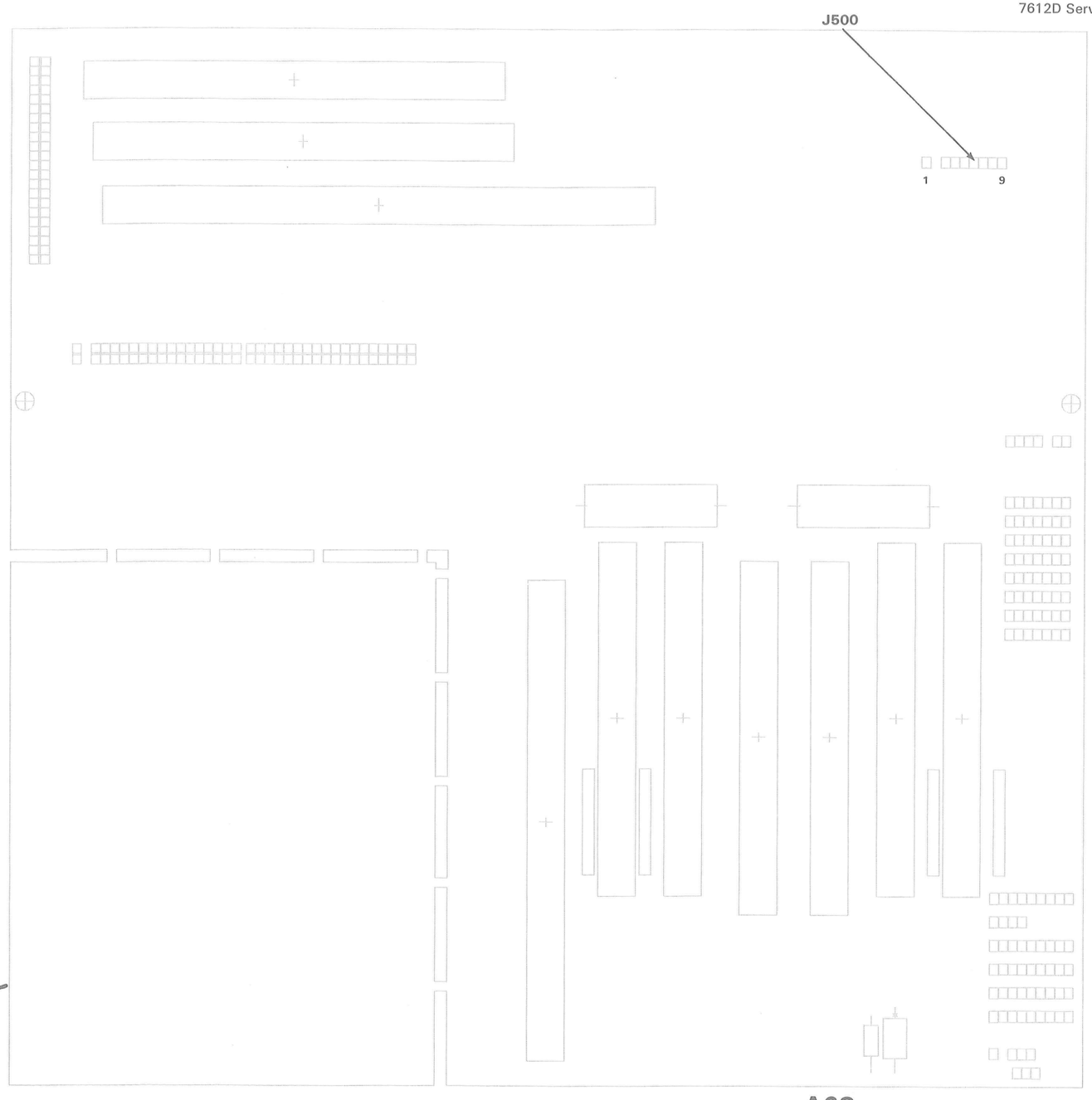


A82 CONTROL BOARD

R521
-5.2 V

.82 are located
. Power Supply—
ts can be reached
les in the bottom
V. Power Supply.





A68 MAIN INTERCONNECT BOARD

2387-853

Fig 8-33. Test Point and Adjustment Locations A.

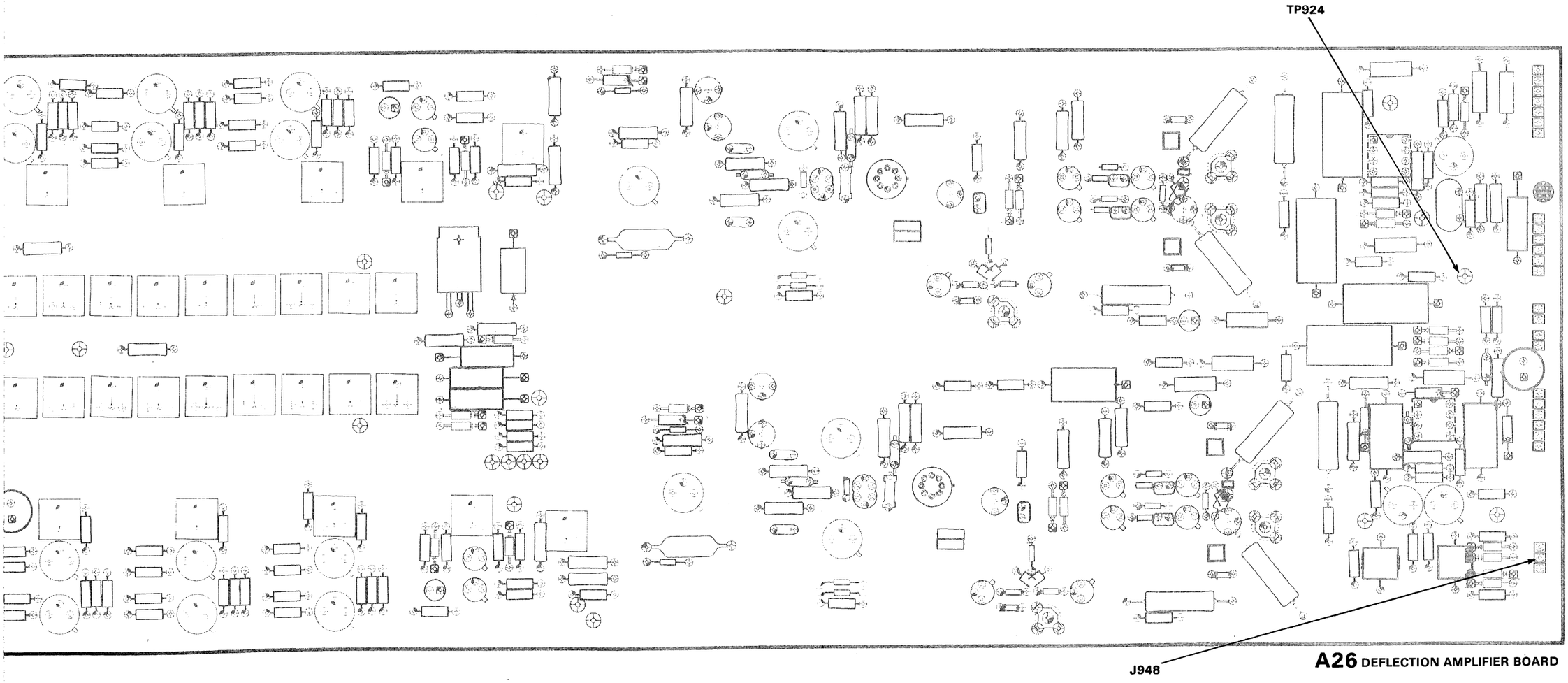
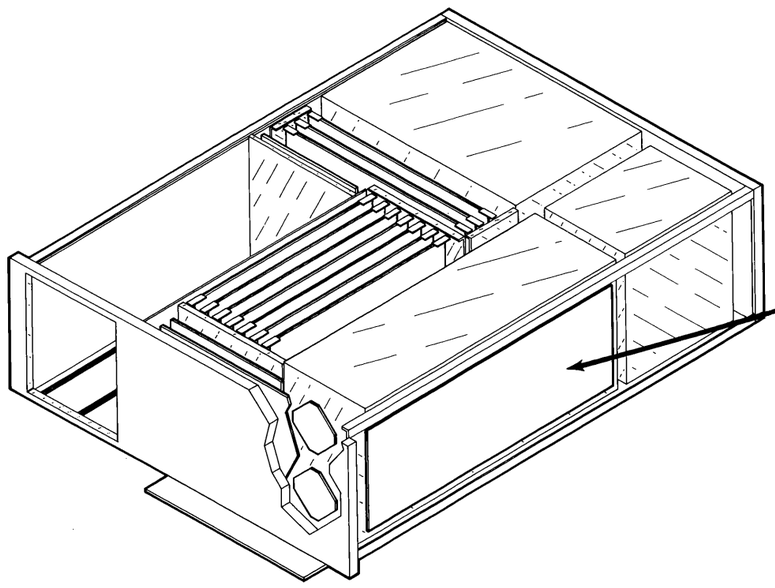


Fig 8-34. Test Point and Adjustment Locations B.



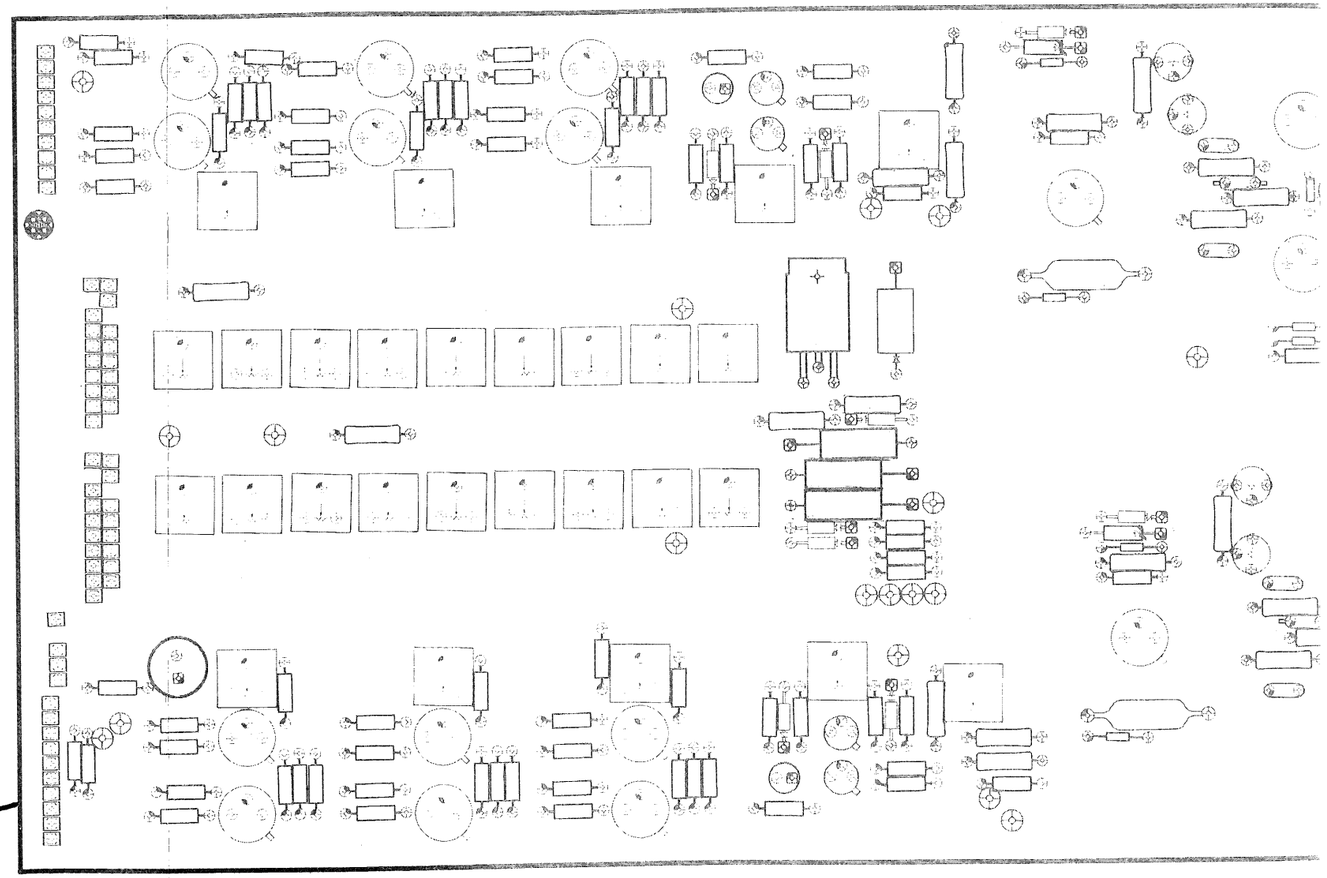
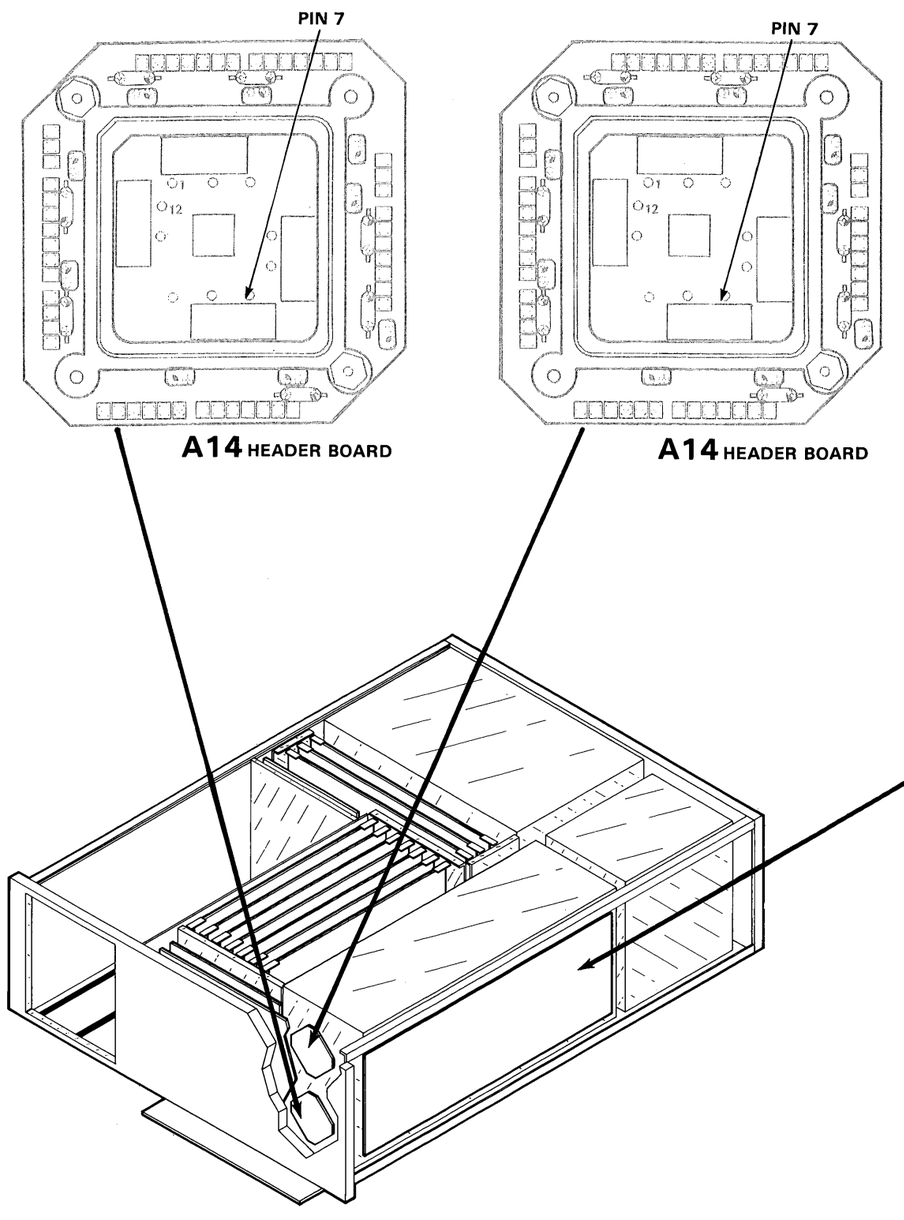


Fig 8-34. Test Point and Adjustment Locations B.



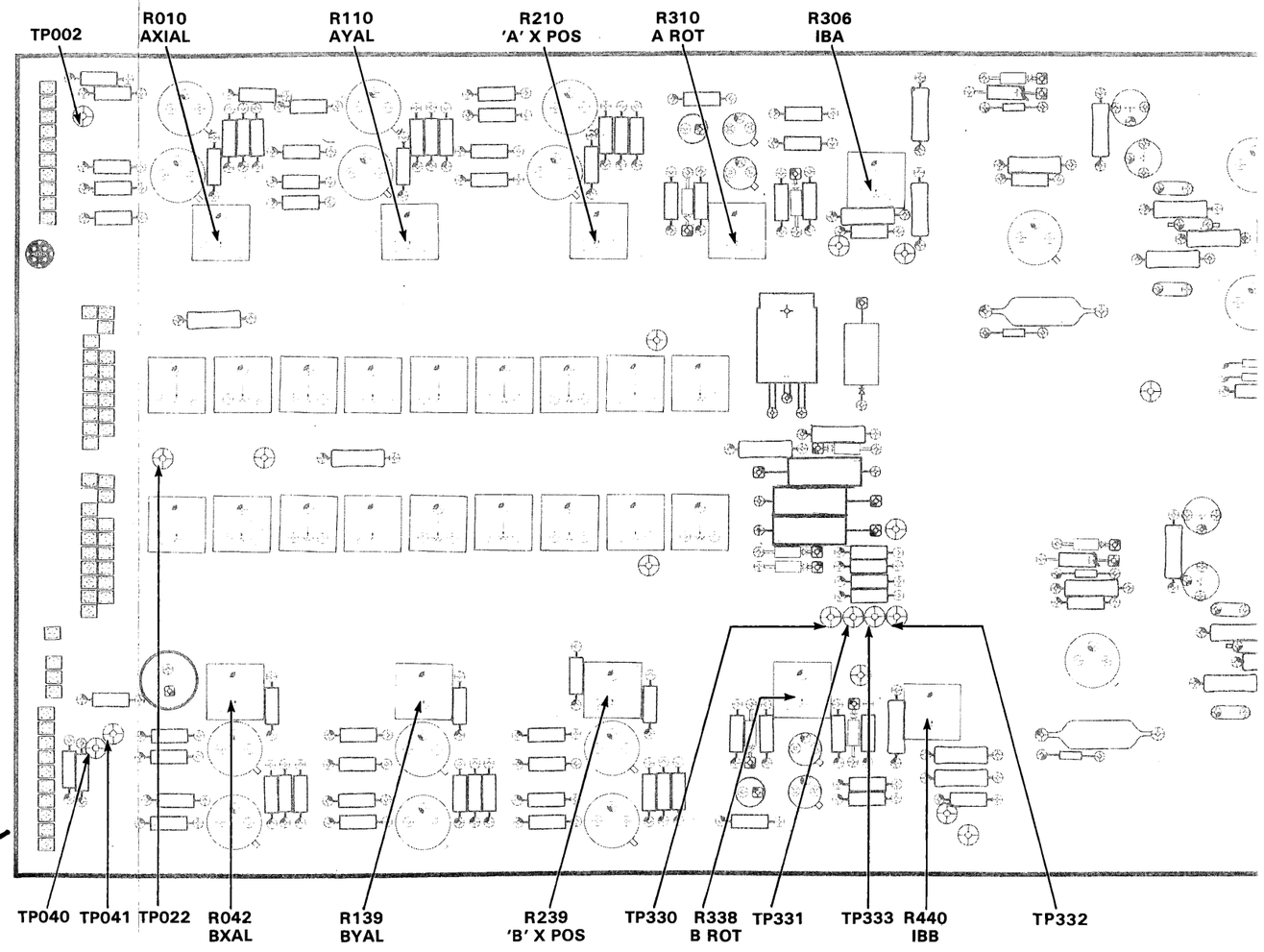


Fig 8-35. Test Point and Adjustment Locations C.

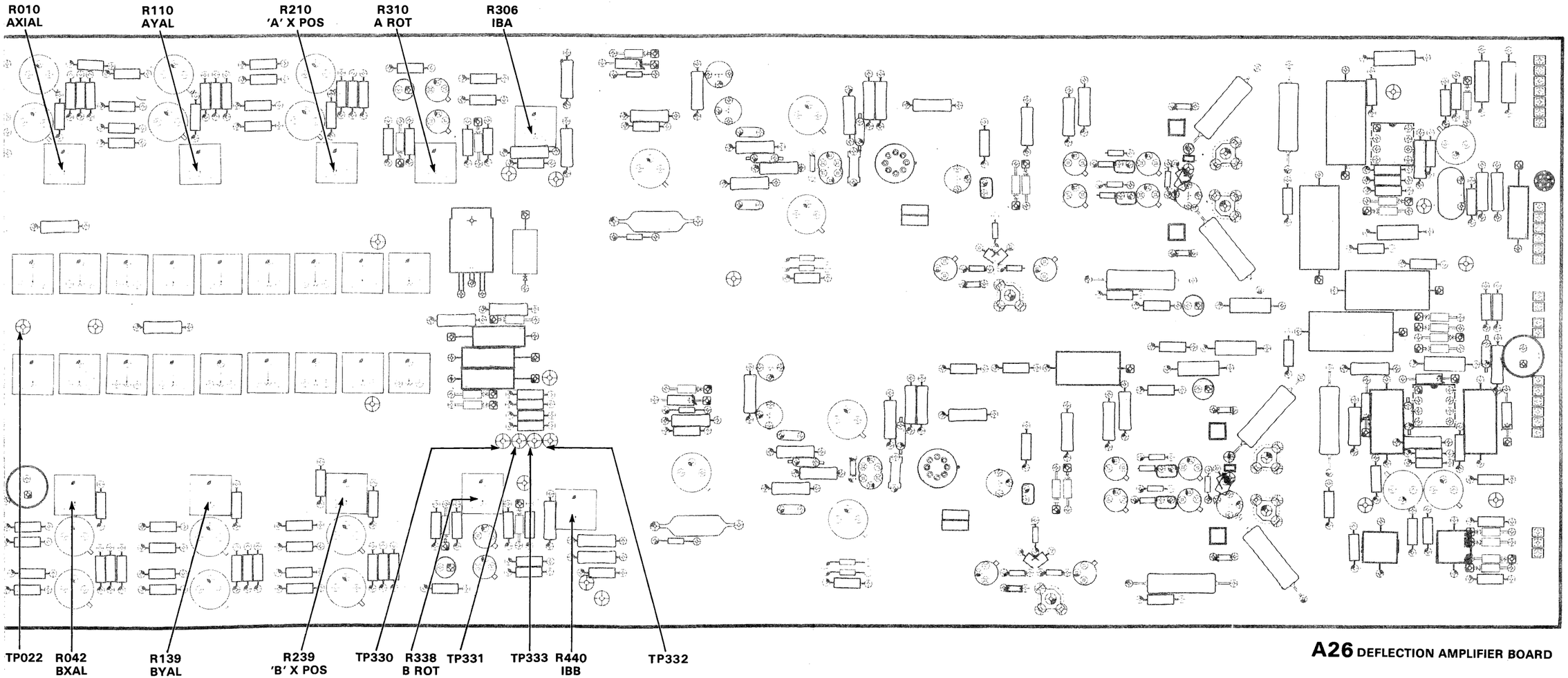
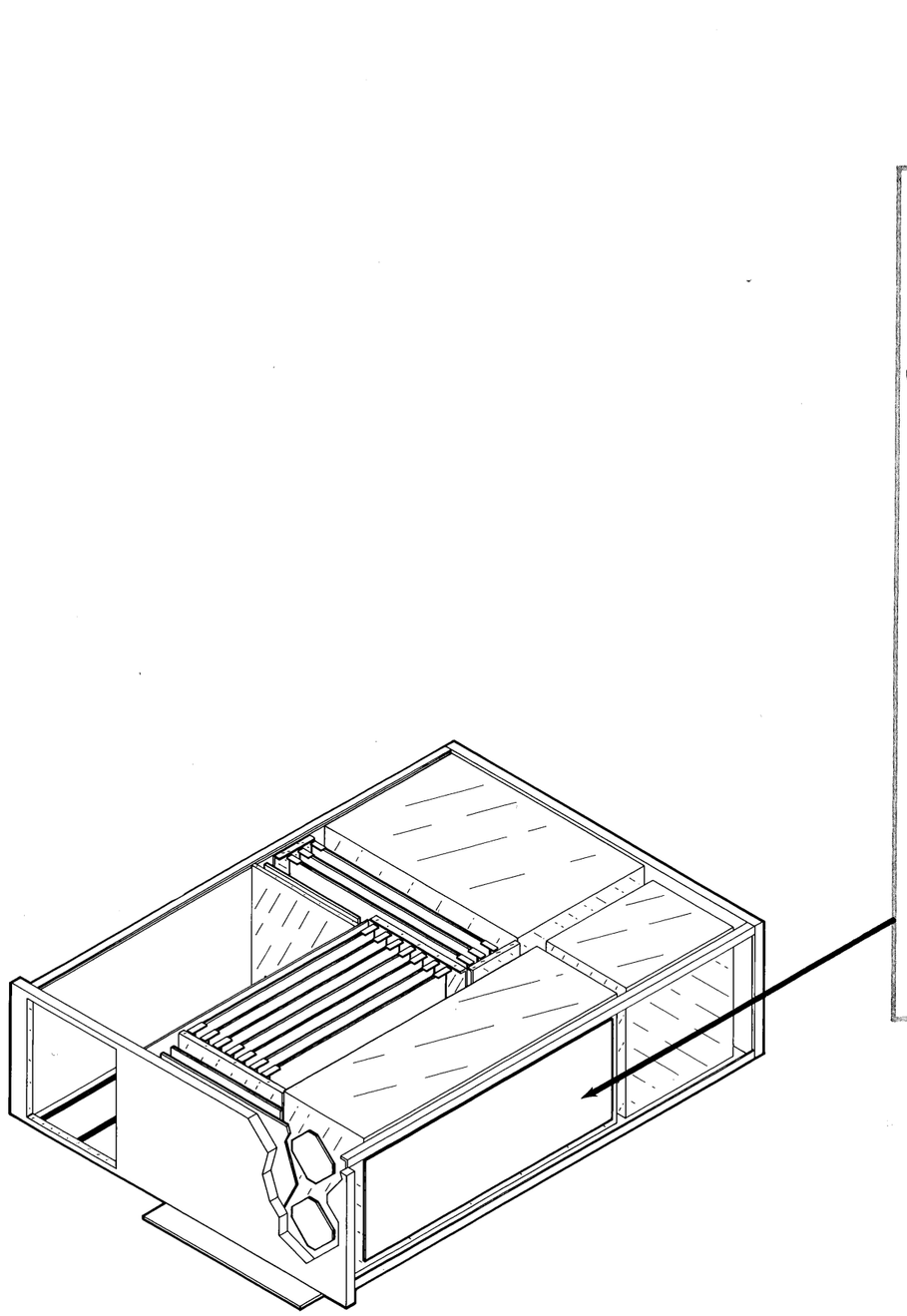


Fig 8-35. Test Point and Adjustment Locations C.



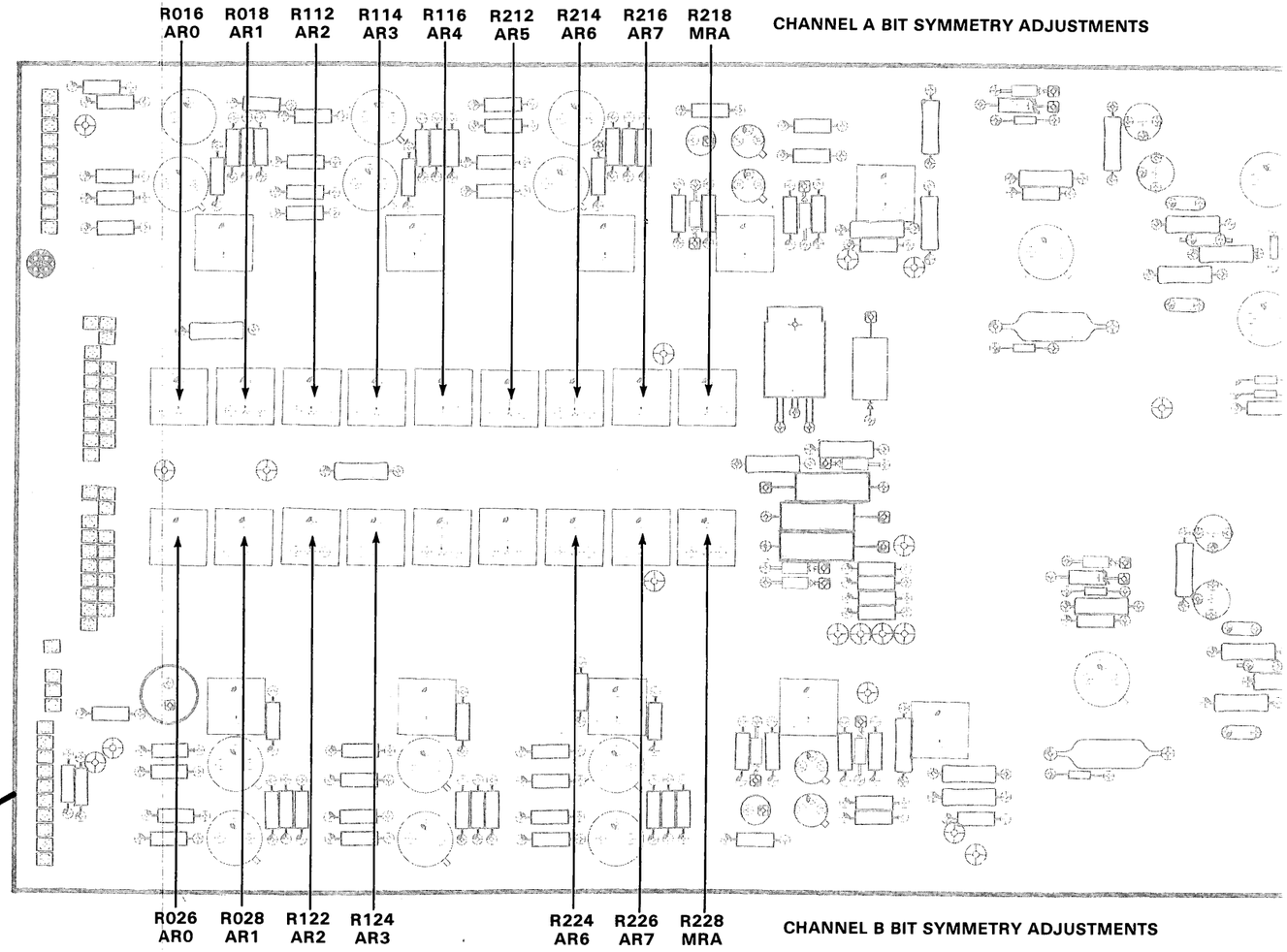


Fig 8-36. Test Point and Adjustment Locations D.

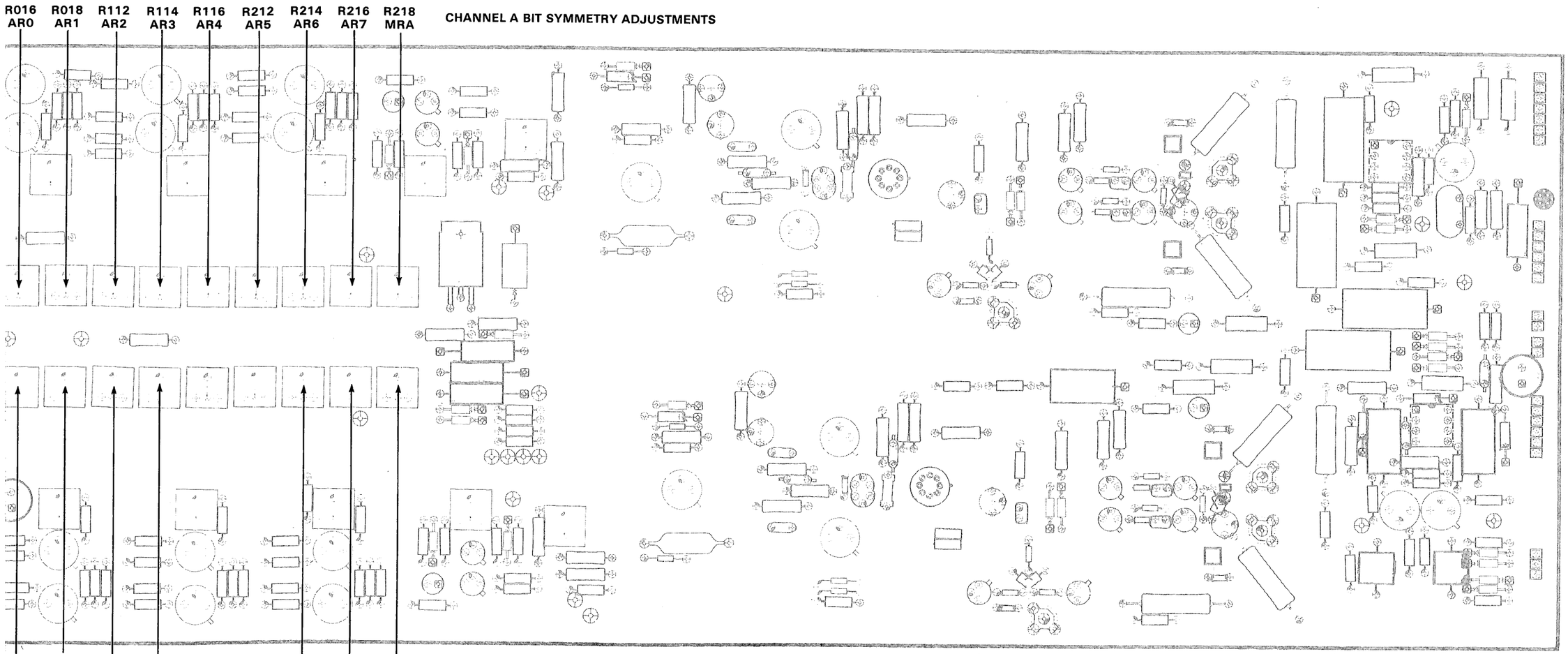
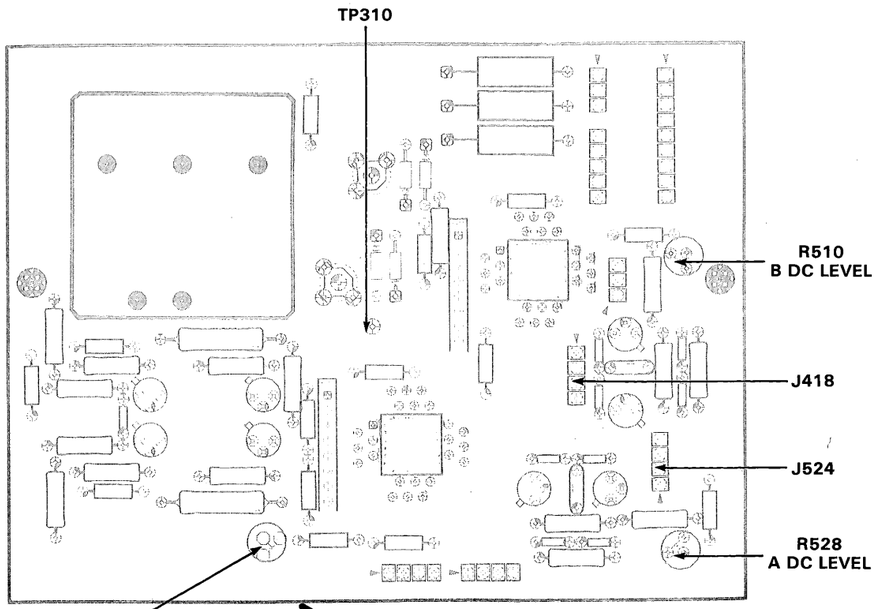
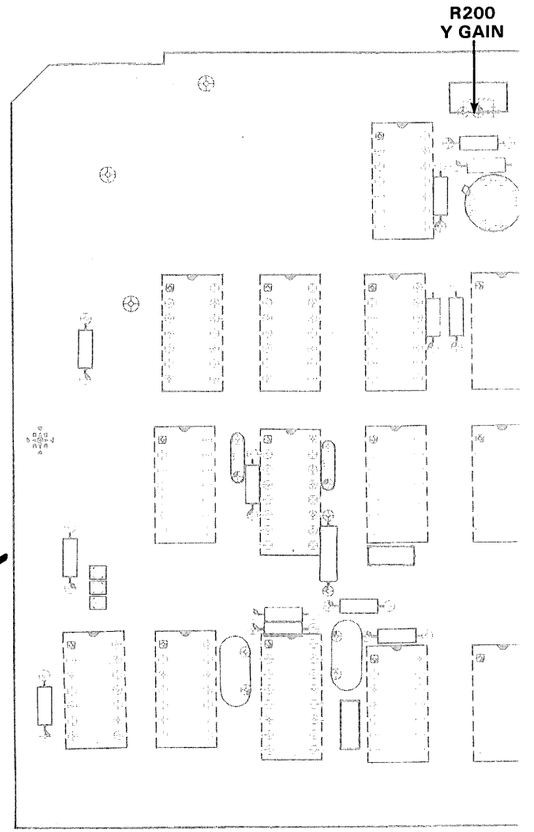


Fig 8-36. Test Point and Adjustment Locations D.





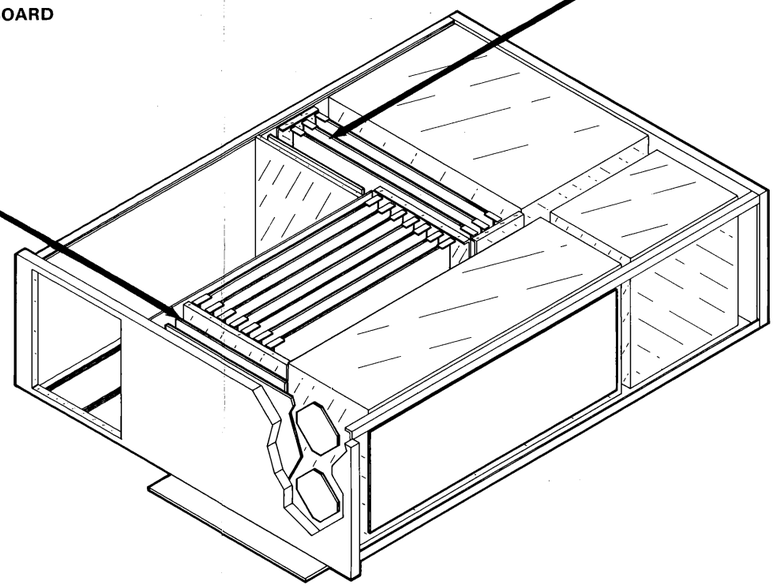


Fig 8-37. Test Point and Adjustment Locations E and F.

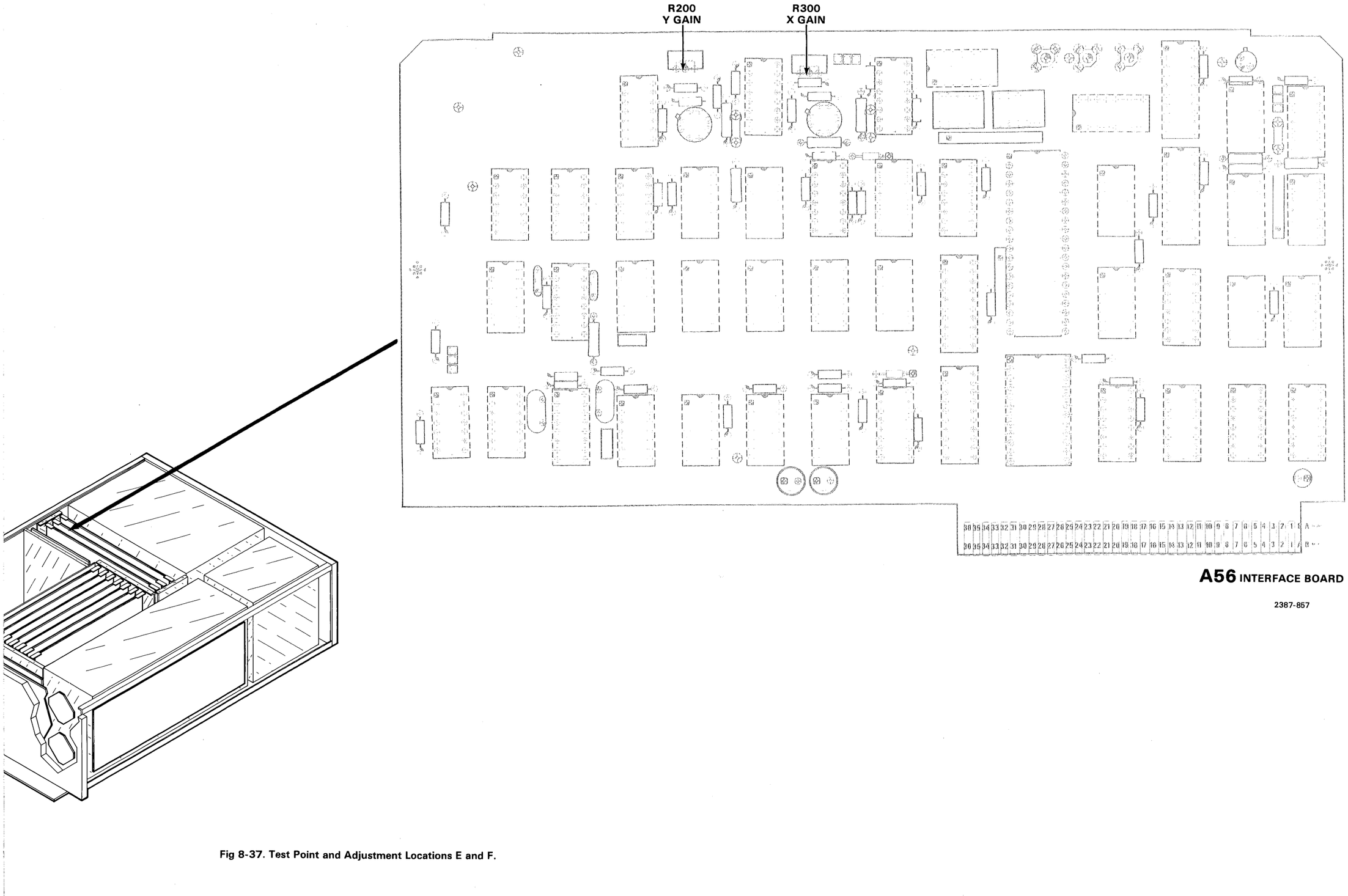
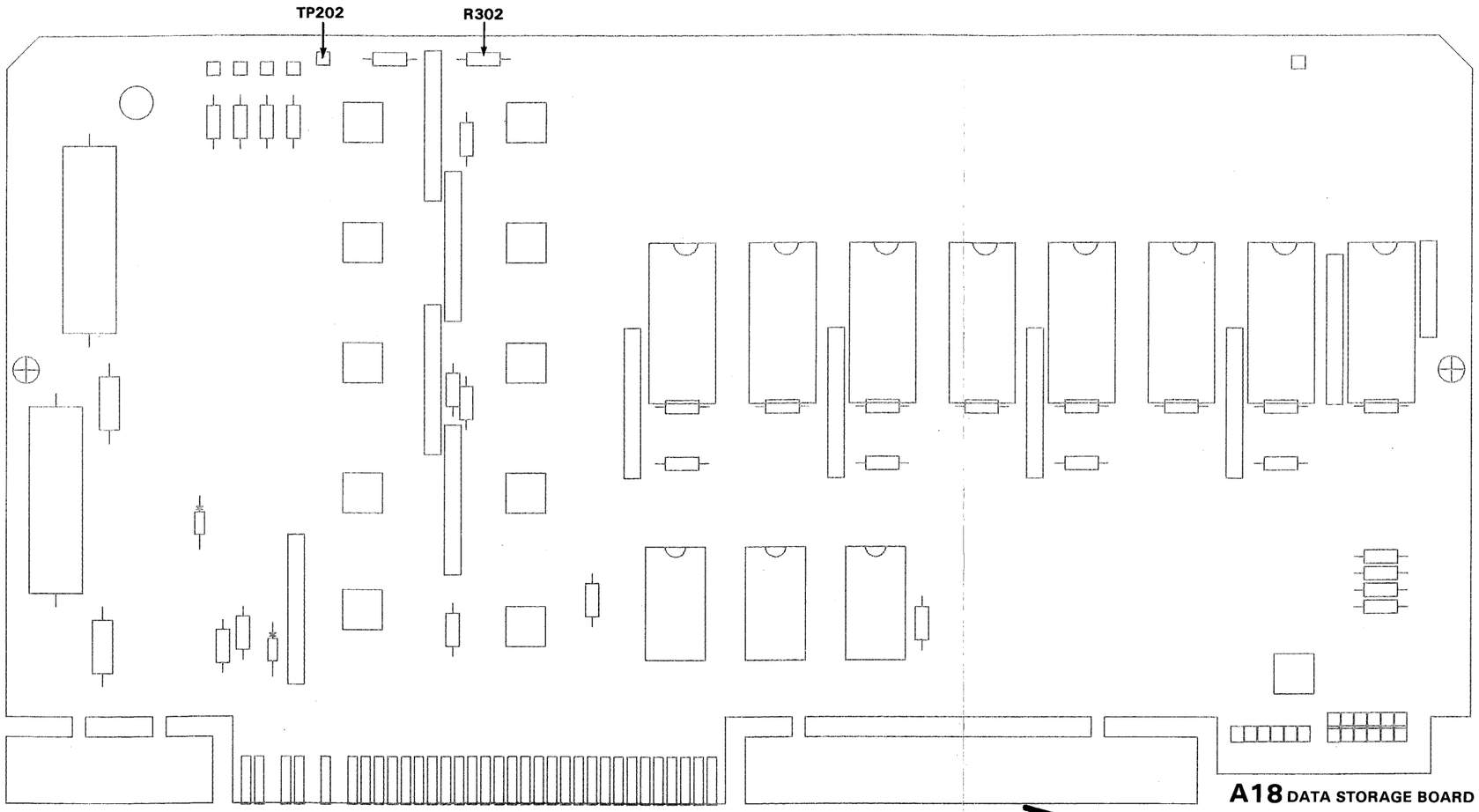
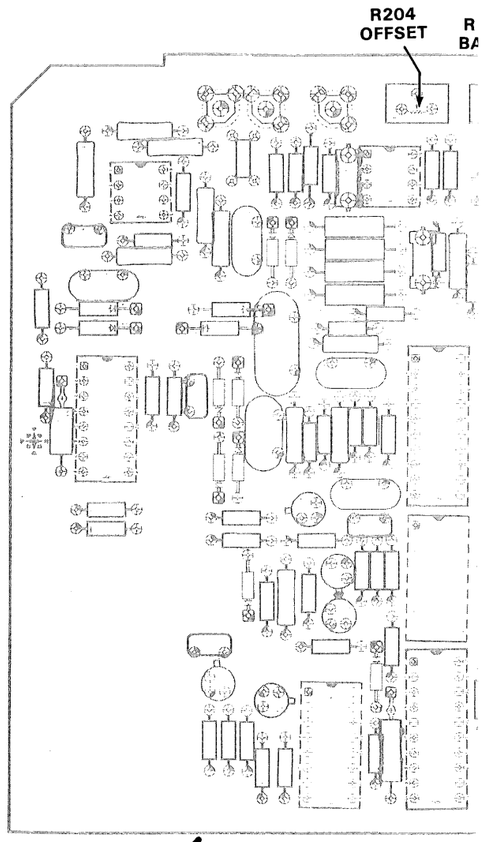


Fig 8-37. Test Point and Adjustment Locations E and F.



A18 DATA STORAGE BOARD



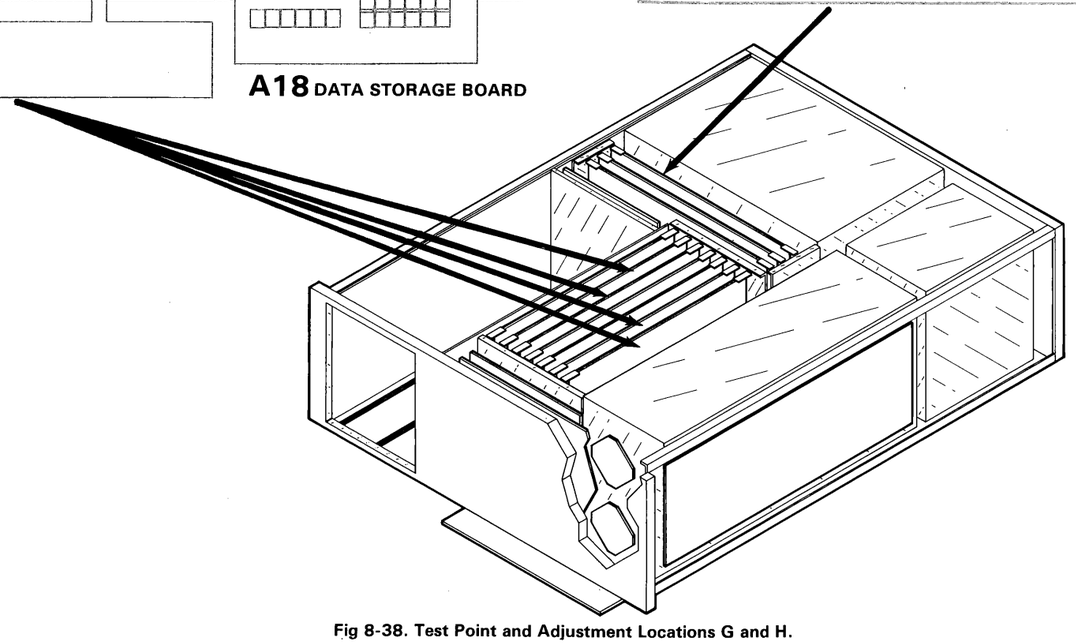
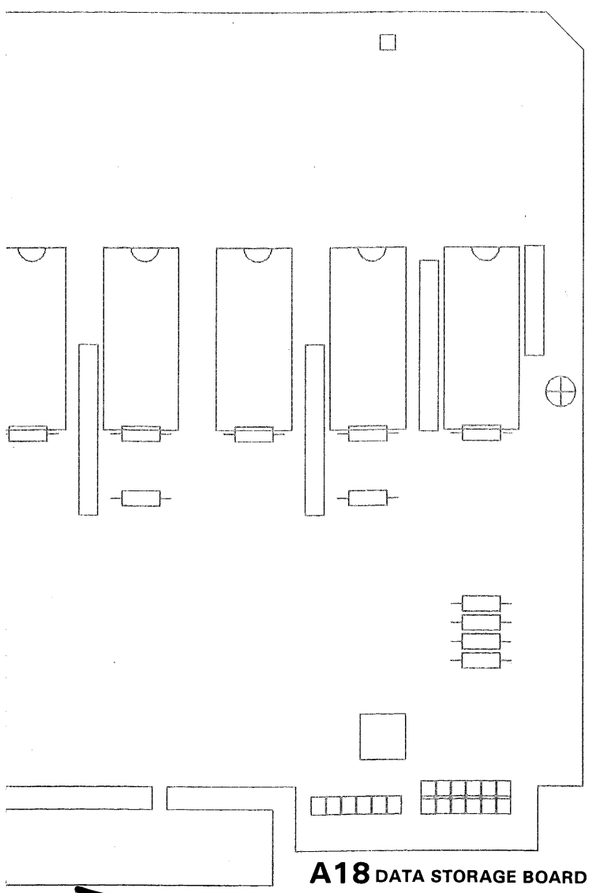
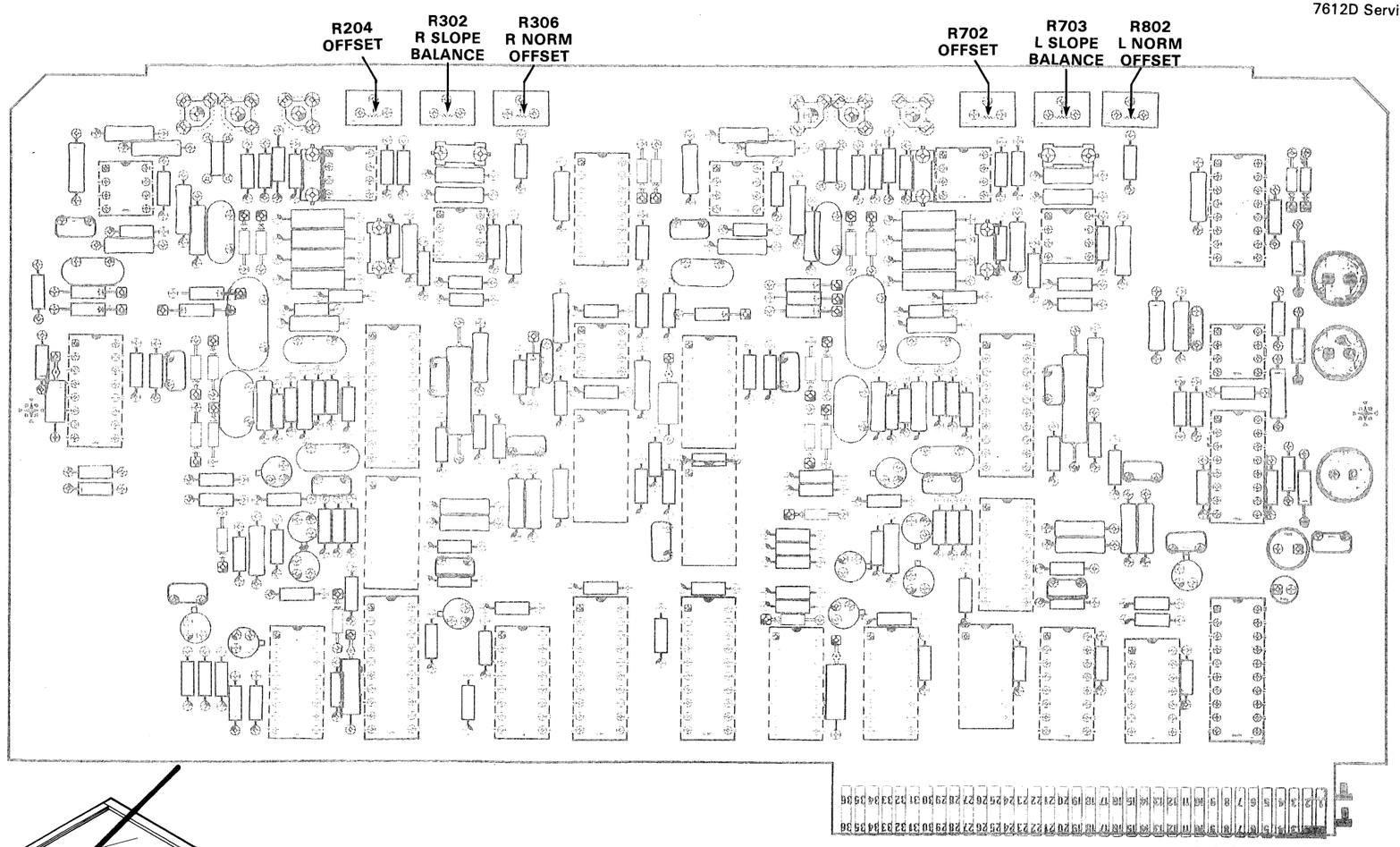


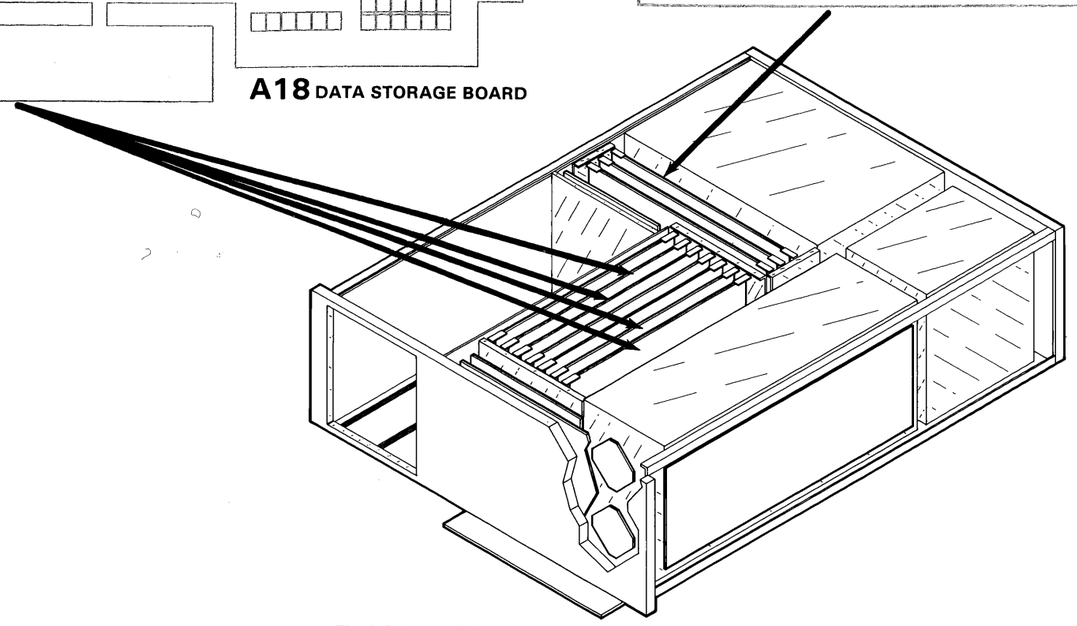
Fig 8-38. Test Point and Adjustment Locations G and H.



A18 DATA STORAGE BOARD

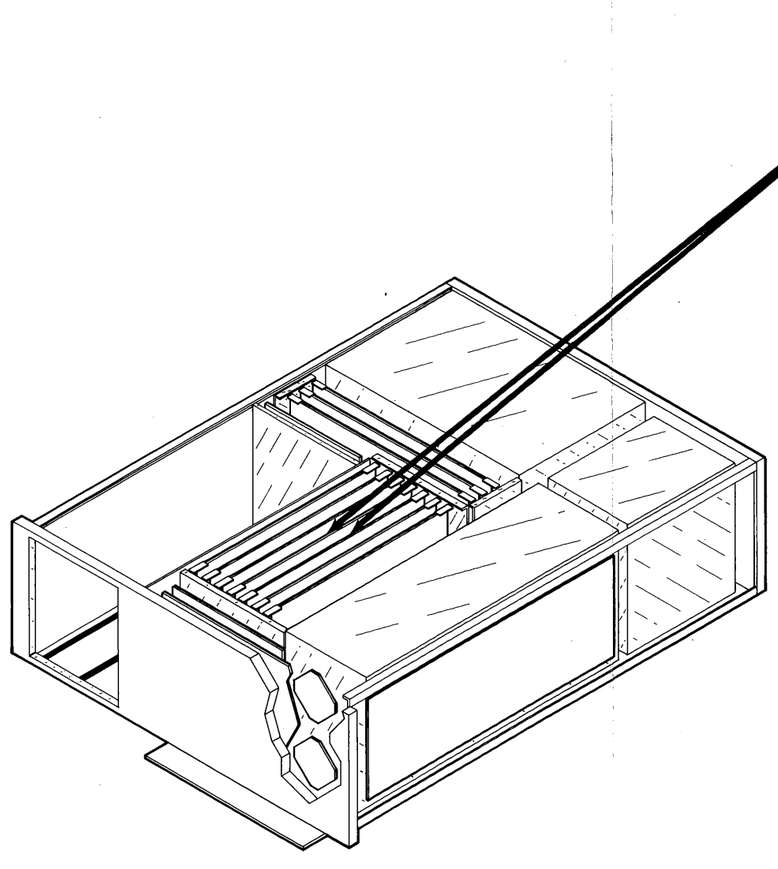


A62 TRIGGER BOARD



2387-858

Fig 8-38. Test Point and Adjustment Locations G and H.



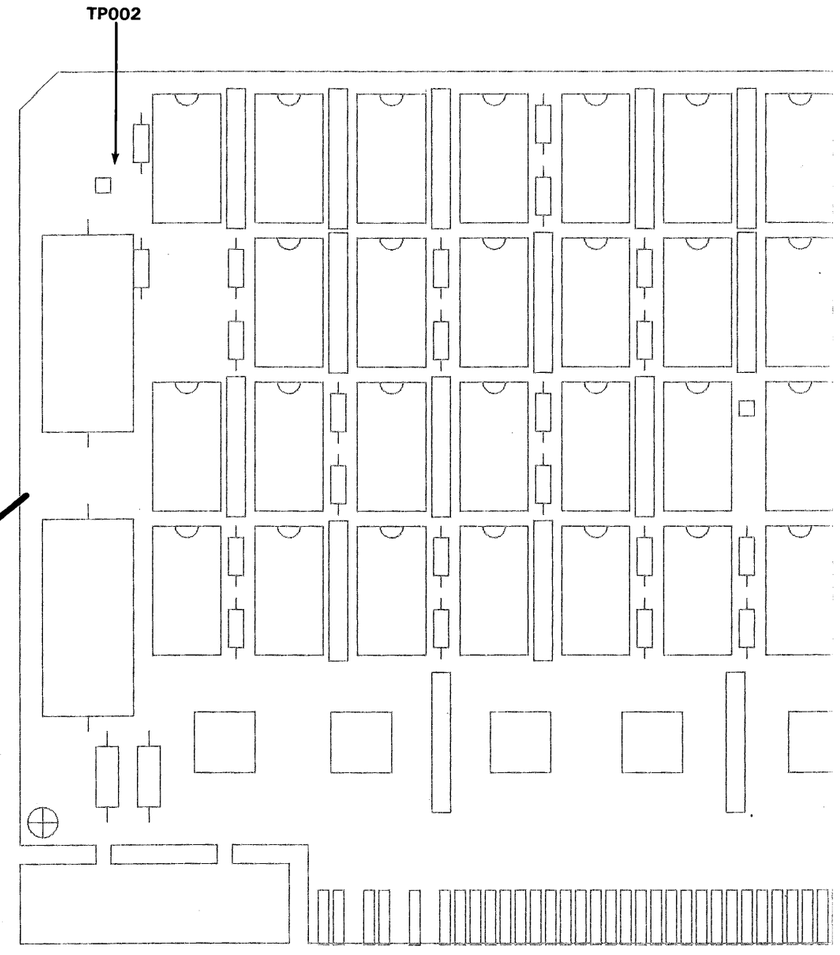


Fig 8-39. Test Point Location I.

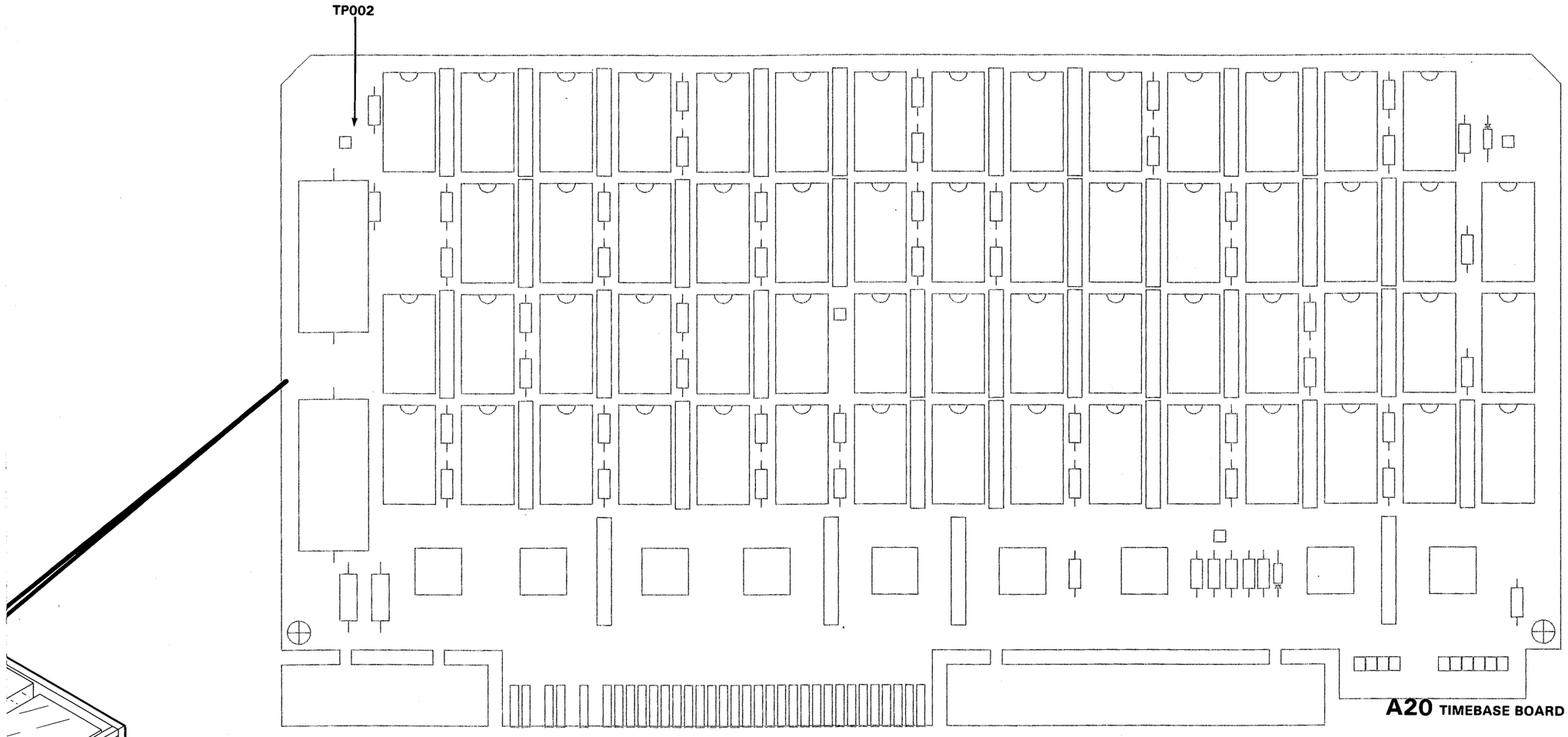
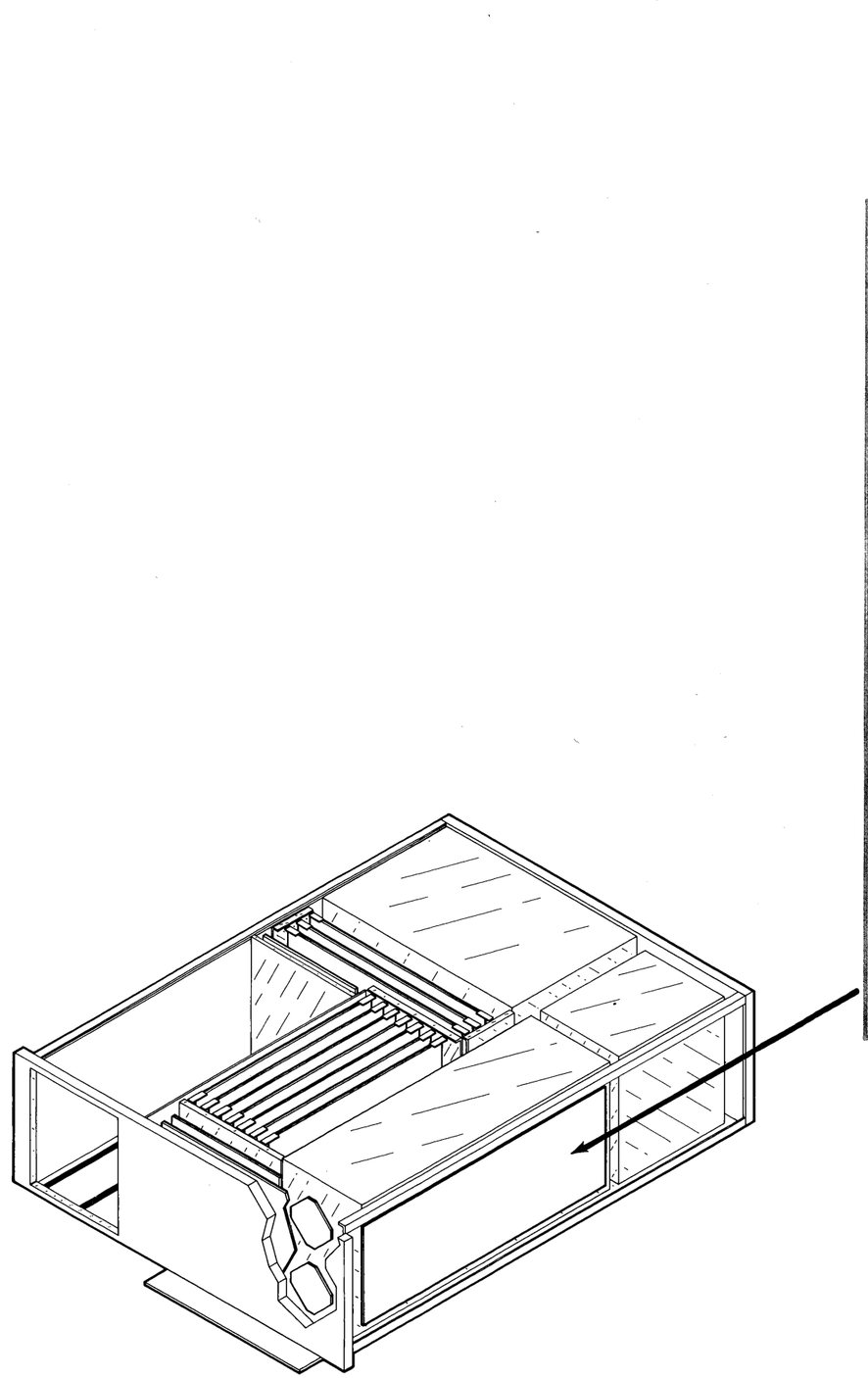


Fig 8-39. Test Point Location I.



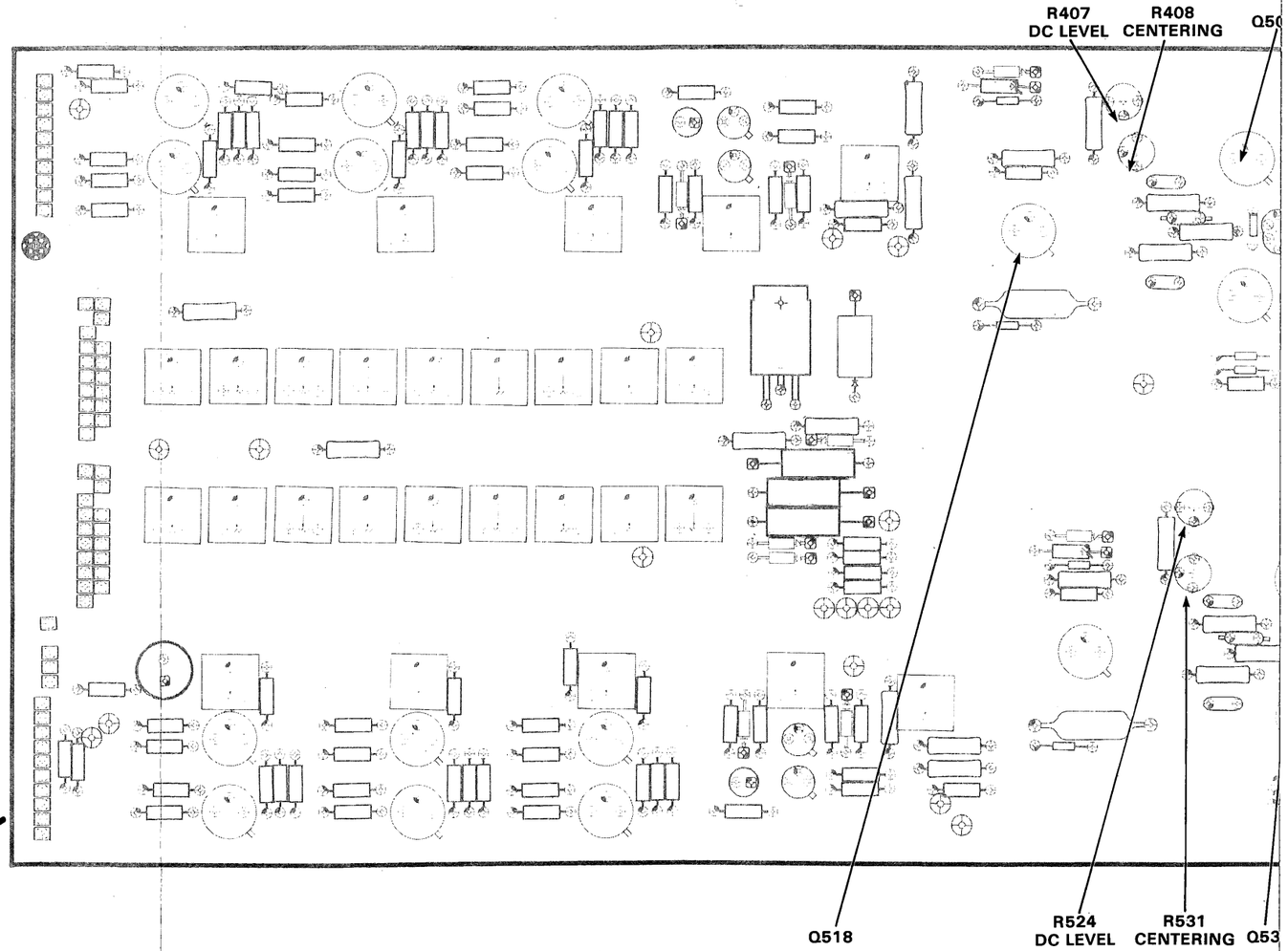


Fig 8-40. Test Point and Adjustment Locations K.

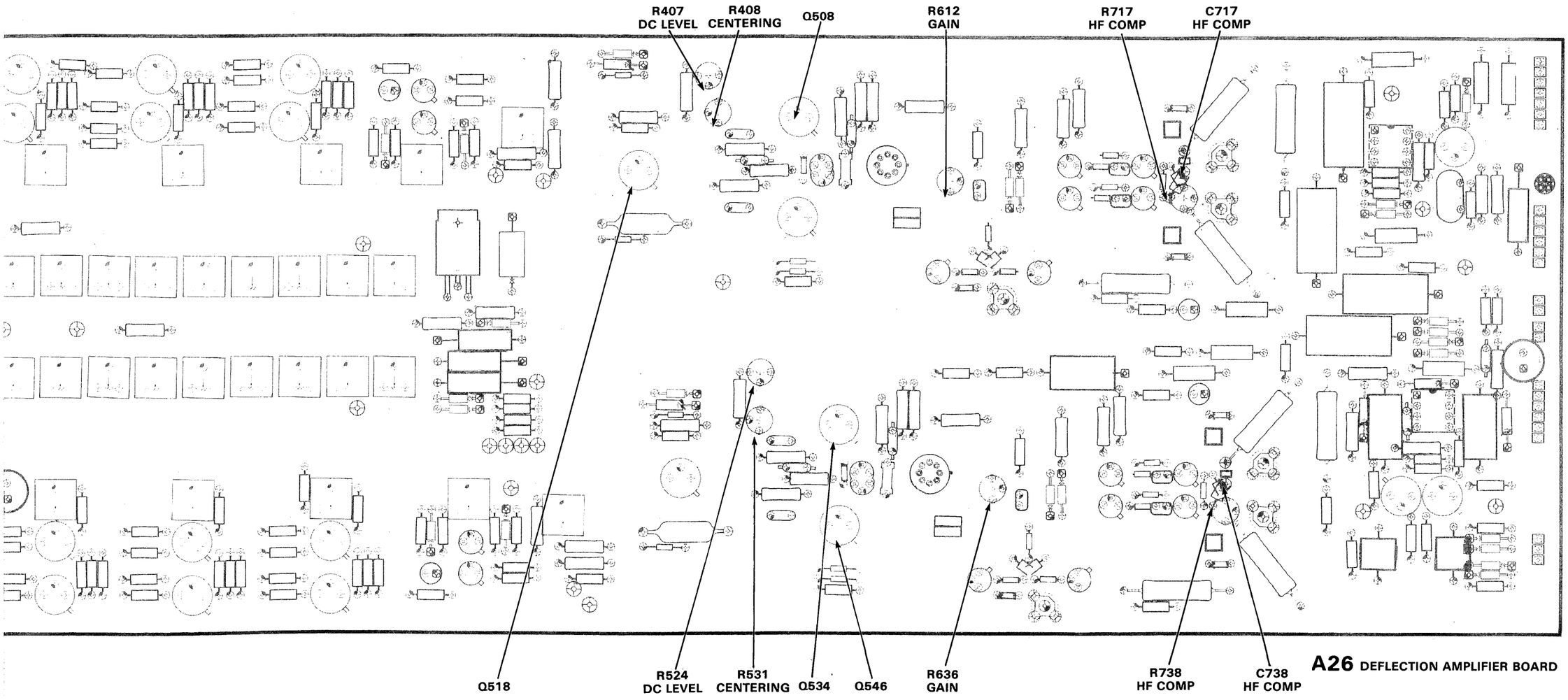


Fig 8-40. Test Point and Adjustment Locations K.

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

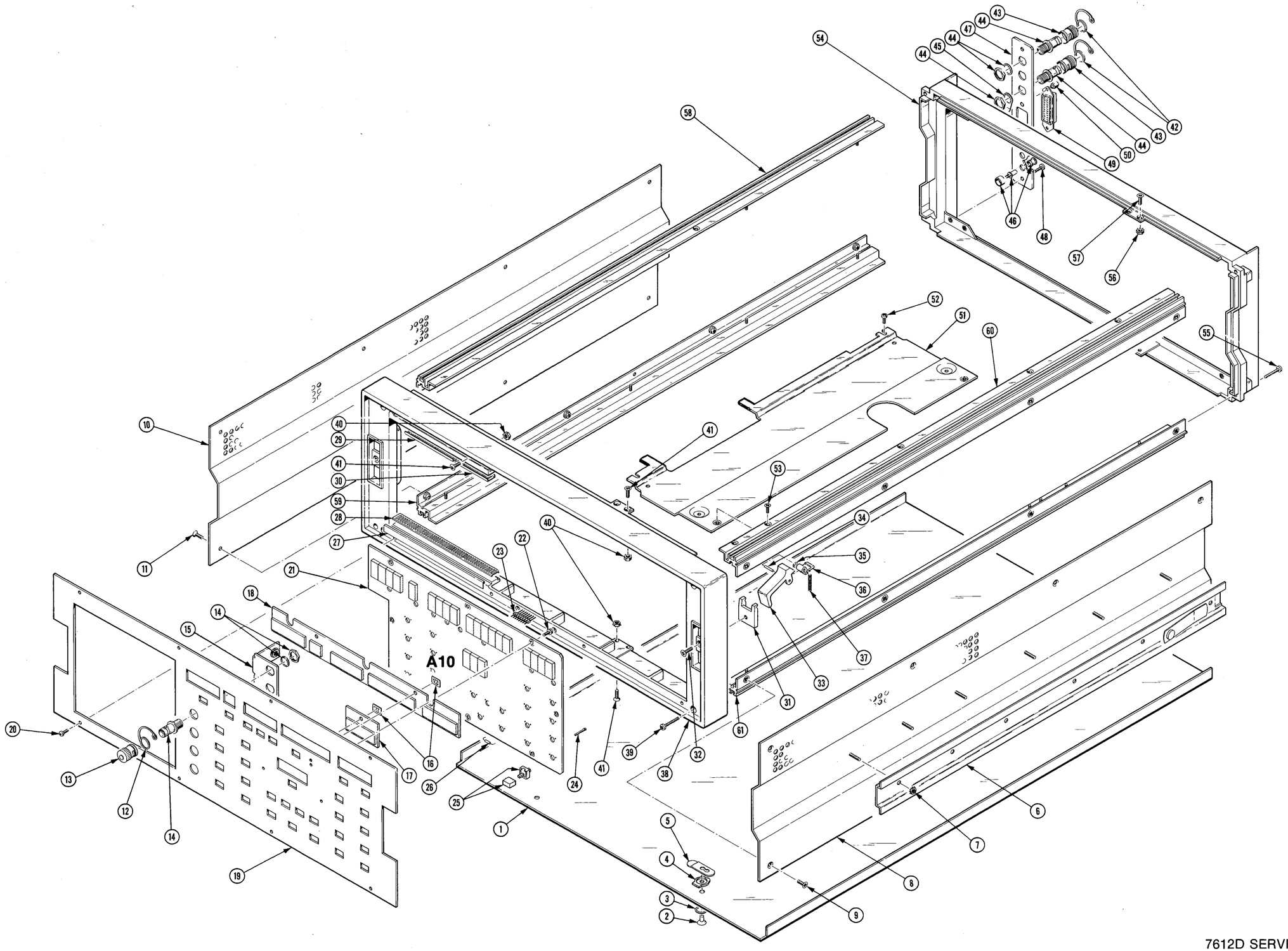
"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
000BB	BERQUIST COMPANY	4350 WEST 78TH	MINNEAPOLIS, MN 55435
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
000CX	N W SPRING AND MANUFACTURING COMPANY	5525 ROSEWOOD STREET	LAKE OSWEGO, OR 97034
000EL	PORTLAND SCREW CO.	6520 N. BASIN AVE.	PORTLAND, OR 97217
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04963	MINNESOTA MINING AND MFG. CO., ADHESIVES COATINGS AND SEALERS DIVISION	3M CENTER	ST. PAUL, MN 55101
06666	GENERAL DEVICES CO., INC.	525 S. WEBSTER AVE.	INDIANAPOLIS, IN 46219
08261	SPECTRA-STRIP CORP.	7100 LAMPSON AVE.	GARDEN GROVE, CA 92642
08530	RELIANCE MICA CORP.	342-39TH ST.	BROOKLYN, NY 11232
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
11897	PLASTIGLIDE MFG. CORPORATION	P O BOX 867, 1757 STANFORD ST.	SANTA MONICA, CA 90406
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
13103	THERMALLOY COMPANY, INC.	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS, TX 75234
16428	BELDEN CORP.	P. O. BOX 1331	RICHMOND, IN 47374
18677	SCANBE MFG. CORP.	3445 FLETCHER AVE.	EL MONTE, CA 91731
18722	RCA CORP., SOLID STATE DIVISION	CRESTWOOD ROAD YOUK EXPRESSWAY	MOUNTAINTOP, PA 18707 NEW CUMBERLAND, PA 17070
22526	BERG ELECTRONICS, INC.	30 LORRAINE AVE.	MT VERNON, NY 10553
23050	PRODUCT COMPONENTS CORP	2620 ENDRESS PLACE	GREENWOOD, IN 46142
24931	SPECIALITY CONNECTOR CO., INC.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
27264	MOLEX PRODUCTS CO.	30 ROCKEFELLER PLAZA	NEW YORK, NY 10020
49671	RCA CORPORATION	571 W. POLK ST.	CHICAGO, IL 60607
70485	ATLANTIC INDIA RUBBER WORKS, INC.	445 CONCORD AVE.	CAMBRIDGE. MA 02138
71279	CAMBRIDGE THERMIONIC CORP.	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
71785	TRW, CINCH CONNECTORS	446 MORGAN ST.	CINCINNATI, OH 45206
73743	FISCHER SPECIAL MFG. CO.	34 FOREST STREET	ATTLEBORO, MA 02703
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	33 E. FRANKLIN ST.	DANBURY, CT 06810
74868	BUNKER-RAMO CORP., THE AMPHENOL RF DIV.	4001 BENEFIT AVE., P O BOX 9	ASHTABULA, OH 44004
74921	ITEN FIBRE CO.,	S. MAIN ST.	CRYSTAL LAKE, IL 60014
76854	OAK INDUSTRIES, INC., SWITCH DIV.	ST. CHARLES ROAD	ELGIN, IL 60120
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	900 INDUSTRIAL RD.	SAN CARLOS, CA 94070
78471	TILLEY MFG. CO.	2100 S. O BAY ST.	MILWAUKEE, WI 53207
79807	WROUGHT WASHER MFG. CO.	P O BOX 500	BEAVERTON, OR 97077
80009	TEKTRONIX. INC.	P O BOX 287	MILFORD, IL 60953
81041	HOWARD INDUSTRIES, DIVISION OF MSL INDUSTRIES, INC.	2530 CRESCENT DR.	BROADVIEW, IL 60153
83385	CENTRAL SCREW CO.	123 N. RACINE	CHICAGO, IL 60607
83907	ACCURATE RUBBER PRODUCTS CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
85471	BOYD, A. B., CO.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
86445	PENN FIBRE AND SPECIALTY CO., INC.	701 SONORA AVENUE	GLENDALE, CA 91201
86928	SEASTROM MFG. COMPANY, INC.	40 MARBLEDALE ROAD	TUCKAHOE, NY 10707
91836	KINGS ELECTRONICS CO., INC.	600 18TH AVE	ROCKFORD, IL 61101
93907	TEXTRON INC. CAMCAR DIV	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
95987	WECKESSER CO., INC.		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	200-2092-00			2		COVER,ACCESS:ALUMINUM	80009	200-2092-00
-2	214-0603-02			6		. PIN ASSY,SECRG:	80009	214-0603-02
-3	214-0604-00			6		. . WASH.,SPG TNSN:0.26 ID X 0.47 INCH OD	80009	214-0604-00
-4	386-0227-01			6		. STOP,CLP,RIM CL:BLACK ACETAL	80009	386-0227-01
-5	386-1151-00			6		. CLAMP,RIM CLENC:SPG STL CD PL	80009	386-1151-00
-6	351-0313-00			1		GUIDE,RACKMOUNT:19.218 INCH LONG,PAIR	06666	OBD
						(ATTACHING PARTS)		
-7	210-0458-00			12		NUT,PL,ASSEM WA:8-32 X 0.344 INCH,STL	83385	OBD
						- - - * - - -		
-8	390-0572-00			1		CABINET,SIDE:RIGHT	80009	390-0572-00
						(ATTACHING PARTS)		
-9	211-0538-00			8		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-10	390-0573-00			1		CABINET,SIDE:LEFT	80009	390-0573-00
						(ATTACHING PARTS)		
-11	211-0538-00			8		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-12	346-0045-00			4		STRAP,CONN COV:BNC ONE END,POLYPROPYLENE	80009	346-0045-00
-13	200-0678-00			4		COVER,ELEC CONN:BNC,SHORTING	91836	KC89-58TR5
-14	131-1315-01			4		CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR 306-1
-15	407-1982-00			1		BRACKET,CONN:ALUMINUM	80009	407-1982-00
-16	210-0437-01			3		NUT,SHEET SPR:6-32,STL CD PL	86928	OBD
-17	378-0138-00			1		FLTR,LED,RDOUT:RED,1.71 L X 1.125 W,PLSTC	80009	378-0138-00
-18	378-0868-00			1		FLTR,LED,RDOUT:RED,9.81 L X 0.95 W,PLSTC	80009	378-0868-00
-19	333-2324-00	B010100	B035589	1		PANEL,FRONT:	80009	333-2324-00
	333-2324-01	B025590		1		PANEL,FRONT:	80009	333-2324-01
						(ATTACHING PARTS)		
-20	213-0794-01			8		SCREW,CAP:4-40,HEX SOC,STEEL	80009	213-0794-01
						- - - * - - -		
-21	----- -----			1		CKT BOARD ASSY:FRONT PANEL(SEE A10 REPL)		
						(ATTACHING PARTS)		
-22	211-0116-00			8		SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-23	----- -----			2		. TERM SET,PIN:(SEE A10J548,J550,J552,		
	----- -----			-		. J554,J556 REPL)		
-24	----- -----			4		. TERM,TEST POINT:(SEE A10TP942,TP944,TP946,		
	----- -----			-		. TP948 REPL)		
-25	----- -----			32		. SWITCH,PB ASSY:(SEE A10S110,S214,S220,S230,		
	----- -----			-		. S240,S250,S314,S324,S334,S344,S354,S410,S416,		
	----- -----			-		. S446,S456,S518,S536,S544,S556,S640,S646,S656,		
	----- -----			-		. S814,S822,S832,S842,S852,S916,S926,S936,S946,		
	----- -----			-		. S956 REPL)		
-26	----- -----			1		. LINK,TERM CONNE:(SEE A10W544 REPL)		
-27	407-2021-00			2		BRACKET,ANGLE:EMI,ALUMINUM	80009	407-2021-00
-28	337-2453-00			1		SHIELD,ELEC:EMI	80009	337-2453-00
-29	337-1543-00			1		SHLD GSKT,ELECT:2.50 INCHES LONG	80009	337-1543-00
-30	337-1542-00			1		SHLD GSKT,ELECT:2.10 INCHES LONG	80009	337-1542-00
-31	343-0706-01			2		RETAINER,LATCH:W/SPRING & INSERT	80009	343-0706-01
						(ATTACHING PARTS)		
-32	212-0070-00			2		SCREW,MACHINE:8-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-33	367-0236-01			2		HANDLE,LATCH:1.925,ALUMINUM	80009	367-0236-01
						(ATTACHING PARTS)		
-34	214-2653-00			2		PIN,STR,HDLS:0.125 DIA X 0.875 L,SST	80009	214-2653-00
						- - - * - - -		
-35	210-1278-00			4		WASHER,SPR TNSN:0.128 ID X 0.003 THK	86928	5806-6-1
-36	105-0756-00			2		CATCH,LATCH:	80009	105-0756-00
-37	214-2654-00			2		SPRING,HLCPS:0.188 OD X 0.69 L,CLOSED END	000CX	OBD
-38	426-1421-01			1		FRAME PANEL,CAB:FRONT,FINISHED	80009	426-1421-01
						(ATTACHING PARTS)		
-39	213-0760-00			4		SCREW,TPG,TF:8-32 X 0.875,SPCL TAPTITE	93907	OBD
-40	210-0457-00			5		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-41	211-0538-00			5		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-42	346-0045-00			3		STRAP,CONN COV:BNC ONE END,POLYPROPYLENE	80009	346-0045-00
-43	200-0678-00			3		COVER,ELEC CONN:BNC,SHORTING	91836	KC89-58TR5
-44	131-1315-01			3		CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR 306-1
-45	210-0255-00			1		TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	80009	210-0255-00
-46	----- -----			2		LAMP,LED:(SEE DS5114,DS5115 REPL)		
-47	333-2600-00	B010100	B030457	1		PANEL,REAR:	80009	333-2600-00
	333-2600-01	B030458	B030668	1		PANEL,REAR:	80009	333-2600-01
	333-2600-02	B030669		1		PANEL,REAR:	80009	333-2600-02
						(ATTACHING PARTS)		
-48	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		FRONT PANEL INCLUDES:		
-49	----- -----			1		. CONNECTOR:(SEE J13 REPL)		
						(ATTACHING PARTS)		
-50	129-0572-00	B010100	B030457	2		. SPACER,POST:0.29 LONG X 0.25 HEX	80009	129-0572-00
	129-0922-00	B030458		2		. SPACER,POST:0.71,W/6-32 THD ONE END,AL	80009	129-0922-00
	210-0008-00	XB030458		2		. WASHER,LOCK:INTL,0.172 ID X 0.331"OD,STL	78189	1208-00-00-0541C
						- - - * - - -		
-51	386-3748-00			1		PLATE,SECURING:CRT,ALUMINUM	80009	386-3748-00
						(ATTACHING PARTS)		
-52	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-53	211-0538-00			2		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-54	426-1422-01			1		FRAME PANEL,CAB:REAR W/HARDWARE	80009	426-1422-01
						(ATTACHING PARTS)		
-55	213-0760-00			4		SCREW,TPG,TF:8-32 X 0.875,SPCL TAPTITE	93907	OBD
-56	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-57	211-0538-00			4		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-58	426-1426-00			1		FRAME SECT,CAB.:TOP LEFT	80009	426-1426-00
-59	426-1425-00			1		FRAME SECT,CAB.:BOTTOM LEFT	80009	426-1425-00
-60	426-1428-00			1		FRAME SECT,CAB.:TOP RIGHT	80009	426-1428-00
-61	426-1427-00			1		FRAME SECT,CAB.:BOTTOM RIGHT	80009	426-1427-00


A10

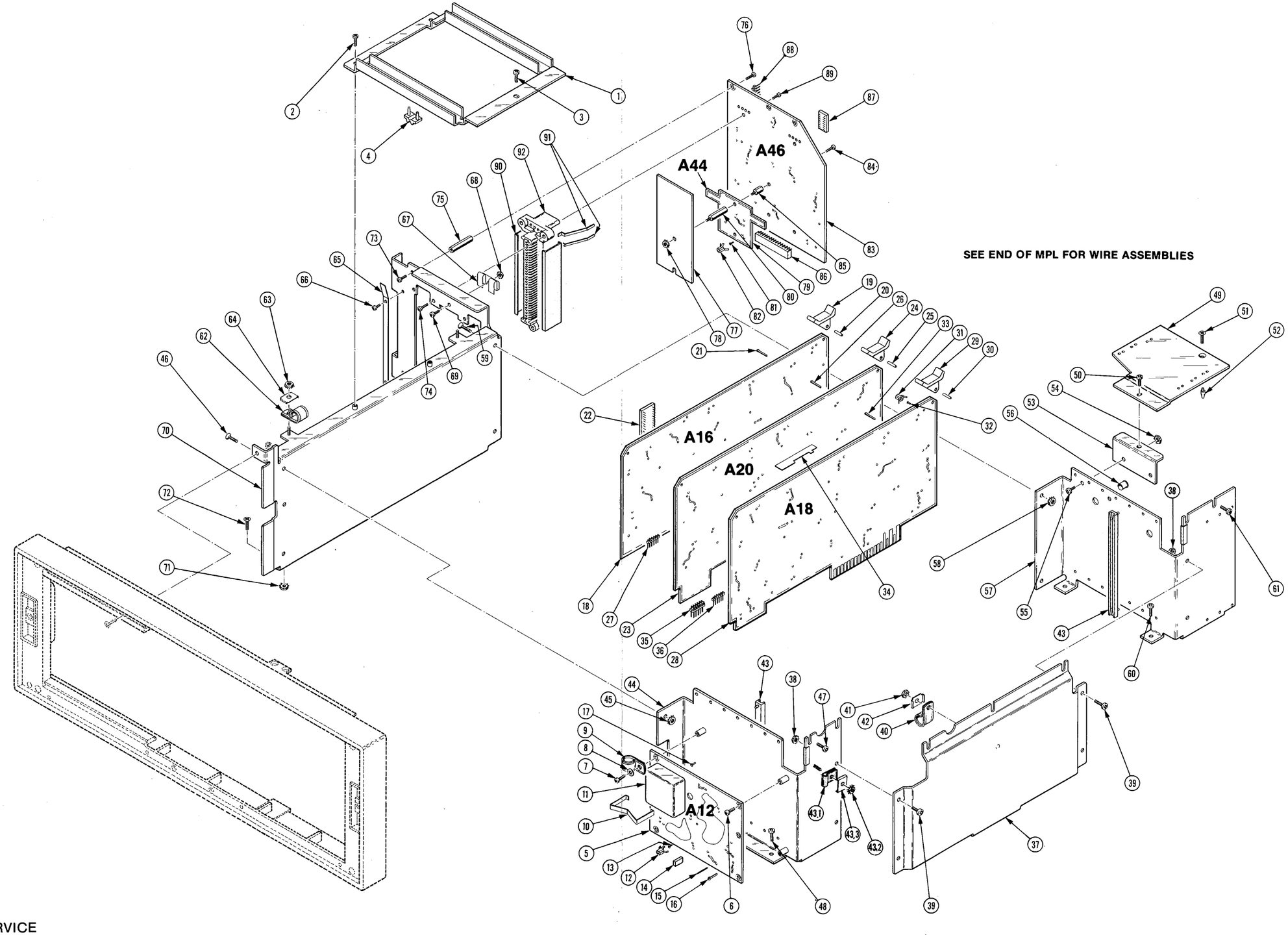

A44
A46
A16
A20
A18
A12
SEE END OF MPL FOR WIRE ASSEMBLIES

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	407-2124-00			1		BRACKET,SUPPORT:ALUMINUM	80009	407-2124-00
						(ATTACHING PARTS)		
-2	211-0008-00	B010100	B010109	2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
	211-0504-00	B010110		2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-3	211-0504-00			1		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-4	352-0509-00			14		HOLDER,CKT CD:	80009	352-0509-00
-5	----- -----			1		CKT BOARD ASSY:CLOCK BUFFER(SEE A12 REPL)		
						(ATTACHING PARTS)		
-6	211-0012-00			3		SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
-7	211-0016-00			1		SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL	83385	OBD
-8	210 0802-00			1		WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
-9	343-0006-00			1		CLAMP,LOOP:0.50 INCH DIAMETER,PLSTC	95987	1-2-6B
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-10	344-0230-00			1		. CLIP,SPG,TNSN:CHOKE COIL,CUBE	80009	344-0230-00
-11	----- -----			1		. CRYSTAL OSC:(SEE A12Y200 REPL)		
-12	----- -----			2		. CONN,RCPT,ELEC:(SEE A12J300,J310 REPL)		
-13	136-0252-07			2		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-14	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-15	----- -----			36		. TERMINAL,PIN:(SEE A12J328,J406,J418,J428,		
	----- -----			-		. J500,J510,J524 REPL)		
-16	----- -----			1		. TERM,TEST POINT:(SEE A12TP310 REPL)		
-17	136-0338-00			5		. SOCKET,PIN TERM:U/W 0.026-0.033 DIA PINS	00779	1-332075-5
-18	----- -----			1		CKT BOARD ASSY:TRANSLATOR(SEE A16 REPL)		
-19	105-0793-00			2		. EJECTOR,CKT BD:WHITE,PLASTIC	71279	415-7036-01-0020
-20	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-21	----- -----			3		. TERM,TEST POINT:(SEE A16TP100,TP600,		
	----- -----			-		. TP1000 REPL)		
-22	136-0578-00	B010100	B010174X	2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-23	----- -----			2		CKT BOARD ASSY:TIME BASE(SEE A20 REPL)		
	----- -----			-		EACH CKT BOARD ASSY INCLUDES:		
-24	105-0793-00			2		. EJECTOR,CKT BD:WHITE,PLASTIC	71279	415-7036-01-0020
-25	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-26	----- -----			5		. TERM,TEST POINT:(SEE A20TP107,TP301,TP311,		
	----- -----			-		. TP547,TP801 REPL)		
-27	----- -----			1		TERM SET,PIN:(SEE A20J658,J754 REPL)		
-28	----- -----			4		CKT BOARD ASSY:DATA STORAGE(SEE A18 REPL)		
	----- -----			-		EACH CKT BOARD ASSY INCLUDES:		
-29	105-0793-00			2		. EJECTOR,CKT BD:WHITE,PLASTIC	71279	415-7036-01-0020
-30	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-31	----- -----			1		. CONN,RCPT,ELEC:(SEE A18J002 REPL)		
-32	136-0252-07			1		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-33	----- -----			6		. TERM,TEST POINT:(SEE A18TP102,TP104,TP106,		
	----- -----			-		. TP108,TP202,TP808 REPL)		
-34	378-0144-00			1		. BAFFLE,AIR:BRASS	80009	378-0144-00
-35	----- -----			1		. TERM SET,PIN:(SEE A18J944 REPL)		
-36	----- -----			1		. TERM SET,PIN:(SEE A18J844,J946 REPL)		
-37	386-3750-00			1		SUPPORT,CHASSIS:	80009	386-3750-00
						(ATTACHING PARTS)		
-38	210-0457-00			9		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-39	211-0507-00			9		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-40	343-0013-00			1		CLAMP,LOOP:0.375 INCH DIA	95987	3-8-6B
						(ATTACHING PARTS)		
-41	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-42	210-0863-00			1		WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
						- - - * - - -		
-43	351-0087-00			14		GUIDE,CKT BOARD:4.75 INCH LONG,PLASTIC	80009	351-0087-00
-43.1	343-0007-00			1		CLAMP,LOOP:	95987	5-8-6B
						(ATTACHING PARTS)		
-43.2	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-43.3	210-0863-00			1		WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
						- - - * - - -		

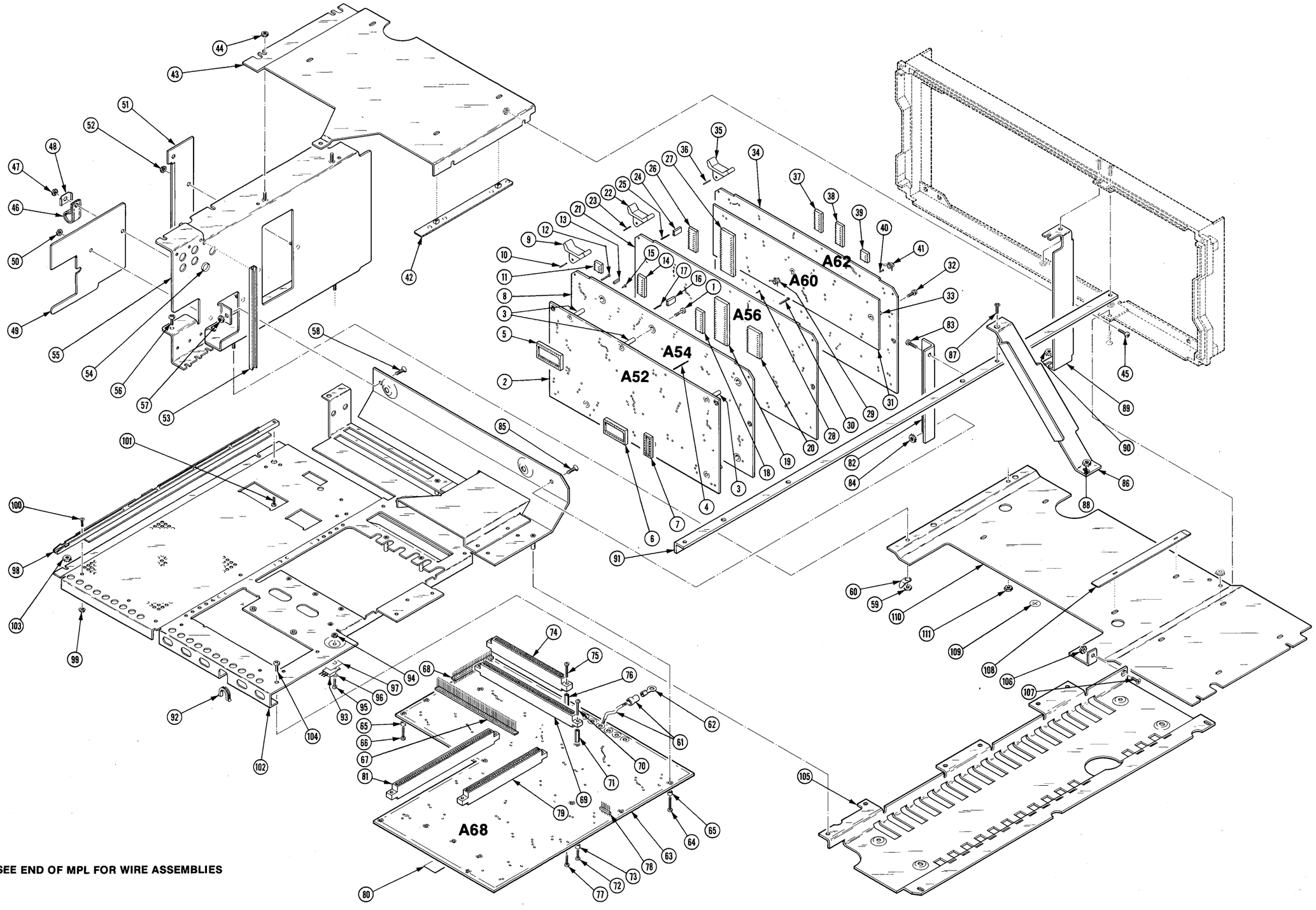
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-44	441-1379-00	B010100	B030640	1		CHAS,DIGITIZER:FRONT CIRCUIT BOARD	80009	441-1379-00
	441-1379-01	B030641		1		CHAS,DIGITIZER:FRONT,CIRCUIT BOARD	80009	441-1379-01
						(ATTACHING PARTS)		
-45	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-46	211-0538-00			2		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
-47	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-48	211-0504-00			4		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-49	386-4257-00	B010100	B030450	1		SUPPORT,CKT BD:ALUMINUM	80009	386-4257-00
	386-4257-01	B030451		1		SUPPORT,CKT BD:ALUMINUM	80009	386-4257-01
						(ATTACHING PARTS)		
-50	211-0504-00			1		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-51	211-0541-00			1		SCREW,MACHINE:6-32 X 0.25"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-52	386-1557-00			12		SPACER,CKT BD:0.29 H,ACETAL	80009	386-1557-00
-53	407-2041-00			1		BRACKET,CKT BD:ALUMINUM	80009	407-2041-00
						(ATTACHING PARTS)		
-54	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-55	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-56	348-0067-00			2		GROMMET,PLASTIC:0.312 INCH DIA	80009	348-0067-00
-57	441-1401-00			1		CHAS,DIGITIZER:REAR,CIRCUIT BOARD	80009	441-1401-00
						(ATTACHING PARTS)		
-58	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-59	211-0538-00			2		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
-60	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-61	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-62	343-0006-00			2		CLAMP,LOOP:0.50 INCH DIAMETER,PLSTC	95987	1-2-6B
						(ATTACHING PARTS)		
-63	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-64	210-0863-00			2		WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
						- - - * - - -		
-65	131-0800-00	B010100	B030697	2		CONTACT,ELEC:PLUG-IN GROUND	80009	131-0800-00
	131-0800-03	B030698		2		E		
						(ATTACHING PARTS)		
-66	213-0138-00			4		SCR,TPG,TF:4-24 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-67	131-0930-00			2		CONTACT,ELEC:PLUG-IN GROUND	80009	131-0930-00
						(ATTACHING PARTS)		
-68	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-69	211-0008-00			2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-70	441-1374-00	B010100	B010109	1		CHAS,PL-IN UNIT:	80009	441-1374-00
	441-1374-01	B010110		1		CHAS,PL-IN UNIT:	80009	441-1374-01
						(ATTACHING PARTS)		
-71	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-72	211-0538-00			4		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
-73	211-0008-00			2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-74	213-0119-00			6		SCR,TPG,THD FOR:4-24 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-75	129-0427-00			2		POST,ELEC-MECH:4-40 X 0.188 X 1.056" L HEX	80009	129-0427-00
						(ATTACHING PARTS)		
-76	211-0008-00			2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-77	200-2099-00			1		COVER,HOLE:ALUMINUM	80009	200-2099-00
						(ATTACHING PARTS)		
-78	210-0586-00			1		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
	672-0648-00			1		CKT BOARD ASSY:PLUG-IN INTERFACE	80009	672-0648-00
-79	-----	-----		1		. CKT BOARD ASSY:VERT INTERCONNECT(SEE A44 REPL)		
						(ATTACHING PARTS)		
-80	129-0285-00			2		. POST,ELEC-MECH:0.281 L X 0.188 HEX BRS	80009	129-0285-00
						- - - * - - -		
	-----	-----		-		. CKT BOARD ASSY INCLUDES:		
-81	136-0252-07			8		. . SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-82	-----	-----		8		. . CONN,RCPT,ELEC:(SEE A44J020,J100,J110,J120,		
	-----	-----		-		. . J200,J210,J220,J320 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-83	----- -----			1		. CKT BOARD ASSY:PLUG-IN INTFC(SEE A46 REPL)		
						(ATTACHING PARTS)		
-84	211-0014-00			2		. SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-85	129-0456-00			2		. SPACER,POST:0.75 L,W/4-40STUD,TAP,BRASS	80009	129-0456-00
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-87	136-0260-00	B010100	B030378	2		. . SOCKET,PLUG-IN:16 CONTACT,RECT SHAPE	71785	133-51-92-008
	136-0729-00	B030379		2		. . SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-88	----- -----			2		. . TERM SET,PIN:(SEE A46J100 REPL)		
	131-0767-11			2		. . CONN,RCPT,ELEC:CKT BD,35/70 CONTACT	80009	131-0767-11
						(ATTACHING PARTS)		
-89	213-0232-00			4		. . SCR,TPG,THD FOR:2-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. . CONNECTOR INCLUDES:		
-90	200-0950-00			4		. . . COVER,ELEC CONN:PLASTIC	80009	200-0950-00
-91	131-2158-01			140		. . . CONTACT,ELEC:CKT BD CONN,PH BRZ GOLD PL	80009	131-2158-01
-92	204-0365-00			2		. . . BODY,CONNECTOR:PLUG-IN CIRCUIT CARD	80009	204-0365-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-	672-0921-00			1		CKT BOARD ASSY:MPU	80009	672-0921-00
						(ATTACHING PARTS)		
-1	211-0155-00			6		SCREW,EXT,RLV B:4-40 X 0.375 INCH,SST	80009	211-0155-00
						- - - * - - -		
-2	----- -----			1		. CKT BOARD ASSY:MPU MEMORY(SEE A52 REPL)		
-3	351-0188-00			6		. . GUIDE-POST,LOCK:0.65 INCH LONG	80009	351-0188-00
-4	131-0590-00			32		. . CONTACT,ELEC:0.71 INCH LONG	22526	47351
-5	136-0578-00	B010100	B030221	11		. . SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
	136-0751-00	B030222		11		. . SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-6	136-0634-00	B010100	B010174X	6		. . SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-7	136-0670-00	B010100	B010174X	2		. . SKT,PL-IN ELEK:MICROCKT,18 PIN,LOW PROFILE	73803	CS9002-18
-8	----- -----			2		. CKT BOARD ASSY:MPU(SEE A54 REPL)		
-9	105-0144-00			2		. . EJECTOR,CKT CD:MOLD PLASTIC,W/ROLL PIN	18677	S203
-10	214-1337-00			2		. . . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-11	136-0514-00	B010100	B010174X	1		. . SKT,PL-IN ELEC:MICROCIRCUIT,8 DIP	73803	CS9002-8
-12	----- -----			7		. . TERM,TEST POINT:(SEE A54TP104,TP112,TP222,		
	----- -----			-		. . TP702,TP734,TP834,TP838 REPL)		
-13	136-0263-04			32		. . SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-14	136-0260-00	B010100	B030389	1		. . SOCKET,PLUG-IN:16 CONTACT,RECT SHAPE	71785	133-51-92-008
	136-0729-00	B030390		1		. . SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-15	136-0252-07	B010100	B010174X	9		. . SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-16	131-0993-00			9		. . BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-17	----- -----			27		. . TERMINAL,PIN:(SEE A54J012,J216,J224,J234,		
	----- -----			-		. . J712,J714,J716,J718,J720 REPL)		
	361-0238-00			6		. . SPACER,SLEEVE:0.25 OD X 0.34 INCH LONG	80009	361-0238-00
-18	136-0634-00	B010100	B010174X	9		. . SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-19	136-0623-00	B010100	B010174	2		. . SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
	136-0623-00	B010175	B030389	1		. . SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
	136-0755-00	B030390		1		. . SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-20	136-0578-00	B010100	B010174X	1		. . SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-21	----- -----			1		CKT BOARD ASSY:IEEE/488 INTFC(SEE A56 REPL)		
-22	105-0144-00			2		. EJECTOR,CKT CD:MOLD PLASTIC,W/ROLL PIN	18677	S203
-23	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-24	131-0993-00			3		. BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-25	----- -----			9		. TERMINAL,PIN:(SEE A56J030,J300,J602 REPL)		
-26	136-0634-00	B010100	B010174X	4		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-27	136-0623-00	B010100	B010174X	1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-28	136-0252-07			3		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-29	----- -----			3		. CONN,RCPT,ELEC:(SEE A56J402,J500,J502 REPL)		
-30	----- -----			7		. TERM,TEST POINT:(SEE A56TP002,TP004,TP012,		
	----- -----			-		. TP232,TP322,TP500,TP600 REPL)		
-31	----- -----			1		CKT BOARD ASSY:SHIELD(SEE A60 REPL)		
-32	211-0116-00			3		. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
-33	129-0461-00			3		. POST,PRESSMOUNT:0.1632,W/4-40THRU,0.219 OD	80009	129-0461-00
-34	----- -----			1		CKT BOARD ASSY:TRIGGER(SEE A62 REPL)		
-35	105-0144-00			2		. EJECTOR,CKT CD:MOLD PLASTIC,W/ROLL PIN	18677	S203
-36	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-37	136-0260-02	B010100	B030368	2		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
	136-0729-00	B030369		2		. SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-38	136-0634-00	B010100	B010174	6		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
	136-0634-00	B010175	B030221	2		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
	136-0752-00	B030222		2		. SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-39	136-0514-00	B010100	B010174X	8		. SKT,PL-IN ELEC:MICROCIRCUIT,8 DIP	73803	CS9002-8
-40	136-0252-07	B010100	B010174	42		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
	136-0252-07	B010175		6		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-41	----- -----			6		. CONN,RCPT,ELEC:(SEE A62J102,J104,J202,J506,		
	----- -----			-		. J602,J606 REPL)		
-42	351-0279-00			2		GUIDE,SHOE:5.18 X 0.375,NYLON	80009	351-0279-00
-43	386-3746-00			1		SUPPORT,CHASSIS:TOP REAR	80009	386-3746-00
						(ATTACHING PARTS)		
-44	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-45	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-46	343-0006-00			1		CLAMP,LOOP:0.50 INCH DIAMETER,PLSTC	95987	1-2-6B
						(ATTACHING PARTS)		
-47	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-48	210-0863-00			1		WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-49	200-2139-00			1		COVER,CHASSIS:IO	80009	200-2139-00
						(ATTACHING PARTS)		
-50	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
						- - - * - - -		
-51	200-2093-00			2		COVER,HOLE:ALUMINUM	80009	200-2093-00
						(ATTACHING PARTS)		
-52	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
						- - - * - - -		
-53	351-0087-00			6		GUIDE,CKT BOARD:4.75 INCH LONG,PLASTIC	80009	351-0087-00
-54	348-0056-00			2		GROMMET,PLASTIC:0.375 INCH DIA	80009	348-0056-00
-55	441-1382-00			1		CHASSIS,CKT CD:	80009	441-1382-00
						(ATTACHING PARTS)		
-56	211-0507-00			1		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-57	210-0457-00			5		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-58	211-0538-00			2		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
-59	210-0407-00			2		NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
						- - - * - - -		
-60	210-0202-00			1		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-61	195-0544-00			1		LEAD,ELECTRICAL:12 AWG,2.0 L,2-N	80009	195-0544-00
-62	210-0337-00			1		. TERMINAL,LUG:0.145 ID,PLAIN,CU TIN PL	00779	320567
	195-0545-00			1		LEAD,ELECTRICAL:12 AWG,2.0 L,6-N	80009	195-0545-00
	210-0337-00			1		. TERMINAL,LUG:0.145 ID,PLAIN,CU TIN PL	00779	320567
	195-0546-00			2		LEAD,ELECTRICAL:12 AWG,2.0 L,0-N	80009	195-0546-00
	210-0337-00			2		. TERMINAL,LUG:0.145 ID,PLAIN,CU TIN PL	00779	320567
	195-0547-00			2		LEAD,ELECTRICAL:12 AWG,2.0 L,7-N	80009	195-0547-00
	210-0337-00			2		. TERMINAL,LUG:0.145 ID,PLAIN,CU TIN PL	00779	320567
-63	----- -----			1		CKT BOARD ASSY:MAIN INTCON(SEE A68 REPL)		
						(ATTACHING PARTS)		
-64	211-0016-00			8		SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL	83385	OBD
-65	361-0762-00			11		SPACER,SLEEVE:0.128 ID X 0.15" L,BRASS	80009	361-0762-00
-66	211-0012-00			3		SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-67	----- -----			1		. TERM SET,PIN:(SEE A68J118 REPL)		
-68	----- -----			5		. TERM SET,PIN(SEE A68J006,J520,J522,J524,J526,		
	----- -----			-		. J528,J530,J532,J534,J536,J546,J548,J550,J552,		
	----- -----			-		. J554,J556,J558 REPL)		
-69	----- -----			1		. CONN,RCPT,ELEC:(SEE A68J108 REPL)		
						(ATTACHING PARTS)		
-70	211-0014-00			2		. SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-71	129-0420-00			2		. POST,ELEC-MECH:0.575 LONG X 0.188 I HEX	80009	129-0420-00
-72	211-0012-00			2		. SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
-73	361-0762-00			2		. SPACER,SLEEVE:0.128 ID X 0.15" L,BRASS	80009	361-0762-00
						- - - * - - -		
-74	----- -----			2		. CONN,RCPT,ELEC:(SEE A68J100,J104 REPL)		
						(ATTACHING PARTS)		
-75	211-0014-00			4		. SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-76	129-0420-00			4		. POST,ELEC-MECH:0.575 LONG X 0.188 I HEX	80009	129-0420-00
-77	211-0008-00			4		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-78	----- -----			1		. CONTACT SET,ELE:(SEE A68J500,J559 REPL)		
-79	----- -----			6		. CONN,RCPT,ELEC:(SEE A68J332,J334,J430,J436,		
	----- -----			-		. J438,J530 REPL)		
-80	334-2208-00			1		. MARKER,IDENT:WARNING	80009	334-2208-00
-81	----- -----			1		. CONN,RCPT,ELEC:(SEE A68J340 REPL)		
-82	407-2462-00			1		BRACKET,SUPPORT:POWER SUPPLY,AL	80009	407-2462-00
						(ATTACHING PARTS)		
-83	211-0507-00			1		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-84	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-85	211-0538-00			1		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-86	426-1420-00			1		FRAME,SUPPORT:DIGITIZER	80009	426-1420-00
						(ATTACHING PARTS)		
-87	211-0538-00			1		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
-88	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
						- - - * - - -		

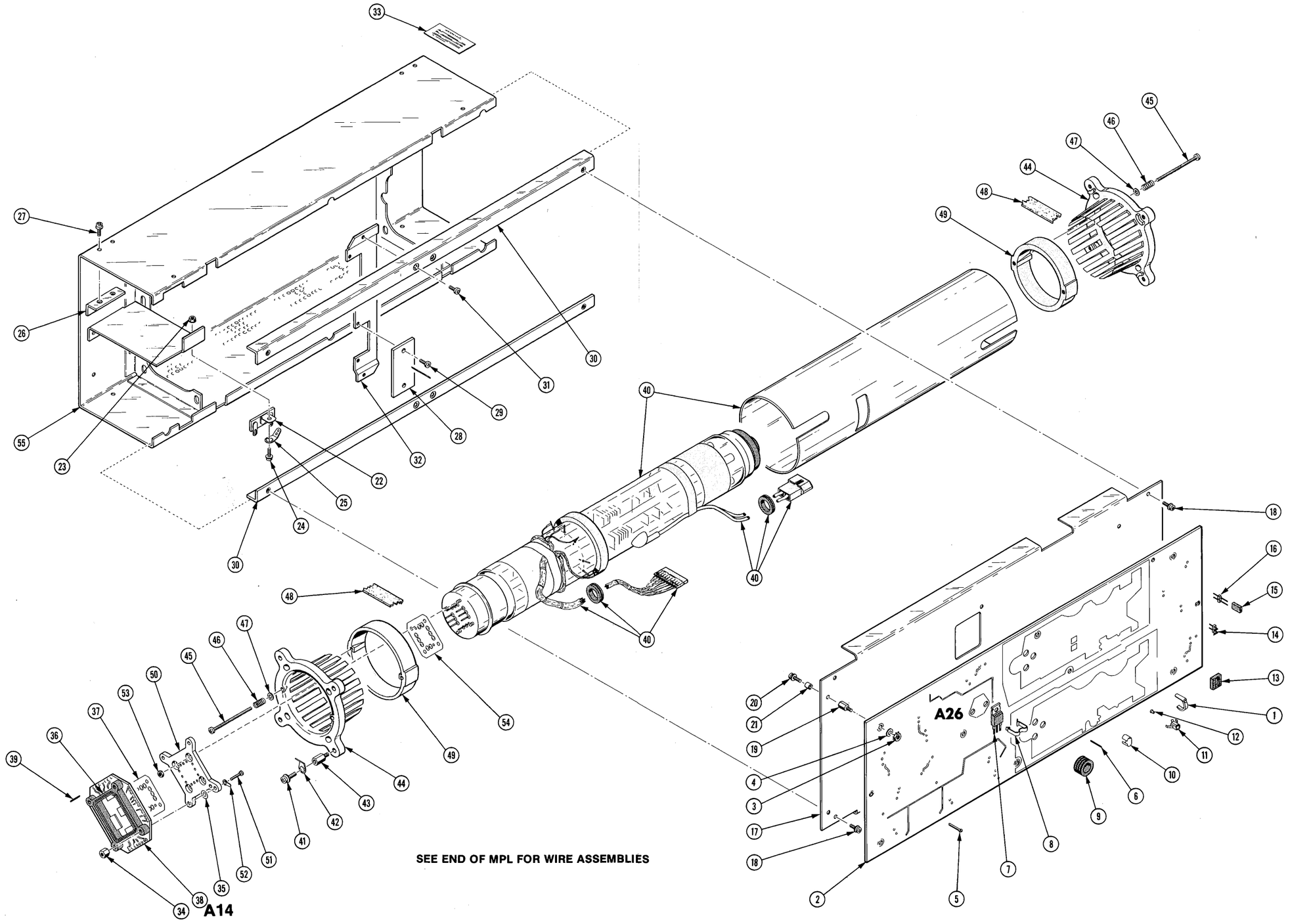
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-89	407-2020-00			1		BRACKET,SHIELD:EMI,ALUMINUM	80009	407-2020-00
						(ATTACHING PARTS)		
-90	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
						- - - * - - -		
-91	386-3757-00			1		SUPPORT,CHASSIS:	80009	386-3757-00
-92	348-0171-00			1		GROMMET,PLASTIC:U-SHAPED	80009	348-0171-00
-93	----- -----			1		MICROCIRCUIT,LI:(SEE U5559 REPL)		
						(ATTACHING PARTS)		
-94	210-0586-00			1		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-95	211-0097-00			1		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-96	210-1178-00			1		WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
-97	342-0355-00			1		INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	000BB	7403-09FR-51
						- - - * - - -		
-98	351-0295-02			2		GUIDE,SLIDE:PLUG-IN,LWR	80009	351-0295-02
						(ATTACHING PARTS)		
-99	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-100	211-0101-00			2		SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
-101	213-0088-00			2		SCR,TPG,THD CTG:4-24 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-102	441-1375-01			1		CHASSIS,PLENUM:W/BRACKET & HARDWARE	80009	441-1375-01
						(ATTACHING PARTS)		
-103	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-104	211-0504-00			1		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-105	441-1380-00			1		CHAS,DIGITIZER:CRT SHIELD	80009	441-1380-00
						(ATTACHING PARTS)		
-106	210-0457-00			3		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-107	211-0538-00			1		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-108	351-0279-00			4		GUIDE,SHOE:5.18 X 0.375,NYLON	80009	351-0279-00
-109	334-3379-01			1		MARKER,IDENT:MARKED GROUNDSYMBOL	80009	334-3379-01
-110	386-3747-00			1		SUPPORT,CHASSIS:BOTTOM REAR	80009	386-3747-00
						(ATTACHING PARTS)		
-111	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
						- - - * - - -		



SEE END OF MPL FOR WIRE ASSEMBLIES

FIG. 2 CHASSIS

FIG. 4 CRT ASSY



SEE END OF MPL FOR WIRE ASSEMBLIES

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-1	343-0089-00			1		CLAMP,LOOP:LARGE	80009	343-0089-00
-2	----- -----			1		CKT BOARD ASSY:DEFLECTION AMP(SEE A26 REPL)		
						(ATTACHING PARTS)		
-3	210-0586-00			8		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-4	210-0994-00			8		WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
						- - - * - - -		
	----- -----			-		CKT BOARD INCLUDES:		
-5	----- -----			23		. TERM,TEST POINT:(SEE A26TP002,TP022,TP040,		
	----- -----			-		. TP041,TP122,TP216,TP226,TP315,TP316,TP320,		
	----- -----			-		. TP330,TP331,TP332,TP333,TP344,TP420,TP446,		
	----- -----			-		. TP448,TP806,TP816,TP924,TP936,TP938 REPL)		
-6	----- -----			4		. TERMINAL,PIN:(SEE A26J926,J928 REPL)		
-7	----- -----			1		. MICROCIRCUIT,LI:(SEE A26U314 REPL)		
						(ATTACHING PARTS)		
-8	344-0236-00			1		. CLIP,SPR TNSN:	80009	344-0236-00
						- - - * - - -		
-9	214-0668-00			8		. HEAT SINK,ELEC:FOR TO-5	13103	2211B
-10	214-0973-00			2		. HEAT SINK,ELEC:0.28 X 0.18 OVAL X 0.187"H	80009	214-0973-00
-11	----- -----			6		. CONN,RCPT,ELEC:(SEE A26J622,J646,J714,J716,		
	----- -----			-		. J836,J838 REPL)		
-12	136-0252-07			42		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-13	136-0514-00	B010100	B010174X	2		. SKT,PL-IN ELEC:MICROCIRCUIT,8 DIP	73803	CS9002-8
-14	----- -----			1		. TERM SET,PIN:(SEE A26J012,J022 REPL)		
-15	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-16	----- -----			2		. TERM SET,PIN:(SEE A26J002,J010,J020,J030,		
	----- -----			-		. J040,J906,J918,J938,J948 REPL)		
	610-0386-00			1		CRT ASSEMBLY:	80009	610-0386-00
-17	200-2073-01			1		. COVER,CRT SHLD:	80009	200-2073-01
						(ATTACHING PARTS)		
-18	211-0116-00			4		. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
-19	220-0706-00			8		. NUT,SLEEVE:4-40 X 0.188 HEX,BRS,CU-SN	80009	220-0706-00
						(ATTACHING PARTS)		
-20	211-0152-00			8		. SCR,ASSEM WSHR:4-40 X 0.625 INCH,PNH BRS	83385	OBD
						- - - * - - -		
-21	361-0552-00			8		. SPACER,SLEEVE:0.093 L X 0.126 ID BRS ID	76854	3-5116-322
-22	131-0023-00			1		. TERMINAL CARD:2 LUG/1 MTG LUG	71785	322-11-03-028
						(ATTACHING PARTS)		
-23	220-0665-00			1		. NUT,PLAIN,HEX.:SLFLKG,4-40 X0.25",PLSTC	23050	OBD
-24	211-0116-00			1		. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
-25	210-0201-00			1		. TERMINAL,LUG:0.12 ID,LOCKING,BRZ TIN PL	86928	OBD
-26	407-1942-00			2		. BRACKET,ANGLE:CRT SHIELD,ALUMINUM	80009	407-1942-00
						(ATTACHING PARTS)		
-27	211-0116-00	B010100	B030290	7		. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
	211-0292-00	B030291		7		. SCR,ASSEM WSHR:4-40 X 0.29,BRS NI PL	78189	OBD
						- - - * - - -		
-28	----- -----			2		. RES.,FXD,FILM:(SEE U5015,U5040 REPL)		
						(ATTACHING PARTS)		
-29	211-0147-00			4		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-30	407-1940-00			2		. BRACKET,COVER:	80009	407-1940-00
						(ATTACHING PARTS)		
-31	211-0147-00			2		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-32	407-1939-00			1		. BRACKET,CRT:	80009	407-1939-00
-33	334-1379-00			1		. LABEL:CRT,ADHESIVE BACK	80009	334-1379-00
	----- -----			2		. CKT BOARD ASSY:HEADER(SEE A24 REPL)		
						(ATTACHING PARTS)		
-34	129-0157-00			8		. POST,ELEC-MECH:0.23 INCH L X0.25 INCH HEX	80009	129-0157-00
-35	210-1274-00			8		. WASHER,FLAT:0.1 ID X 0.002 THK	80009	210-1274-00
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-	----- -----			-		HEADER BOARD ASSY INCLUDES:		
-36	426-1434-00			1		. FRAME,MICROCKT:	80009	426-1434-00
-37	348-0512-00			1		. GASKET:CRT CKT INTERFACE	80009	348-0512-00
-38	----- -----			1		. CKT BOARD ASSY:HEADER		
	----- -----			-		(NOT REPLACEABLE ORDER NEXT HIGHER ASSY)		
-39	----- -----			49		. . TERMINAL,PIN:(SEE A14J007,J008,J009,		
	----- -----			-		. . J015,J016,J101,J102,J113,J114 REPL)		
-40	----- -----			2		. ELECTRON,TUBE:(SEE V5201,V5202 REPL)		
						(ATTACHING PARTS)		
-41	211-0601-00			8		. SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	OBD
-42	210-0202-00			2		. TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-43	129-0648-00			6		. SPACER,POST:0.675 L,W/6-32 EXT & INT THD	80009	129-0648-00
						- - - * - - -		
	----- -----			-		. ELECTRON,TUBE ASSY INCLUDES:		
-44	343-0205-01			2		. . RTNR,ELCTRN TU:3.0 DIA X 1.5L,DELRIN	80009	343-0205-01
						(ATTACHING PARTS)		
-45	211-0170-00			4		. . SCREW,MACHINE:4-40 X 2.75 INCH,PNH STL	83385	OBD
-46	214-1333-00			4		. . SPRING,HLCPS:0.213 OD X 0.375 INCH LONG	80009	214-1333-00
-47	210-1002-00			4		. . WASHER,FLAT:0.125 ID X 0.25 INCH OD,BRS	12327	OBD
-48	253-0056-00			4		. . CUSHION:POLYURETHANE FOAM,PRESSURE SENS	04963	4116
-49	440-2498-00			2		. . RING,CLAMP:SLOTTED	80009	440-2498-00
-50	440-2315-00			1		. . MTG PL,CKT BD:ASSEMBLY	80009	440-2315-00
						(ATTACHING PARTS)		
-51	211-0081-00			4		. . SCREW,MACHINE:2-56 X 0.562,PNH STL	83385	OBD
-52	210-0259-00			1		. . TERMINAL,LUG:0.099"ID INT TOOTH,SE	80009	210-0259-00
-53	210-0405-00			4		. . NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	12157-50
						- - - * - - -		
-54	348-0512-01			2		. . GASKET:CRT CKT INTERFACE,W/TAB	80009	348-0512-01
-55	337-2409-02			1		. SHIELD,CRT:OUTSIDE,W/SUPPORT & BRACKET	80009	337-2409-02

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
5-1	343-0006-00			2		CLAMP,LOOP:0.50 INCH DIAMETER,PLSTC	95987	1-2-6B
						(ATTACHING PARTS)		
-2	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-3	210-0863-00			2		WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
						- - - * - - -		
-3.1	343-0013-00			1		CLAMP,LOOP:0.375 INCH DIA	95987	3-8-6B
						(ATTACHING PARTS)		
-3.2	211-0507-00			1		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-3.3	210-0863-00			1		WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
						- - - * - - -		
	621-0477-00	B010100	B029999	1		POWER SUPPLY:	80009	621-0477-00
	621-0477-01	B030000		1		POWER SUPPLY:	80009	621-0477-01
						(ATTACHING PARTS)		
-4	211-0504-00			4		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		HIGH VOLTAGE ASSY INCLUDES:		
-5	346-0045-00			8		STRAP,CONN COV:BNC ONE END,POLYPROPYLENE	80009	346-0045-00
-6	200-0678-00			8		COVER,ELEC CONN:BNC,SHORTING	91836	KC89-58TR5
-7	131-1171-00			4		. CONNECTOR,RCPT,:BNC,50 OHM	24931	28JR231-1
-8	131-1315-01			4		. CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR 306-1
-9	333-2307-00			1		. PANEL,REAR:HV BOX	80009	333-2307-00
						(ATTACHING PARTS)		
-10	211-0008-00			4		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-11	200-2091-00			2		. COVER,HV BOX:ALUMINUM	80009	200-2091-00
						(ATTACHING PARTS)		
-12	211-0101-00			4		. SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-13	407-2505-00			1		. BRACKET,CKT BD:RESISTOR,AL	80009	407-2505-00
						(ATTACHING PARTS)		
-14	211-0503-00			1		. SCREW,MACHINE:6-32 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-15	----- -----			1		. CKT BOARD ASSY:HV RESISTOR(SEE A70 REPL)		
-16	342-0384-00			1		. INSULATOR,HV:POLYSULFONE	80009	342-0384-00
-17	----- -----			1		. CKT BOARD ASSY:HIGH VOLTAGE OSC(SEE A76 REPL)		
						(ATTACHING PARTS)		
-18	211-0008-00			4		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-19	----- -----			6		. . TERMINAL,PIN:(SEE A76J001 REPL)		
-20	----- -----			1		. . TRANSFORMER:(SEE A76T110 REPL)		
-21	----- -----			1		. TRANSISTOR:(SEE Q002 REPL)		
						(ATTACHING PARTS)		
-22	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-23	210-1178-00			1		. WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
						- - - * - - -		
-24	342-0202-00			1		. INSULATOR,PLATE:TRANSISTOR	01295	10-21-023-106
-25	348-0005-00			1		. GROMMET,RUBBER:0.50 INCH DIA	70485	230
-26	441-1381-00			1		. CHASSIS,CKT BD:HIGH VOLTAGE SUPPLY	80009	441-1381-00
						(ATTACHING PARTS)		
-27	211-0033-00			3		. SCR,ASSEM WSHR:4-40 X 0.312 PNH,STL,CD PL	83385	OBD
-28	211-0101-00			1		. SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-29	337-2425-00			1		. SHIELD,ELEC:HIGH VOLTAGE SUPPLY	80009	337-2425-00
-30	----- -----			1		. POWER SUPPLY:(SEE A74 REPL)		
-31	----- -----			1		. POWER SUPPLY:(SEE A72 REPL)		
-32	348-0145-00			2		. GROMMET,PLASTIC:U-SHP,1.0 X 0.42 INCH	80009	348-0145-00
-33	210-0201-00			1		. TERMINAL,LUG:0.12 ID,LOCKING,BRZ TIN PL	86928	OBD
						(ATTACHING PARTS)		
-34	211-0101-00			2		. SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
-35	210-0551-00			1		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	OBD
						- - - * - - -		
-35.1	175-2808-00			2		. LEAD ASSY,ELEC:2,22 AWG,5.5 L	80009	175-2808-00
-36	204-0826-00			2		. . CONN BODY,RCPT:2 CONT,FEMALE	27264	03-09-1021

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
5-37	426-1674-01			1		. MOUNT,PWR SPLY:STEEL	80009	426-1674-01
						(ATTACHING PARTS)		
-38	210-0458-00	B010100	B029999	1		. NUT,PL,ASSEM WA:8-32 X 0.344 INCH,STL	83385	OBD
	210-0409-00	B030000		1		. NUT,PLAIN,HEX.:8-32 X 0.312 INCH,BRS	73743	3046-402
-38.1	210-0205-00	XB030000		1		. TERMINAL,LUG:SE #8	86928	5442-7
						- - - * - - -		
-39	342-0408-00	B010100	B029999	2		. INSULATOR,STDF:0.975 L X 0.312 OD,TEFLON	80009	342-0408-00
	342-0408-00	B030000		3		. INSULATOR,STDF:0.975 L X 0.312 OD,TEFLON	80009	342-0408-00
						(ATTACHING PARTS)		
-40	213-0149-00	B010100	B029999	6		. SCR,TAP.,THD FO:6-32 X 0.375 INCH,PNH BRS	83385	OBD
	213-0146-00	B030000		6		. SCR,TPG,THD FOR:6-20 X 0.313 INCH,PNH STL	83385	OBD
-41	210-0202-00	B010100	B029999	3		. TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
	210-0202-00	B030000		4		. TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-42	210-0203-00	B010100	B029999X	1		. TERMINAL,LUG:SE #6	78189	2103-06-00-2520N
						- - - * - - -		
-43	----- -----			2		. RES,VAR,NONWW:(SEE R5006,R5007 REPL)		
						(ATTACHING PARTS)		
-44	220-0413-00	B010100	B029999	2		. NUT,SLEEVE:4-40 X 0.562 INCH LONG	80009	220-0413-00
	220-0787-00	B030000		2		. NUT,PLAIN,HEX:0.25-36 X 0.312 HEX,SST	24931	OBD
-45	210-0978-00	B010100	B029999	2		. WASHER,FLAT:0.375 ID X 0.50 INCH OD,STL	78471	OBD
	210-0905-00	B030000		4		. WASHER,FLAT:0.256 ID X 0.05 THK,BRS	83385	OBD
-45.1	210-0940-00	XB030000		4		. WASHER,FLAT:0.25 ID X 0.375 INCH OD,STL	79807	OBD
-46	210-0051-00	B010100	B029999	2		. WASHER,LOCK:INTL,0.425" ID X 0.615 OD,STL	78189	1220-08-00-0541C
	210-1026-00	B030000		2		. WASHER,LOCK:0.26 ID,INTL,0.025 THK,STL	78189	1114-00
						- - - * - - -		
-47	348-0005-00			1		. GROMMET,RUBBER:0.50 INCH DIA	70485	230
-48	380-0506-00			1		. HSG,HV SUPPLY:	80009	380-0506-00
-48.1	252-0571-00	XB030578		AR		. NEOPRENE EXTR:CHAN,0.234 X 0.156	85471	DIE#1353
-49	343-0235-00			2		. CLAMP,CRT SKT:DELRIN	80009	343-0235-00
-50	367-0117-00			2		. PULL,SOCKET:	80009	367-0117-00
-51	200-0917-01			2		. COV,ELECTRON TU:2.052 OD X 0.291" THK,PLSTC	80009	200-0917-01
-51.1	136-0304-03			2		. SKT,PL-IN ELEC:ELECTRON TUBE,14 CONTACT	80009	136-0304-03
-52	204-0355-02			2		. . BODY,CRT SOCKET:14 CONTACTS,NYLAFIL	80009	204-0355-02
-53	214-0464-00			28		. . CONTACT,ELEC:CRT	80009	214-0464-00

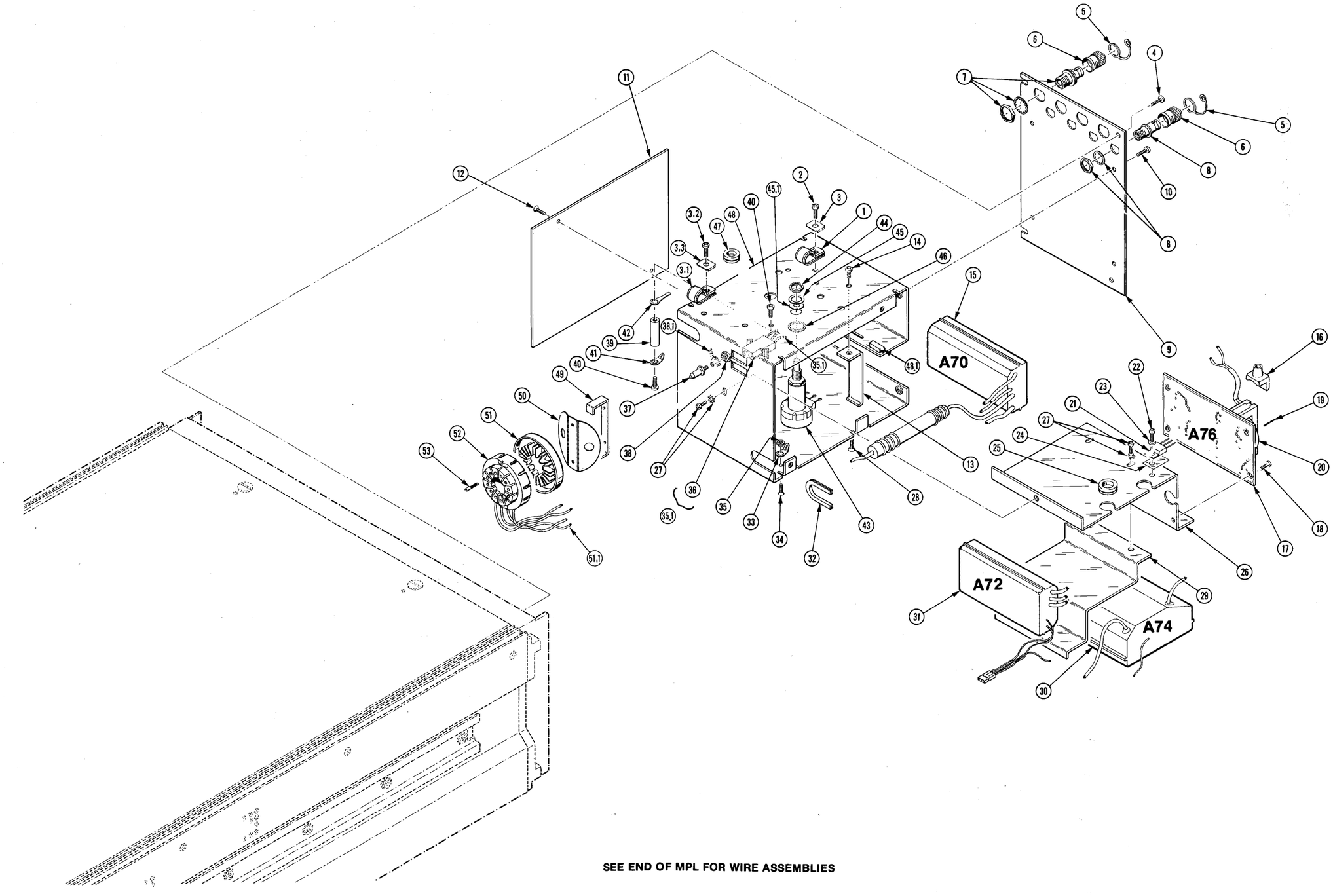


FIG. 5 HIGH VOLTAGE ASSY

SEE END OF MPL FOR WIRE ASSEMBLIES

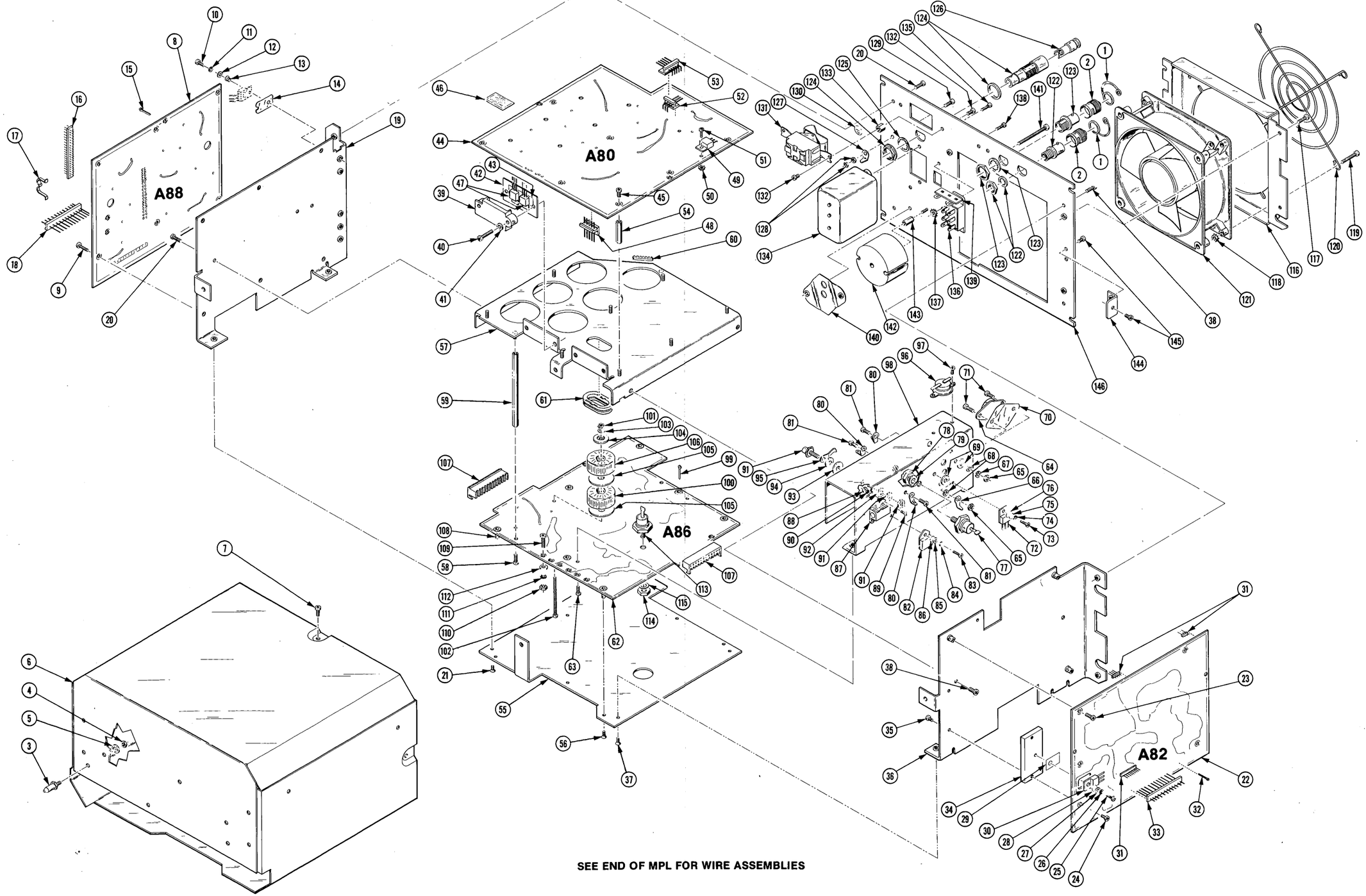


FIG. 6 POWER SUPPLY

SEE END OF MPL FOR WIRE ASSEMBLIES

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
6-1	346-0045-00			2		STRAP,CONN COV:BNC ONE END,POLYPROPYLENE	80009	346-0045-00
-2	200-0678-00			2		COVER,ELEC CONN:BNC,SHORTING	91836	KC89-58TR5
	620-0259-00	B010100	B030174	1		POWER SUPPLY:	80009	620-0259-00
	620-0259-01	B030175		1		POWER SUPPLY:	80009	620-0259-01
-3	426-1674-01			2		. MOUNT,PWR SPLY:STEEL	80009	426-1674-01
						(ATTACHING PARTS)		
-4	220-0555-00			2		. NUT,PLAIN,HEX.:8-32 X 0.25 INCH STL	000EL	OBD
-5	210-0008-00			2		. WASHER,LOCK:INTL,0.172 ID X 0.331"OD,STL	78189	1208-00-00-0541C
						- - - * - - -		
-6	200-2072-00			1		. COVER,PWR SPLY:TOP & BOTTOM	80009	200-2072-00
						(ATTACHING PARTS)		
-7	211-0504-00			7		. SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-8	----- -----			1		. CKT BOARD ASSY:REGULATOR(SEE A88 REPL)		
						(ATTACHING PARTS)		
-9	211-0008-00			6		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-10	211-0097-00			5		. SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-11	210-0054-00			5		. WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD STL	83385	OBD
-12	210-0994-00			5		. WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
-13	210-1178-00			5		. WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
-14	342-0203-00			5		. INSULATOR,PLATE:XSTR,0.675 X 0.625 X 0.001	18722	DF103C
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-15	----- -----			1		. . TERM,TEST POINT:(SEE A88TP328 REPL)		
-16	----- -----			2		. . TERM SET,PIN:(SEE A88J420 REPL)		
-17	344-0236-00			1		. . CLIP,SPR TNSN:	80009	344-0236-00
-18	----- -----			1		. . CONN,RCPT,ELEC:(SEE A88J450 REPL)		
-19	441-1372-00			1		. CHASSIS,RGLTR:	80009	441-1372-00
						(ATTACHING PARTS)		
-20	211-0507-00			4		. SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-21	211-0101-00	B010100	B030625	2		. SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
	211-0008-00	B030626		2		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-22	----- -----			1		. CKT BOARD ASSY:CONTROL(SEE A82 REPL)		
						(ATTACHING PARTS)		
-23	211-0008-00			3		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-24	211-0007-00			2		. SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
-25	211-0097-00			1		. SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-26	210-0054-00			1		. WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD STL	83385	OBD
-27	210-0994-00			1		. WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
-28	210-1178-00			1		. WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
-29	342-0202-00			1		. INSULATOR,PLATE:TRANSISTOR	01295	10-21-023-106
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-30	----- -----			1		. . TRANSISTOR:(SEE A82Q301 REPL)		
-31	----- -----			1		. . TERM SET,PIN:(SEE A82P020,P060,P320 REPL)		
-32	----- -----			5		. . TERM,TEST POINT:(SEE A82TP252,TP253,TP311,		
	----- -----			-		. . TP431,TP141 REPL)		
-33	----- -----			1		. . CONN,RCPT,ELEC:(SEE A82P040 REPL)		
-34	214-2771-00			1		. HEAT SINK,XSTR:(2)TO-220,ALUMINUM	80009	214-2771-00
						(ATTACHING PARTS)		
-35	211-0007-00			2		. SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-36	441-1452-00			1		. .CHAS,CNTRL BD:	80009	441-1452-00
						(ATTACHING PARTS)		
-37	211-0101-00	B010100	B030625	2		. SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
	211-0008-00	B030626		2		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-38	211-0507-00			4		. SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-39	200-2269-01			2		. COVER,XSTR:	80009	200-2269-01
						(ATTACHING PARTS)		
-40	211-0513-00			4		. SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-41	210-1092-00			4		. WASHER,FLAT:0.147 ID X 0.312" OD,BRS	12327	OBD
						- - - * - - -		
-42	342-0449-01			2		. INSULATOR,PLATE:TRANSISTOR,ALUMINA,PRINTED	80009	342-0449-01
-43	342-0458-00			2		. INSULATOR,PLATE:TRANSISTOR,MICA	08530	OBD
-44	----- -----			1		. CKT BOARD ASSY:LINE POWER(SEE A80 REPL)		
						(ATTACHING PARTS)		
-45	211-0008-00			8		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
6-	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-46	334-2359-00			1		. . MARKER,IDENT:WARNING	80009	334-2359-00
-47	----- -----			1		. . TRANSISTOR:(SEE A80Q011,Q012,Q031,Q041 REPL)		
-48	----- -----			1		. . CONN,RCPT,ELEC:(SEE A80J4 REPL)		
-49	----- -----			2		. . TRANSISTOR:(SEE A80Q501,Q521 REPL)		
						(ATTACHING PARTS)		
-50	210-0586-00			2		. . NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-51	211-0097-00			2		. . SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-52	----- -----			1		. . TERM SET,FEEDTH:(SEE A80J3 REPL)		
-53	----- -----			1		. . TERM SET,PIN:(SEE A80J2 REPL)		
-54	129-0427-00			8		. POST,ELEC-MECH:4-40 X 0.188 X 1.056" L HEX	80009	129-0427-00
-55	441-1454-00	B010100	B030625	1		. CHAS,RECT BD:	80009	441-1454-00
	441-1454-01	B030626		1		. CHAS,DIGITIZER:CIRCUIT BOARD	80009	441-1454-01
						(ATTACHING PARTS)		
-56	211-0101-00	B010100	B030625	7		. SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
	211-0008-00	B030626		7		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
	361-0917-00	XB030626		1		. SPACER,SLEEVE:0.141 ID X 0.25 INCH LONG	80009	361-0917-00
						(ATTACHING PARTS)		
	211-0016-00	XB030626		1		. SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL	83385	OBD
	210-0994-00	XB030626		1		. WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
	210-1178-00	XB030626		2		. WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
						- - - * - - -		
	386-1657-00	XB030626		1		. SUPPORT,CKT BD:	80009	386-1657-00
-57	441-1453-00			1		. CHAS,LINE PWR:	80009	441-1453-00
						(ATTACHING PARTS)		
-58	211-0012-00			2		. SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
-59	129-0783-00			2		. SPACER,POST:3.46 L,W/4-40 THD BOTH ENDS	80009	129-0783-00
						- - - * - - -		
-60	255-0334-00			3		. PLASTIC CHANNEL:12.75 X 0.175X 0.155,NYL	11897	122-37-2500
-61	348-0051-00			1		. GROMMET,RUBBER:BLACK,ROUND,0.75 ID	83907	1107
-62	----- -----			1		. CKT BOARD ASSY:RECTIFIER(SEE A86 REPL)		
	650-0183-00			1		. . MECHANICAL KIT:RECTIFIER	80009	650-0183-00
						(ATTACHING PARTS)		
-63	211-0008-00			2		. . SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
	----- -----			-		. . RECTIFIER,BRACKET INCLUDES:		
-64	----- -----			1		. . . TRANSISTOR:(SEE Q421 REPL)		
						(ATTACHING PARTS)		
-65	210-0407-00			2		. . . NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-66	210-0202-00			1		. . . TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-67	210-0006-00			1		. . . WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
-68	210-1092-00			2		. . . WASHER,FLAT:0.147 ID X 0.312" OD,BRS	12327	OBD
-69	210-0813-00			2		. . . WSHR,SHOULDERED:# 10 FIBER	74921	OBD
-70	386-0978-00			1		. . . INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
-71	211-0510-00			2		. . . SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-72	----- -----			1		. . . TRANSISTOR:(SEE Q511 REPL)		
						(ATTACHING PARTS)		
-73	211-0097-00			1		. . . SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-74	210-0054-00			1		. . . WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD STL	83385	OBD
-75	210-0994-00			1		. . . WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
-76	210-1178-00			1		. . . WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
						- - - * - - -		
-77	----- -----			3		. . . SEMICOND DEVICE:(SEE CR321,CR531,		
	----- -----			-		. . . CR631 REPL)		
						(ATTACHING PARTS)		
-78	210-0412-00			3		. . . NUT,PLAIN,HEX.:0.25-28 X 0.438,BRS CD PL	73743	3091-402
-79	210-0046-00			3		. . . WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	78189	1214-05-00-0541C
						- - - * - - -		
-80	210-0202-00			3		. . . TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
						(ATTACHING PARTS)		
-81	211-0504-00			3		. . . SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
6-82	----- -----			1		. . . TRANSISTOR:(SEE Q211 REPL)		
						(ATTACHING PARTS)		
-83	211-0097-00			1		. . . SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-84	210-0054-00			1		. . . WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD STL	83385	OBD
-85	210-0994-00			1		. . . WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
-86	210-1178-00			1		. . . WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
						- - - * - - -		
-87	----- -----			1		. . . RESISTOR:(SEE R111 REPL)		
						(ATTACHING PARTS)		
-88	210-0405-00			2		. . . NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	12157-50
-89	211-0062-00			2		. . . SCREW,MACHINE:2-56 X 0.312,PNH,STL	83385	OBD
-90	210-0001-00			2		. . . WASHER,LOCK:INTL,0.092 ID X 0.18"OD,STL	78189	1202-00-00-0541C
						- - - * - - -		
-91	----- -----			2		. . . SEMICOND DEVICE:(SEE CR231,CR331 REPL)		
-92	210-0813-00			4		. . . WSHR,SHOULDERED:# 10 FIBER	74921	OBD
-93	210-0917-00			2		. . . WASHER,NONMETAL:0.191 ID X 0.625 INCH OD	86445	OBD
-94	210-0805-00			2		. . . WASHER,FLAT:0.204 ID X 0.438 INCH OD,STL	12327	OBD
-95	210-0224-00			2		. . . TERMINAL,LUG:0.20 ID X 0.344 OD,SE,BRS	86928	A373-148-1
-96	----- -----			1		. . . SW,THERMOSTATIC:(SEE S5022 REPL)		
						(ATTACHING PARTS)		
-97	211-0008-00			2		. . . SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-98	214-2928-00			1		. . . HEAT SINK,ELEC:POWER SUPPLY,AL	80009	214-2928-00
-99	----- -----			1		. . TERM,TEST POINT:(SEE A86TP002 REPL)		
-100	----- -----			3		. . COIL,RF:(SEE A86L0511,L251,L261 REPL)		
						(ATTACHING PARTS)		
-101	210-0586-00			2		. . NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-102	211-0166-00			2		. . SCREW,MACHINE:4-40 X 1.750,PNH,STL,CD PL	83385	OBD
-103	210-0801-00			2		. . WASHER,FLAT:0.14 ID X 0.025 THK,BRS NI PL	12327	OBD
-104	200-0847-00			2		. . CAP,INSERT,KNOB:BLK,0.561 OD X0.18 H,PLSTC	80009	200-0847-00
-105	210-0966-00			4		. . WASHER,NONMETAL:0.312 ID X 0.875" OD,RBR	80009	210-0966-00
						- - - * - - -		
-106	----- -----			1		. . COIL,RF:(SEE A86L151 REPL)		
-107	131-1795-00			2		. . CONNECTOR,RCPT,:12 FEMALE CONTACT,RT-ANGLE	27264	09-62-3121
-108	129-0160-00			7		. . SPACER POST:0.25 L X 0.2188 TO MT SEAT	80009	129-0160-00
-109	211-0511-00			6		. . SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-110	210-0407-00			6		. . NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-111	210-0055-00			6		. . WASHER,LOCK:SPLIT,0.145 ID X 0.253 OD,STL	83385	OBD
-112	210-0802-00			6		. . WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
-113	----- -----			1		. . SEMICOND DEVICE:(SEE A86CR311 REPL)		
						(ATTACHING PARTS)		
-114	210-0412-00			1		. . NUT,PLAIN,HEX.:0.25-28 X 0.438,BRS CD PL	73743	3091-402
-115	210-0046-00			1		. . WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	78189	1214-05-00-0541C
						- - - * - - -		
-116	407-1934-01			1		. BRACKET,FAN:ALUMINUM	80009	407-1934-01
						(ATTACHING PARTS)		
-117	211-0507-00			4		. SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-118	210-0457-00			4		. NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
-119	211-0514-00			4		. SCREW,MACHINE:6-32 X 0.750 INCH,PNH STL	83385	OBD
						- - - * - - -		
-120	200-2222-00			1		. GUARD,FAN:	81041	6-182-033
-121	----- -----			1		. FAN:(SEE B5020 REPL)		
-122	131-0955-01			1		. CONN,RCPT,ELEC:BNC,FEMALE,MODIFIED	80009	131-0955-01
-123	131-0274-00			1		. CONNECTOR,RCPT,:BNC	91836	KC79-67
-124	204-0833-00			1		. BODY,FUSEHOLDER:3AG & 5 X 20MM FUSES	S3629	031.1653(MDLFEU)
-125	210-1039-00			1		. WASHER,LOCK:INT,0.521 ID X 0.625 INCH OD	24931	OBD
-126	200-2264-00			1		. CAP.,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-127	210-0202-00			2		. TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
						(ATTACHING PARTS)		
-128	210-0407-00			4		. NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-129	211-0510-00			2		. SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-130	334-3379-01			2		. MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-01
-131	----- -----			1		. SWITCH,TOGGLE:(SEE S5020 REPL)		
						(ATTACHING PARTS)		
-132	211-0504-00			4		. SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-133	385-0079-00			2		. SPACER,POST:0.375 L W/6-32 THD THRU,AL	80009	385-0079-00
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
6-134	----- -----			1		. FILTER:(SEE FL5020 REPL)		
						(ATTACHING PARTS)		
-135	211-0012-00			2		. SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
						- - - * - - -		
-136	----- -----			1		. SWITCH,SLIDE:(SEE S5021 REPL)		
						(ATTACHING PARTS)		
-137	210-0586-00			2		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-138	211-0012-00			2		. SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
						- - - * - - -		
-139	131-0023-00			1		. TERMINAL CARD:2 LUG/1 MTG LUG	71785	322-11-03-028
-140	386-2634-00			1		. PL,CHOKE MTG:	80009	386-2634-00
						(ATTACHING PARTS)		
-141	211-0553-00			2		. SCREW,MACHINE:6-32 X 1.5 INCH,PNH STL	83385	OBD
						- - - * - - -		
-142	----- -----			1		. TRANSFORMER:(SEE T5020 REPL)		
-143	220-0706-00			1		. NUT,SLEEVE:4-40 X 0.188 HEX,BRS,CU-SN	80009	220-0706-00
-144	406-0908-00			2		. BRACKET,ANGLE:CHASSIS LATCH	80009	406-0908-00
						(ATTACHING PARTS)		
-145	211-0504-00			4		. SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-146	333-2306-00			1		. PANEL,REAR:POWER SUPPLY	80009	333-2306-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						WIRE ASSEMBLIES		
	175-2062-00	B010100	B030577	2		CA ASSY,SP,ELEC:4,26 AWG,10.0L	80009	175-2062-00
	----- -----			-		(FROM A12J328 TO A20J658)		
	----- -----			-		(FROM A12J428 TO A20J658)		
	175-7371-00	B030578		1		CABLE ASSY,RF:50 OHM COAX,6.0 L,6-N	80009	175-7371-00
	----- -----			-		(FROM A12J428 TO A20J658)		
	175-7372-00	B030578		1		CABLE ASSY,RF:50 OHM COAX,6.0 L,6-O	80009	175-7372-00
	----- -----			-		(FROM A12J328 TO A20J658)		
	352-0162-00			4		. HLDR,TERM CONN:4 WIRE BLACK	80009	352-0162-00
	175-2454-00			1		CA ASSY,SP,ELEC:4,22 AWG,3.5 L,RIBBON	80009	175-2454-00
	----- -----			-		(FROM A80 TO A80P020) SUBPART OF A80		
	352-0162-03			1		. CONN BODY,PL,EL:4 WIRE ORANGE	80009	352-0162-03
	175-2582-00			6		CA ASSY,SP,ELEC:6,26 AWG,3.0 L,RIBBON	80009	175-2582-00
	----- -----			-		(FROM A18J944 TO A18J946) QTY 2		
	----- -----			-		(FROM A18J946 TO A20J754) QTY 2		
	----- -----			-		(FROM A18J844 TO A18J844) QTY 2		
	352-0164-00			12		. CONN BODY,PL,EL:6 WIRE BLACK	80009	352-0164-00
	175-2775-00			1		CA ASSY,SP,ELEC:8,26 AWG,8.0 L	80009	175-2775-00
	----- -----			-		(FROM A82P320 TO A68J500) SUBPART OF 620-0259-00		
	175-2794-00			1		CA ASSY,SP,ELEC:40,22 AWG,9.0L	80009	175-2794-00
	----- -----			-		(FROM A46J100 TO A88J420)		
	352-0330-00			2		. HLDR,TERM. CONN:44 WIRE,DBL ROW,BLACK	22526	65043-015
	134-0153-00			8		. KEY,PLZN CONN:MINI LATCH HSG	80009	134-0153-00
	175-2796-00			2		CA ASSY,SP,ELEC:6,26 AWG,3.5 L	80009	175-2796-00
	----- -----			-		(FROM A26J010 TO A14J102,J5009) V5201		
	----- -----			-		(FROM A26J020 TO A14J102,J5009) V5202		
	352-0168-01			2		. HLDR,TERM CONN:10 WIRE,BROWN	80009	352-0168-01
	352-0165-02			2		. CONN BODY,PL,EL:7 WIRE RED	80009	352-0165-02
	352-0169-09			2		. CONN BODY,PL,EL:2 WIRE WHITE	80009	352-0169-09
	134-0153-00			4		. KEY,PLZN CONN:MINI LATCH HSG	80009	134-0153-00
	175-2798-00			2		CA ASSY,SP,ELEC:5,26 AWG,6.0 L	80009	175-2798-00
	----- -----			-		(FROM A26J012 TO A14J113,J016) V5201		
	----- -----			-		(FROM A26J022 TO A14J113,J016) V5202		
	352-0167-02			2		. CONN BODY,PL,EL:9 WIRE RED	80009	352-0167-02
	352-0164-06			2		. CONN BODY,PL,EL:6 WIRE BLUE	80009	352-0164-06
	352-0161-03			2		. CONN BODY,PL,EL:3 WIRE ORANGE	80009	352-0161-03
	134-0153-00			4		. KEY,PLZN CONN:MINI LATCH HSG	80009	134-0153-00
	175-2799-00			1		CA ASSY,SP,ELEC:9,26 AWG,14.0L,RIBBON	80009	175-2799-00
	----- -----			-		(FROM A68J556 TO A10J556)		
	352-0167-03			2		. CONN BODY,PL,EL:9 WIRE ORANGE	80009	352-0167-03
	175-2800-00			1		CA ASSY,SP,ELEC:9,26 AWG,14.0L,RIBBON	80009	175-2800-00
	----- -----			-		(FROM A68J554 TO A10J554)		
	352-0167-04			2		. CONN BODY,PL,EL:9 WIRE YELLOW	80009	352-0167-04
	175-2801-00			1		CA ASSY,SP,ELEC:9,26 AWG,15.0L,RIBBON	80009	175-2801-00
	----- -----			-		(FROM A68J552 TO A10J552)		
	352-0167-05			2		. CONN BODY,PL,EL:9 WIRE GREEN	80009	352-0167-05
	175-2802-00			1		CA ASSY,SP,ELEC:9,26 AWG,15.0L,RIBBON	80009	175-2802-00
	----- -----			-		(FROM A68J550 TO A10J550)		
	352-0167-06			2		. CONN BODY,PL,EL:9 WIRE BLUE	80009	352-0167-06
	175-2803-00			1		CA ASSY,SP,ELEC:4,26 AWG,16.0L,RIBBON	80009	175-2803-00
	----- -----			-		(FROM A68J548 TO A10J548)		
	352-0162-07			2		. CONN BODY,PL,EL:4 WIRE VIOLET	80009	352-0162-07
	175-2804-00			1		CA ASSY,SP,ELEC:6,26 AWG,20.0L	80009	175-2804-00
	----- -----			-		(FROM A68J520 TO A26J906)		
	352-0165-09			2		. CONN BODY,PL,EL:7 WIRE WHITE	80009	352-0165-09
	175-2805-00			1		CA ASSY,SP,ELEC:4,22 AWG,18.0L	80009	175-2805-00
	----- -----			-		(FROM A68J558 TO A26J030)		
	352-0163-02			2		. CONN BODY,PL,EL:5 WIRE RED	80009	352-0163-02
	134-0153-00			2		. KEY,PLZN CONN:MINI LATCH HSG	80009	134-0153-00
	175-2806-00			1		LEAD ASSY,ELEC:3,26 AWG,2.0 L	80009	175-2806-00
	----- -----			-		(FROM A68J559 TO U5559)		
	352-0161-01			1		. CONN BODY,PL,EL:3 WIRE BROWN	80009	352-0161-01
	175-2807-00			1		CA ASSY,SP,ELEC:4,26 AWG,16.0L,RIBBON	80009	175-2807-00
	----- -----			-		(FROM A68J546 TO A12J500)		
	352-0167-08			2		. CONN BODY,PL,EL:9 WIRE GRAY	80009	352-0167-08

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	175-2812-00			2		CA ASSY,RF:1,50 OHM COAX	80009	175-2812-00
	----- -----			-		(FROM A12J418 TO A14J007) V5201		
	----- -----			-		(FROM A12J524 TO A14J007) V5202		
	352-0162-07			2		. CONN BODY,PL,EL:4 WIRE VIOLET	80009	352-0162-07
	175-2827-00			1		CA ASSY,SP,ELEC:28,26 AWG,19.0 L,RIBBON	80009	175-2827-00
	----- -----			-		(FROM A68J536 TO A14J008) V5202		
	----- -----			-		(FROM A68J534 TO A14J101) V5202		
	----- -----			-		(FROM A68J532 TO A14J114) V5202		
	----- -----			-		(FROM A68J530 TO A14J015) V5202		
	352-0165-01			2		. CONN BODY,PL,EL:7 WIRE BROWN	80009	352-0165-01
	352-0165-02			1		. CONN BODY,PL,EL:7 WIRE RED	80009	352-0165-02
	352-0165-03			1		. CONN BODY,PL,EL:7 WIRE ORANGE	80009	352-0165-03
	352-0165-04			2		. CONN BODY,PL,EL:7 WIRE YELLOW	80009	352-0165-04
	352-0165-05			1		. CONN BODY,PL,EL:7 WIRE GREEN	80009	352-0165-05
	352-0165-08			1		. CONN BODY,PL,EL:7 WIRE GRAY	80009	352-0165-08
	175-2828-00			1		CA ASSY,SP,ELEC:28,26 AWG,18.0 L,RIBBON	80009	175-2828-00
	----- -----			-		(FROM A68J528 TO A14J008) V5201		
	----- -----			-		(FROM A68J526 TO A14J101) V5201		
	----- -----			-		(FROM A68J524 TO A14J114) V5201		
	----- -----			-		(FROM A68J522 TO A14J015) V5201		
	352-0165-01			1		. CONN BODY,PL,EL:7 WIRE BROWN	80009	352-0165-01
	352-0165-04			1		. CONN BODY,PL,EL:7 WIRE YELLOW	80009	352-0165-04
	352-0165-05			2		. CONN BODY,PL,EL:7 WIRE GREEN	80009	352-0165-05
	352-0165-06			1		. CONN BODY,PL,EL:7 WIRE BLUE	80009	352-0165-06
	352-0165-07			1		. CONN BODY,PL,EL:7 WIRE VIOLET	80009	352-0165-07
	352-0165-08			2		. CONN BODY,PL,EL:7 WIRE GRAY	80009	352-0165-08
	175-2872-00			1		CA ASSY,SP,ELEC:4,18 AWG,10.0L	80009	175-2872-00
	----- -----			-		(FROM A86 TO A80J4) SUBPART OF A86		
	195-0540-00			2		LEAD,ELECTRICAL:26 AWG,1.5 L,9-1	80009	195-0540-00
	----- -----			-		(FROM U5015,U5040,TO A26) SUBPART OF A26		
	352-0171-00			2		. HLDR,TERM CONN:1 WIRE BLACK	80009	352-0171-00
	195-0541-00			2		LEAD,ELECTRICAL:26 AWG,1.5 L,9-2	80009	195-0541-00
	----- -----			-		(FROM U5015,U5040 TO A26) SUBPART OF A26		
	352-0171-00			2		. HLDR,TERM CONN:1 WIRE BLACK	80009	352-0171-00
	195-0542-00			2		LEAD,ELECTRICAL:26 AWG,1.5 L,9-3	80009	195-0542-00
	----- -----			-		(FROM U5015,U5040 TO A26) SUBPART OF A26		
	352-0171-00			2		. HLDR,TERM CONN:1 WIRE BLACK	80009	352-0171-00
	195-0581-00			2		LEAD,ELECTRICAL:26 AWG,1.5 L,9-1	80009	195-0581-00
	----- -----			-		(FROM U5015,U5040 TO V5201,V5202)		
	195-0582-00			2		LEAD,ELECTRICAL:26 AWG,1.5 L,9-2	80009	195-0582-00
	----- -----			-		(FROM U5015,U5040 TO V5201,V5202)		
	198-4187-00			1		WIRE SET,ELEC:	80009	198-4187-00
	----- -----			-		(FROM A80J2 TO S5021)		
	----- -----			-		(FROM A80J3 TO B5020)		
	----- -----			-		(FROM A82P060 TO BNC'S)		
	----- -----			-		(SUBPART OF POWER SUPPLY ASSY)		
	175-0826-00			1		. WIRE,ELECTRICAL:3 WIRE RIBBON	80009	175-0826-00
	204-0671-00			1		. CONN BODY,PLUG:1 X 3 CONTACTS NYLON	27264	09-50-7031
	204-0749-00			1		. CONN BODY,PLUG:CKT CD,5 CONTW/O LKG RAMP	27264	2139-052
	352-0161-04			1		. CONN BODY,PL,EL:3 WIRE YELLOW	80009	352-0161-04
	198-4248-00			1		WIRE SET,ELEC:	80009	198-4248-00
	----- -----			-		(FROM A68J006 TO J13 AND DS5114)		
	175-0827-00			1		. CABLE,SP,ELEC:4,26 AWG,STRD.PVC JKT,RBN	08261	SS04267(1061)0C
	175-0828-00			2		. WIRE,ELECTRICAL:5 WIRE RIBBON	08261	SS-0526-710610C
	352-0330-00			1		. HLDR,TERM. CONN:44 WIRE,DBL ROW,BLACK	22526	65043-015

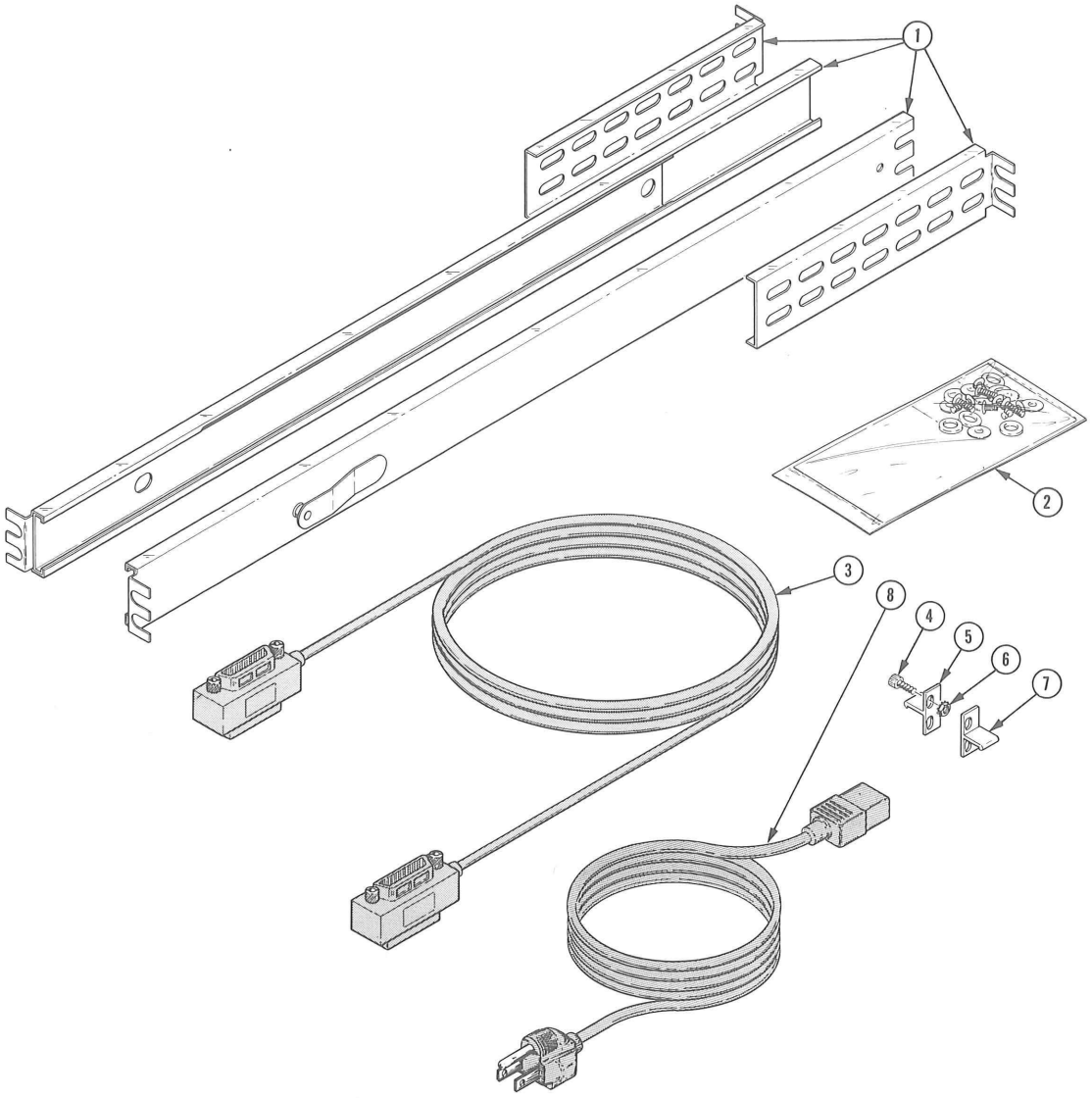


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
-1	351-0375-00	B010100	B030190	1PR		SLIDE,DWR,EXT:24.0 X 1.69	80009	351-0375-00
	351-0375-01	B300191		1PR		SLIDE,DWR,EXT:W/CLOSED MOUNTING SLOTS	80009	351-0375-01
-2	016-0099-00			1		HDW KIT,ELEK EQ:RACKMOUNT HDW	80009	016-0099-00
-3	012-0630-03			1		CABLE,INTCON:2 METERS L	74868	AC30147-102
	020-0398-00			1		COMPONENT KIT:	80009	020-0398-00
-4	212-0615-00			4		. SCREW,CAP:10-32 X 0.625 INCH,STL	83385	OBD
-5	105-0757-00			1		. STRIKE,LATCH:LEFT	80009	105-0757-00
-6	220-0410-00			4		. NUT,EXTENDED WA:10-32 X 0.375 INCH,STL	83385	OBD
-7	105-0758-00			1		. STRIKE,LATCH:RIGHT	80009	105-0758-00
-8	161-0066-00			1		CABLE ASSY,PWR,:3,18 AWG,115V,98.0 L	16428	KH8481
	070-2386-00			1		MANUAL,TECH:OPERATORS 7612D DUAL	80009	070-2386-00
	070-2387-00			1		MANUAL,TECH:SERVICE 7612D DUAL CHANNEL	80009	**070-2387-00**

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: Aug. 9, 1982 Change Reference: M44227 REV

Product: 7612D Service - Manual Part No.: 070-2387-00

DESCRIPTION

EFF SN B030556

REPLACEABLE ELECTRICAL PARTS & SCHEMATIC CHANGES

CHANGE TO:

A76	670-4949-03	CKT BOARD ASSY:HIGH VOLTAGE OSC
A76C308	290-0977-00	CAP,FXD,ELCTLT:470 UF,63V
A76C310	290-0977-00	CAP,FXD,ELCTLT:470 UF,63V

These capacitors are located on the HIGH VOLTAGE OSC board, and are shown on Diagram 12.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: March 23, 1983 Change Reference: M50366

Product: 7612D Service Manual Part No.: 070-2387-00

DESCRIPTION

EFF SN B030869

REPLACEABLE ELECTRICAL PARTS & SCHEMATIC CHANGES

CHANGE TO:

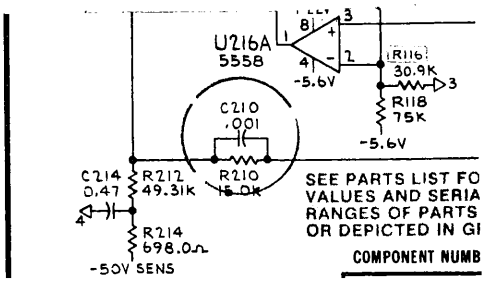
A88	670-4954-03	CKT BOARD ASSY:REGULATOR

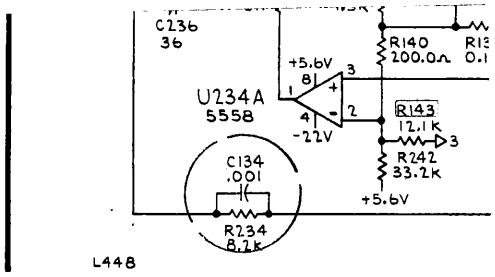
REMOVE:

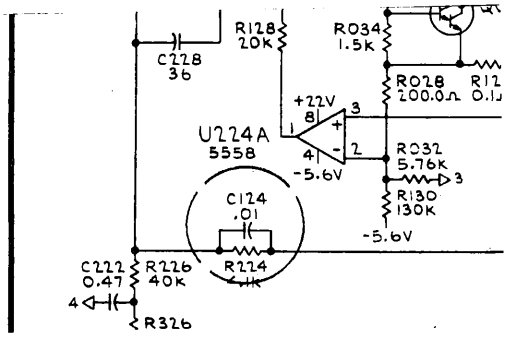
A88C124	285-0598-00	CAP,FXD,PLSTC:0.01 UF,5%,100V
A88C134	285-0862-00	CAP,FXD,PLSTC:0.001 UF,10%,100V
A88C210	285-0862-00	CAP,FXD,PLSTC:0.001 UF,10%,100V

These capacitors are located on the A88-REGULATOR board, and are shown on Diagram 29.

PARTIAL DIAGRAM 29







Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: June 22, 1983 Change Reference: M49856

Product: 7612D and 7912AD Manual Part No.: See Below

DESCRIPTION

EFF SN:B031015 (7612D) 070-2387-00
B111211 (7912AD) 070-2385-00

REPLACEABLE ELECTRICAL PARTS & SCHEMATIC CHANGES

CHANGE TO:

A56	670-5773-03	CKT BOARD ASSY:IEEE 488 INTERFACE(7612D)
A56	670-4946-05	CKT BOARD ASSY:7912AD/GPIB INTERFACE
A56R610	321-0203-00	RES,FXD,FILM:1.27K OHM,1%,0.125W

This resistor is located on the A56-Interface board, and is shown on Diagram 22(7612D), or Diagram 29(7912AD), XYZ DISPLAY.